

LMC669 Auto-Zero

General Description

The LMC669 uses sampled-data techniques to reduce the input offset voltage (V_{OS}) of an amplifier or system to approximately $5\ \mu\text{V}$. A four-stage comparator samples the summing node of an inverting amplifier and generates a correction voltage that is applied to the amplifier's non-inverting input. The offset correction is independent of time, temperature, and supply voltage, and requires no initial or periodic user offset adjustments.

The user may also adjust clock frequency, sample rate, and the correction voltage's step size and magnitude.

The Auto-Zero operates on supply voltages of $\pm 8\text{V}$ to $\pm 20\text{V}$ with a quiescent current of $3\ \text{mA}$.

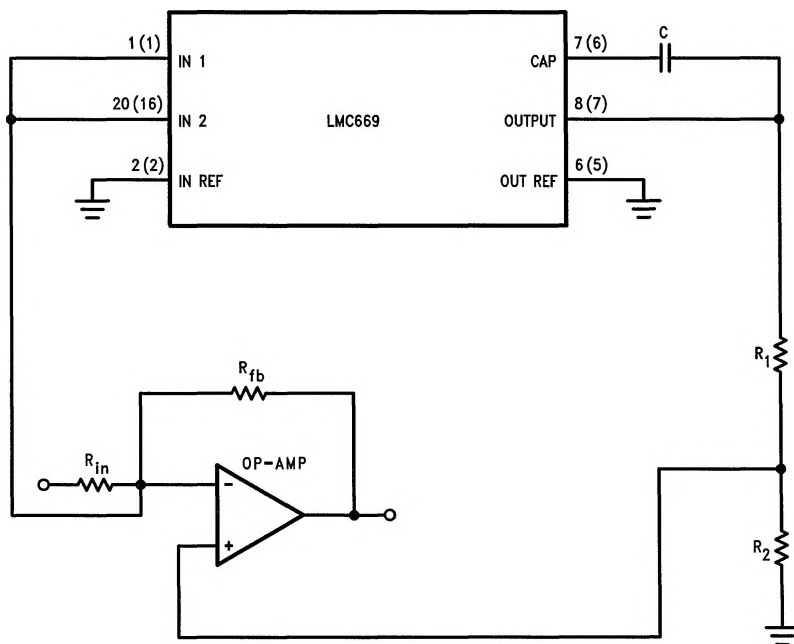
The use of the LMC669 does not limit the performance of the amplifier it is used with. Full use of the gain-bandwidth product, slew rate, and DC gain is retained.

The LMC669 can be used as a precision comparator with a latched, open drain output, or as a low-offset inverting operational amplifier for low-speed applications.

Features

- 5 microvolts typical offset voltage
- Temperature independent offset correction
- Internal or external clocking
- Automatic and continuous offset voltage correction
- High voltage CMOS—up to $\pm 20\text{V}$ supplies

Typical Application



Numbers in () are for 16-pin packages

TL/H/8561-1

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Positive Supply Voltage (V^+)	+22V
Negative Supply Voltage (V^-)	-22V
Voltage of Logic Pins T1, T2, RESET, CLK	-0.2V to ($V^+ + 0.2V$)
Voltage at Inputs	-0.2V to ($V^+ + 0.2V$)
Input Current (Note 3) INREF, IN1 and IN2	20 mA

Power Dissipation (Note 4)	500 mW
Storage Temperature	-65°C to +150°C
Lead Temp. (soldering, 10 seconds)	300°C

Operating Ranges (Notes 1 & 2)

Temperature Range	$T_{MIN} \leq T_A \leq T_{MAX}$ LMC669D -40°C $\leq T_A \leq$ +85°C
Positive Supply Voltage	+8V to +20V
Negative Supply Voltage	-8V to -20V
INREF, IN1 and IN2 Voltage (Note 5)	-200 mV to +2V
ESD rating to be determined.	

Electrical Characteristics The following specifications apply for $V^+ = +15V$, and $V^- = -15V$ unless otherwise specified. **Boldface limits apply for T_{MIN} to T_{MAX}** ; all other limits $T_A = T_J = 25^\circ C$.

Symbol	Parameter		Conditions	Typical (Note 6)	Tested Limit (Note 7)	Design Limit (Note 8)	Units
V_{OS}	Maximum Input Offset Voltage (Note 9)	LMC669BIN, BIM	Signal applied to both IN1 & IN2, $T_{CLK} =$ 50 μs , $V_{INREF} =$ 0V, 0.5V	± 5	$\pm \mathbf{25}$		μV
		LMC669BCN, BCM			± 25		
		LMC669CIN, CIM		± 10	$\pm \mathbf{50}$		
		LMC669CCN, CCM			± 50		
		LMC669CD		± 5	$\pm \mathbf{25}$		
V_{OS}	Maximum Input Offset Voltage (Note 9)	LMC669BIN, BIM	Signal applied only to IN1 or IN2, $T_{CLK} =$ 50 μs , $V_{INREF} =$ 0V	± 10	$\pm \mathbf{50}$		μV
		LMC669BCN, BCM			± 50		
		LMC669CIN, CIM		± 20	$\pm \mathbf{100}$		
		LMC669CCN, CCM			± 100		
		LMC669CD		± 10	$\pm \mathbf{50}$		
I_b	Maximum Input Bias Current	IN2	Clock Off	1	100		pA
				400			pA
		IN1 or IN1 & IN2		5	100		pA
				40		75	nA
$\frac{\Delta V_{OS}}{\Delta T}$	Average Input Offset Drift			0.1			$\mu V/^\circ C$
V_{IN1}, V_{IN2}	IN1 & IN2 Input Voltage Range (Note 5)	min		-200	0		mV
		max		+2.0	+0.5		V
V_{INREF}	IN REF Input Voltage Range (Note 5)	min		-200	0		mV
		max		+2.0	+0.5		V
V_{OUTREF}	OUT REF Input Voltage Range	min		-100			mV
		max		+100			mV
PSRR	Power Supply Rejection Ratio			120			dB
V_{OUT}	Integrator Output Voltage Range			± 14	± 12	$\pm \mathbf{11}$	V
V_{CO}	Comparator Open-Drain Output Voltage Range	Low (max)	Sink Current = 1.0 mA	0.25	0.4		V
		High (min)		25	20	19	
I_S^+	Maximum Positive Supply Current		RESET Low, $T_{CLK} = 50 \mu s$	3.2	6.0		mA
					10.0		

Electrical Characteristics The following specifications apply for $V^+ = +15V$, and $V^- = -15V$ unless otherwise specified. **Boldface limits apply for T_{MIN} to T_{MAX}** ; all other limits $T_A = T_J = 25^\circ C$. (Continued)

Symbol	Parameter		Conditions	Typical (Note 6)	Tested Limit (Note 7)	Design Limit (Note 8)	Units
I_{S-}	Maximum Negative Supply Current		$\overline{RESET}$ Low, $T_{CLK} = 50 \mu s$	2.0	5.0		mA
					7.0		
f_S	Maximum Sample Rate		$\overline{RESET}$ Low, Internal Clock	100	66.6	56	kHz
f_{CLK}	Clock Frequency Range	min		100		100	Hz
		max		100		100	kHz
T_R	Minimum $\overline{RESET}$ Pulse Width			80	150	175	ns
V_{TH}	Digital Input Threshold Voltage	T1, T2, $\overline{RESET}$	High (min)	2.9	3.5		V
			Low (max)	2.9	1.5		V
		CLK	High (min)	3.5	4.0		V
			Low (max)	1.5	1.0		V
I_{DIN}	T1, T2, $\overline{RESET}$, & CLK Maximum Digital Input Current	High		1.0			pA
					1.0		μA
		Low		1.0			pA
					1.0		μA

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating conditions.

Note 2: All voltages are with respect to AGND.

Note 3: This input current will exist only when an input is driven to a voltage greater than $(V^+ + 0.2V)$ or less than $-0.2V$. It is due to internal diode clamps at the inputs turning on. If the current is limited to 20 mA, the overdrive will not be harmful to the LMC669.

Note 4: The typical junction-to-ambient thermal resistance (θ_{JA}) of the 16 pin J package is $80^\circ C/W$.

Note 5: If input currents are limited, input voltages may be driven beyond these limits and the device will still be functional. The comparator output will be correct as long as the voltage on either the INREF pin or the two input IN1 & IN2 pins is between $-200 mV$ and $+2V$.

Note 6: Typicals are at $25^\circ C$ and represent most likely parametric norm.

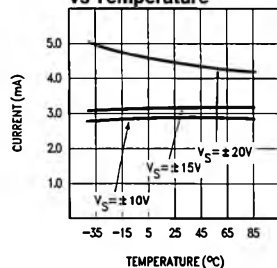
Note 7: Guaranteed and 100% tested.

Note 8: Guaranteed, but not 100% production tested. These limits are not used to calculate outgoing quality levels.

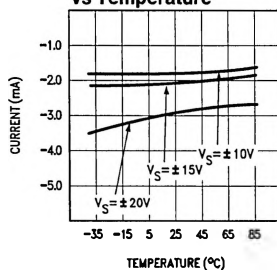
Note 9: The LMC669CD exhibits a warm-up drift of approximately $3 \mu V$ to $5 \mu V$ in the negative direction. There are two factors that work together to cause this. Firstly, as the die becomes warm, a temperature gradient forms between pin 2 and pins 1 and 16. Secondly, a thermocouple is created between the metal of the leadframe and the metal of the wire (usually copper) used to connect the IC to a circuit. It takes about 6 minutes for the drift to stabilize. The N and M packages do not exhibit this drift because their leadframes are 90% copper.

Typical Performance Characteristics

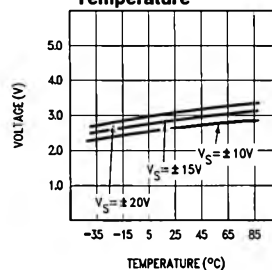
Positive Supply Current vs Temperature



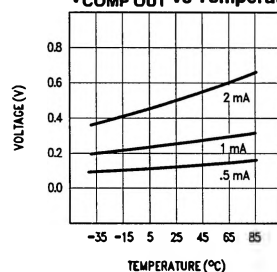
Negative Supply Current vs Temperature



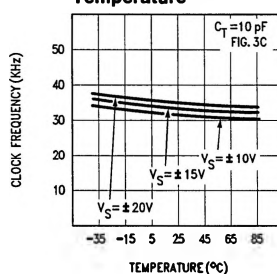
T1, T2 & RESET thresholds vs Temperature



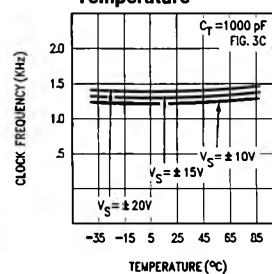
V_{COMP} OUT vs Temperature



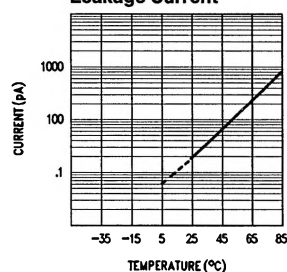
Clock Frequency vs Temperature



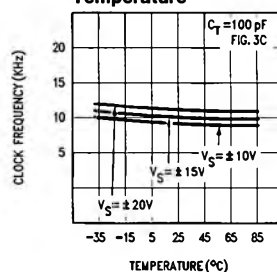
Clock Frequency vs Temperature



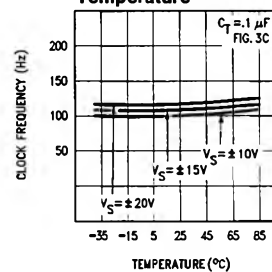
Integrator Summing Node Leakage Current



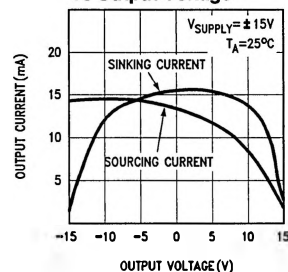
Clock Frequency vs Temperature



Clock Frequency vs Temperature



Output Current Limit vs Output Voltage

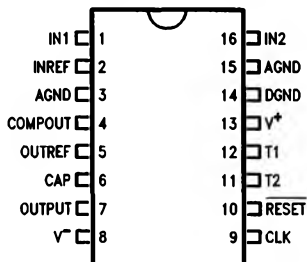


TL/H/8561-2

TL/H/8561-3

Connection Diagram

16-Pin Dual-In-Line Package

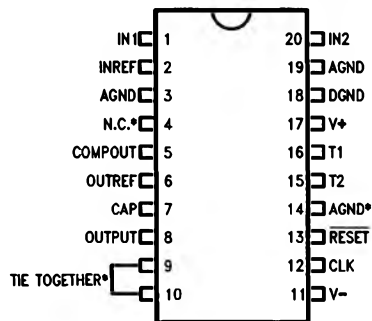


Top View

TL/H/8561-4

Order Number LMC669D
See NS Package Number D16C

20-Pin Dual-In-Line (N) Package
20-Pin Small-Outline (M) Package



Top View

TL/H/8561-17

*These pins must be connected as shown to ensure compatibility with future parts.

Pin Description LMC669 Numbers in () are for 16-pin package

Pin	Description
IN1, IN2 1, 20 (1, 16)	These are the inputs to the Auto Zero's comparator. They should be tied together and connected to the summing node of the host operational amplifier (op amp). One set of inputs, either IN1 and IN2 or INREF, must be between +2 volts and ground while the other can go to V^+ (also refer to notes 3 and 5).

Pin	Description
INREF 2 (2)	This is the input for the comparator's reference voltage. Correction of V_{OS} is accomplished by connecting this pin to a good clean system ground of its own. One set of inputs, either IN1 and IN2 or INREF, must be between +2 volts and ground while the other can go to V^+ (also refer to notes 3 and 5).

Pin Description 16-pin LMC669 (Continued)

Pin	Description
AGND 3, 19 (3, 15)	These act to shield the IN1, IN2, and INREF connections from stray capacitance and leakage which could degrade the part's performance. They should be connected to a high quality ground.
DGND 18 (14)	Provides a separate ground for the internal digital circuitry to prevent noise from corrupting the comparator inputs. It should have its own ground connection.
COMPOUT 5 (4)	This is the latched output from the internal comparator. It is an open drain which can be left unconnected if not needed. Its response time is equal to the sample rate's period. The rise time, from 10% to 90%, is nominally 500 ns with a 10 k Ω pull-up resistor. The output is typically capable of swinging from +0.25 (at 1 mA) to +25 volts.
OUTREF 6 (5)	Output reference; for proper integrator operation this input should be connected to a good system ground, such as the ground to which INREF is connected.
OUTPUT 8 (7)	This is the LMC669's integrator output. It can swing from -12 to +12 volts in 0.2 volt steps with a ≥ 10 K Ω load and no external integrating capacitor.
CAP 7 (6)	When a capacitor is used to decrease the correction voltage's step size, it is connected between CAP and OUTPUT. It parallels an internal 10 pF capacitor.
CLK 12 (9)	External clock input/internal adjust. The frequency of the internal clock (nominally 100 kHz) may be reduced with an external capacitor or an external clock connected to the CLK input. The logic thresholds for this input are 4 volts for a logic high and 1 volt for logic low. The internal clock can be stopped by applying a logic high, through a diode, to the CLK input. When a logic low is applied to the diode, the internal clock runs freely. (See Figure 3)
RESET 13 (10)	Comparator reset. At power-up, or when RESET is pulled low during normal operation, the Auto Zero will run at its fastest sample rate. This allows for the quickest V_{OS} nulling.
4	Leave this pin unconnected.
9, 10	Connect these pins together.
14	Connect to analog ground.

Pin	Description
T1, T2 16, 15 (12, 11)	These pins select one of five clock divider ratios. The ratio, hence the sample rate can be changed by applying V^+ or ground to T1 and T2. The ratio chosen by these inputs is valid after the comparator's output changes state; i.e., a zero-crossing between the offset and correction voltage has taken place. These inputs can also be changed at any time to modify the LMC669's sample rate. Use the table below to determine the reduction in the clock's frequency for each combination of T1 and T2.

T1	T2	RESET	$\div$
X	X	0	1
1	1	1	4
1	0	1	16
0	1	1	128
0	0	1	1024

V^+ , V^-
17, 11
(13, 8)

Positive and negative power supply inputs. Typical supply voltages are ± 15 volts, but operation will take place from ± 8 to ± 20 volts. Power supply current is typically 3 mA. Bypass capacitors (0.01 $\sim$ 0.1 μ F) should be connected to the power supply pins.

Application Hints

1.0 INTRODUCTION

In its standard application shown in *Figure 1*, the LMC669 continuously samples the summing node of an inverting amplifier and generates a correction voltage for the amplifier's non-inverting input, nulling the amplifier's input offset voltage (V_{OS}) to 5 μ V. The offset correction is independent of time, temperature, and supply voltage. The LMC669 eliminates the need for initial or periodic offset adjustments, compensates for V_{OS} drift due to temperature changes, allows the use of greater DC gain, and increases immunity to changes in power supply voltages.

At the input of the LMC669 is a sampled-data differential comparator with very low offset voltage. When the comparator samples the summing node voltage and determines that it is not at ground, the LMC669's output generates a small voltage step in the opposite direction of the error. The size of the step and the sample rate are user-selectable. The correction voltage continues to step up or down until the summing node is within the V_{OS} of the LMC669—typically 5 μ V. At this point the Auto Zero continues to monitor the summing node and perform any needed corrections. An internal divider generates five different sampling rates for any given clock frequency.

The only external parts needed for V_{OS} correction of most amplifiers are two resistors and one capacitor. Since the capacitor is in the feedback loop of an integrator, it should be a low leakage type (polycarbonate, polypropylene, polystyrene, mylar, etc.). The tolerance of the resistors and capacitor is not critical (10% components are satisfactory).

Application Hints (Continued)

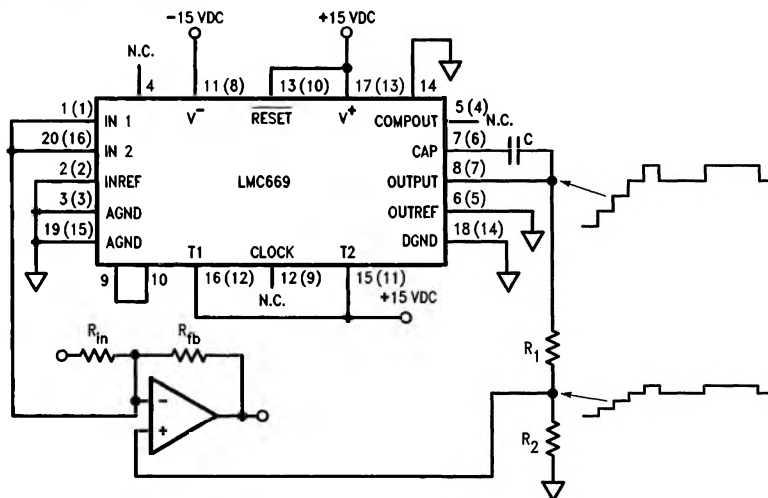


FIGURE 1. Typical Application

TL/H/8561-5

1.1 CIRCUIT OPERATION

At the heart of the LMC669 is a four-stage precision sampled-data comparator, shown in Figure 2. The circuit operates by successively zeroing the offset of each stage, resulting in a very high gain amplifier with extremely low input offset voltage.

After a comparator decision is made, the latch is enabled and holds the comparator's output state. At the same time this state appears at COMPOUT. The latch also generates a $\pm 1V$ signal that charges capacitor C_1 to $\pm 1V$. C_1 's charge is then transferred to the integrator's feedback capacitor C_2 . Since C_2 is five times larger than C_1 , a 200 mV step will appear at the integrator's output. Further reduction of the step size is possible with an external capacitor connected in parallel with C_2 (between OUTPUT and CAP). The integrator output is then attenuated by a resistive divider network before being applied to the external op amp's non-inverting input, completing the offset correction loop.

1.2 CLOCKS

In order to control the events that take place in the LMC669, an internal Schmitt trigger oscillator generates a 100 kHz clock. This oscillator's frequency can be lowered by connecting a capacitor between the CLK input and ground as in Figure 3c. It can also be overridden by applying an external clock source (≤ 100 kHz) to the CLK input (Figure 3a). Further, the clock can be halted with a diode connected as shown in Figure 3(b).

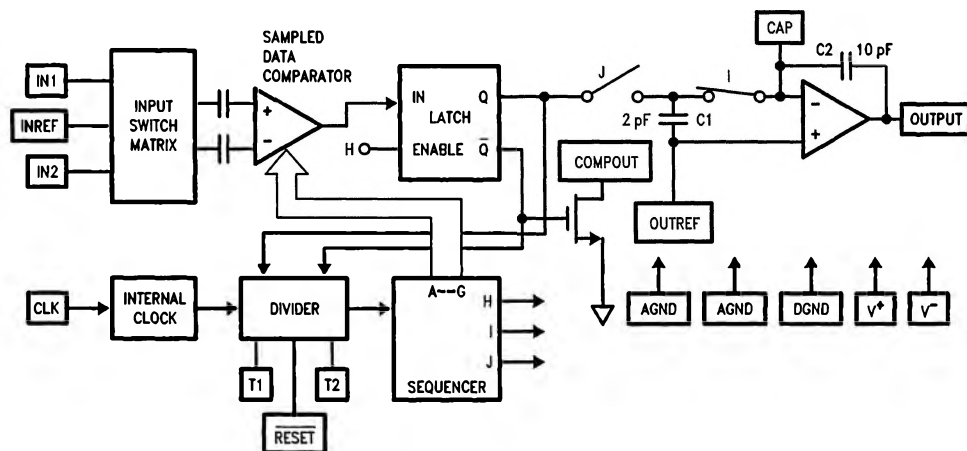
The clock signal drives the input of the divider (See Figure 2). Depending on the logic levels at inputs T1, T2, and RESET, the clock can be divided by five different ratios (1, 4, 16, 128, and 1024). The output of the divider triggers the sequencer which controls the auto-zero function.

When the LMC669 is powered-up or reset the internal divider automatically divides by one. This allows the Auto-Zero to operate at maximum sampling rate so that large initial offsets can be rapidly corrected. When the comparator toggles for the first time, this indicates that input null has been achieved and that maximum sample rate is no longer required. The latch then switches the divider from $\div 1$ to the ratio programmed via T1 and T2. By employing this "two speed" approach the device can move quickly to handle turn-on transients and then shift to the optimum "gear" for long term offset correction. It is also possible to return to the maximum sample rate via the RESET input so that non-power-up transients can be dealt with as well.

1.3 INPUT RANGE

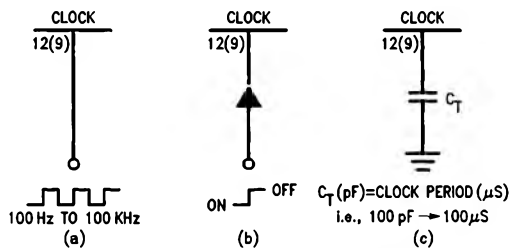
The IN1, IN2, and INREF inputs can accept signal levels between 0 and +2 V. However, as long as both IN1 and IN2, or INREF, is kept between 0 and 2V the other input (or inputs) can be taken to V^+ and, if input current limiting (≤ 20 mA) is provided, to V^- . In most auto-zero applications IN1 and IN2 will be able to go to these extended limits since INREF will normally be grounded.

Application Hints (Continued)



TL/H/8561-6

FIGURE 2. Block Diagram



TL/H/8561-8

FIGURE 3. Clock Input. External clock (a), controlling internal clock (b), reducing internal clock frequency (c).

Application Hints (Continued)

2.0 APPLICATION CIRCUITS

The most general application of the Auto-Zero is offset correction of an inverting op amp as shown in *Figure 1*. The example below shows how the integration capacitor and the resistor divider are chosen.

Determine the maximum expected offset voltage from the op amp characteristics and the requirements of the overall system. The correction voltage swing capability should be greater than or equal to this value. Also select the minimum system resolution and the time that can be allowed to null the initial offset. These will determine the correction voltage step size. The magnitude of the correction voltage (V_{corr}) and the step size (dv) are defined according to equations 1 and 2:

$$\text{Correction voltage} = V_{corr} = V_{out} \frac{R_2}{R_1 + R_2} \quad (1)$$

V_o is typically $\pm 12V$ for $\pm 15V$ supplies.

$$R_2 = \frac{R_1 V_{corr}}{(V_o - V_{corr})} \quad (1a)$$

$$= \frac{10K V_{corr}}{(12 - V_{corr})}$$

for $R_1 = 10 k\Omega$ (For proper operation $R_1 + R_2$ should be greater than $10 k\Omega$.)

$$\text{step size} = dv = 1.0V \left(\frac{C_1}{C_2 + C} \right) \left(\frac{R_2}{R_1 + R_2} \right) \quad (2)$$

$$C = \frac{C_1 R_2}{dv (R_1 + R_2)} - C_2 \quad (2a)$$

with $C_1 = 2 pF$, $C_2 = 10 pF$, R_1 and R_2 from Eq. 1a. C_1 and C_2 are internal.

A further consideration regarding the selection of step size is resolution: the magnitude of the smallest significant signal. In the case of nulling the V_{os} of an op amp used with a digital-to-analog converter (DAC) the smallest signal is the voltage produced by the least-significant bit (LSB). Therefore, the correction voltage's step size would need to be much smaller than the magnitude of the DAC's LSB in order to retain the DAC's desired resolution.

Finally, for proper operation, the sampling period should be longer than the amplifier's settling time. $10 \mu s$ or more should be adequate for most contemporary amplifiers.

DESIGN EXAMPLE

As an example, assume that the offset of the op amp in *Figure 1* is expected to be no more than $15 mV$ and the system can tolerate a $1 \mu V$ square wave at a rate equal to the internal clock. Begin by using R_1 and R_2 to set the maximum correction voltage to $15 mV$. The LMC669's output can swing to ± 12 volts with a $10 k\Omega$ load and a ± 15 volt power supply. R_1 and R_2 should be chosen to reduce this to $15 mV$:

$$R_2 = \frac{R_1 V_{corr}}{V_o - V_{corr}}$$

$$= \frac{(10K)(0.015)}{(12 - 0.015)}$$

$$= 12.5\Omega \approx 13\Omega$$

for $\pm 15V$ supplies and $R_1 = 10K$.

Now choose C , the integrator's external feedback capacitor, to set the final step size to $1 \mu V$. Using equation (2a):

$$C = \frac{C_1 R_2}{dv(R_1 + R_2)} - C_2$$

with $R_1 = 10 k\Omega$, $R_2 = 13\Omega$, $C_1 = 2 pF$,

and $C_2 = 10 pF$, yields

$$C \approx 2500 pF$$

The null time for this example, with an amplifier offset of $15 mV$, step size of $1 \mu V$, and initial sample rate of $100 kHz$, is

$$\text{Null time} = \frac{V_{os}}{(dv)(\text{sample rate})} \quad (3)$$

$$= 150 \text{ msec}$$

If this is too slow, the step size can be increased.

OP AMP INPUT BIAS CURRENT

Input bias current should be considered when selecting an op amp that is nulled by the LMC669. If this current is too high, the result is a significant voltage drop across the feedback components and consequent output offset. The Auto Zero will not correct this error since it does not appear as a voltage at the summing node. Therefore, use low resistance feedback networks, or op amps with low input bias current such as the LF156, LF400, and LF411.

NOISE

Through careful selection of the sample rate and step size a compromise can be made between noise and null time. Low sample rates achieve low noise but take a long time to null an offset or correct it when a sudden change occurs. High sample rates can quickly null or correct changes in V_{os} but do so with an increase in noise. Step size directly affects the null time and the amount of noise introduced: small step sizes ($< 100 nV$) contribute almost no noise, but result in long null times.

Low noise LMC669 applications are beneficial to instrumentation and audio electronics. An LM833 low noise operational amplifier ($4.5 nV / \sqrt{Hz}$) with the LMC669 is shown in *Figure 4*. In this circuit the Auto Zero adds only $1 nV / \sqrt{Hz}$ referred to the amplifier's input. To achieve this the step size is set to $100 nV$. The sample rate, with the internal clock free-running, is set to $98 Hz$ (clock frequency $\div 1024$), and input and output filters are added to the LMC669. The input filter prevents switching transients from reaching the amplifier input and the output filter attenuates AC components of the steps at the Auto Zero's output. The filter at the op amp's input also introduces a pole at

$$F_p = \frac{1}{2\pi(R_{in} + R_i)C_i}$$

and a zero at

$$F_z = \frac{1}{2\pi R_i C_i}$$

The maximum V_{os} that can be corrected by the circuit in *Figure 4* is $12 mV$. More offset correction can be obtained while retaining good noise performance by increasing the size of R_2 and C the same percentage. Increasing C compensates for the reduced attenuation caused by increasing R_2 . This allows the step size to remain the same but increases the amount of correction voltage applied to the op amp.

Application Hints (Continued)

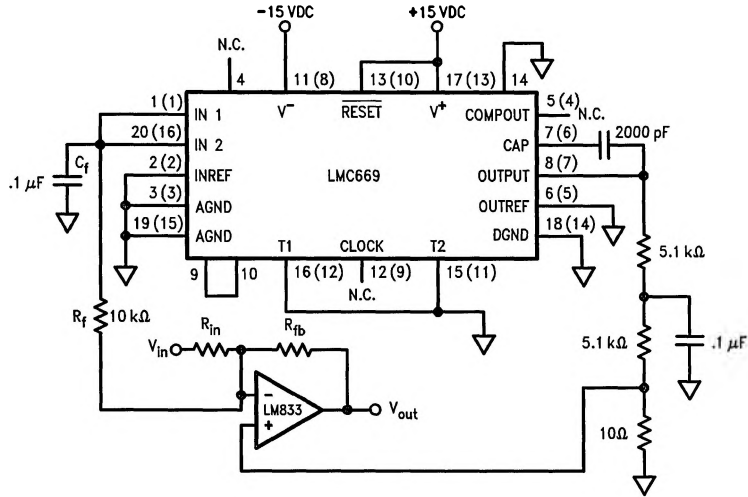


FIGURE 4. Low Noise Application

TL/H/8561-9

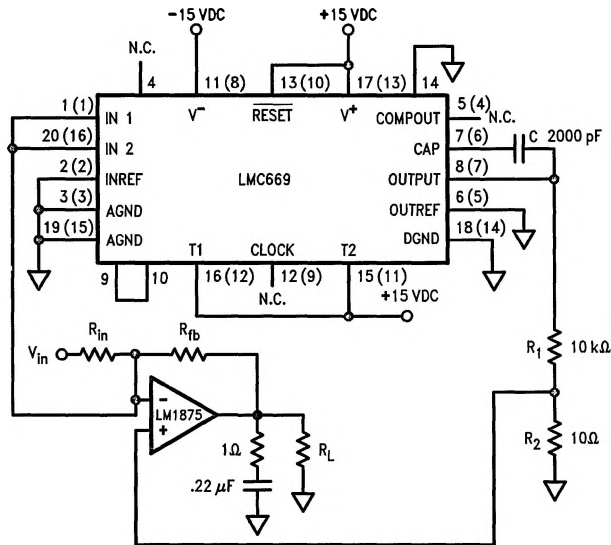


FIGURE 5. Zeroing LM1875 Power Op-Amp

TL/H/8561-10

Application Hints (Continued)

POWER AMPLIFIERS

For applications such as motor control, automated servo systems, and power amplification the LMC669 can also be used with amplifiers other than standard small signal op amps. *Figure 5* shows how the Auto Zero can allow an LM1875 audio power amplifier to operate with very low offset. While the sample rate for this configuration is not critical, the LMC669's output step size should be set for less than 1 μV to ensure low system noise.

NON-INVERTING AMPLIFIERS AND SYSTEMS

A variation of the above circuit appears in *Figure 6* with the LMC669 operating as a DC-servo integrating feedback loop. This configuration is applicable when the Auto Zero is used with non-inverting op amps amplifying AC-only signals. The output error of the amplifier is reduced to the V_{OS} of the Auto Zero, typically $5\ \mu\text{V}$. A filter at the input of the LMC669 limits current and ensures that only DC and very low frequencies

(< 0.6 Hz) are sampled. In this application the output of the op amp is sampled and compared with a reference ground. The correction output from the Auto Zero now replaces the ground reference for the feedback resistor connected to the inverting input.

Systems can also benefit from the Auto Zero. *Figure 7* shows how the V_{OS} of an MF6 Butterworth low-pass switched capacitor filter is nulled by the LMC669. The Auto Zero's IN1 and IN2 inputs are connected to the MF6's output while INREF is connected to its input. The correction signal is applied to the MF6's V_{OS} ADJ input. RC low-pass filters (R_{11} , C_{11} and R_{12} , C_{12}) are used to reduce AC signals at the LMC669's inputs and provide current limiting. It is important to set each passive RC filter's cutoff as low as possible, at most 0.1 of the MF6's f_o .

This correction makes the MF6 useful in applications calling for good DC accuracy. The MF6's typical 250 mV offset is decreased to 5 μ V with a step size of 1 μ V.

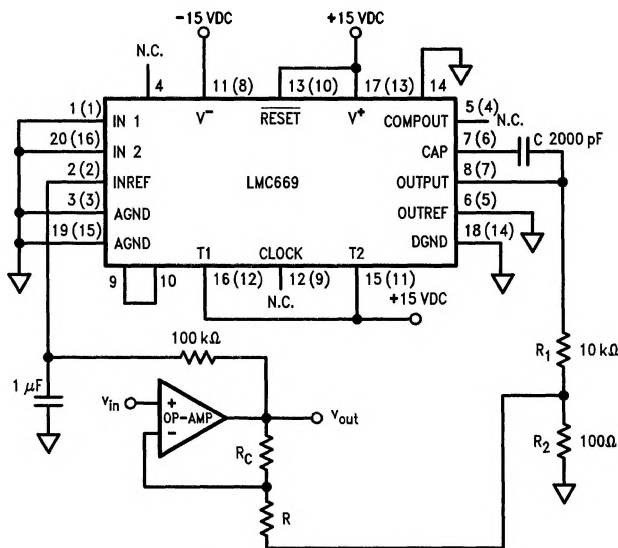


FIGURE 6. DC Servo Loop

TL/H/8561-11

Application Hints (Continued)

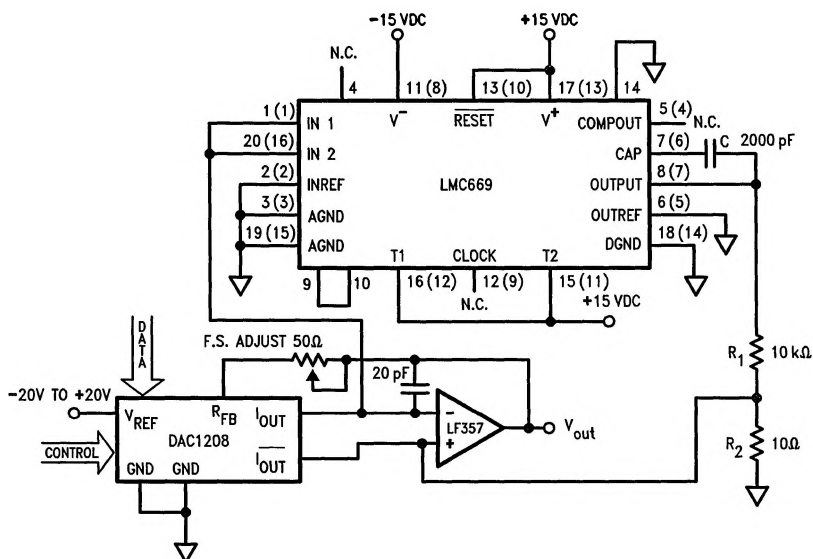


FIGURE 8. Reducing V_{OS} -Induced linearity errors in a 12-bit DAC by 0.01% /mV offset.

TL/H/8561-13

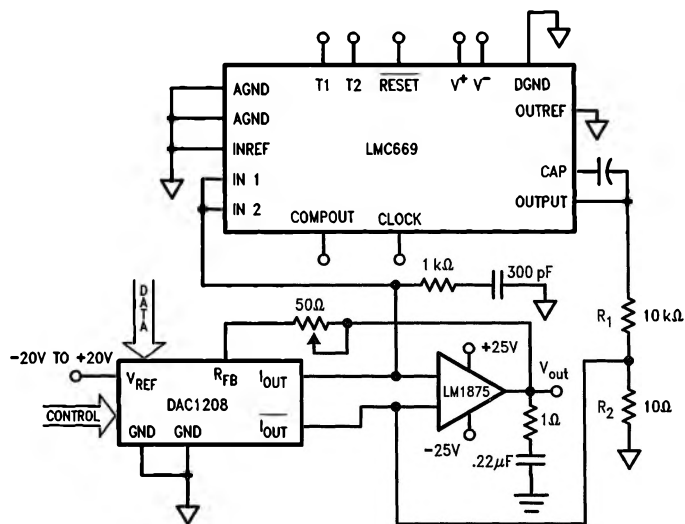


FIGURE 9. Power DAC with $\pm 20V_{p-p}$ and 3A output capabilities.

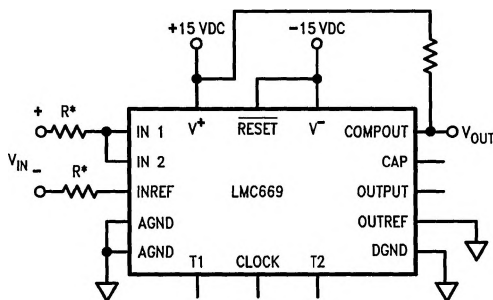
TL/H/8561-14

Application Hints (Continued)

LOW-FREQUENCY, HIGH-GAIN AMPLIFIER

For applications that require precision high-gain DC and low-frequency performance, the LMC669 can be connected as an amplifier as shown in Figure 11. For a closed-loop gain of ~ 1000 the useful frequency range is typically

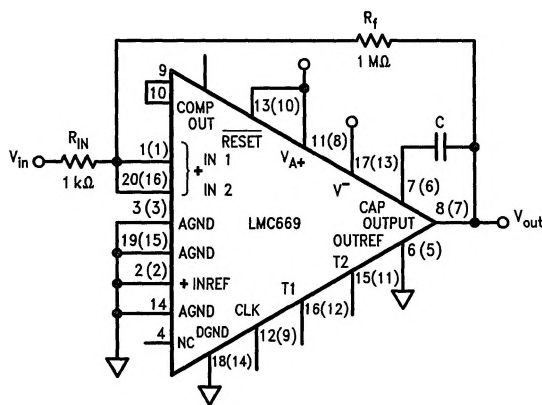
$$F_{\max} = 20 \frac{\text{Hz}}{\text{mV of step size}}$$



TL/H/8561-16

*R = 10K. For inputs greater than 2 volts.

FIGURE 10. Low-Speed Precision Comparator



TL/H/8561-15

**FIGURE 11. Low Offset, High Gain,
Low Frequency Op Amp.**

$$\text{Bandwidth} \approx 20 \frac{\text{Hz}}{\text{mV of step size}}, \text{ sample rate} = 100 \text{ kHz.}$$