# National Semiconductor

## LMF100 High Performance Dual Switched Capacitor Filter

## **General Description**

The LMF100 consists of two independent general purpose high performance switched capacitor filters. With an external clock and 2 to 4 resistors, various second-order and first-order filtering functions can be realized by each filter block. Each block has 3 outputs. One output can be configured to perform either an allpass, highpass, or notch function. The other two outputs perform bandpass and lowpass functions. The center frequency of each filter stage is tuned by using an external clock or a combination of a clock and resistor ratio. Up to a 4th-order biquadratic function can be realized with a single LMF100. Higher order filters are implemented by simply cascading additional packages, and all the classical filters (such as Butterworth, Bessel, Elliptic, and Chebyshev) can be realized.

The LMF100 is fabricated on National Semiconductor's high performance analog silicon gate CMOS process,

LMCMOSTM. This allows for the production of a very low offset, high frequency filter building block. The LMF100 is pin-compatible with the industry standard MF10, but provides greatly improved performance.

#### Features

Wide 4V to 15V power supply range

Operation up to 100 kHz	
Low offset voltage	typically
(50:1 or 100:1 mode)	$Vos1 = \pm 5 mV$
	$Vos2 = \pm 15 \text{ mV}$
	$Vos3 = \pm 15 \text{ mV}$
Low crosstalk -60 dB	

- Clock to center frequency ratio accuracy ±0.2% typical
- If  $f_0 \times Q$  range up to 1.8 MHz
- Pin-compatible with MF10



## Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V+ – V-)	16V
Voltage at Any Pin	V <sup>+</sup> + 0.3V
	V 0.3V
Input Current at Any Pin (Note 2)	5 mA
Package Input Current (Note 2)	20 mA
Power Dissipation (Note 3)	500 mW
Storage Temperature	150°C
ESD Susceptability (Note 11)	2000V

Soldering Information	
N Package: 10 sec.	260°C
J Package: 10 sec.	300°C
SO Package: Vapor Phase (60 sec.)	215°C
Infrared (15 sec.)	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" (Appendix D) for other methods of soldering surface mount devices.

## **Operating Ratings** (Note 1)

Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$
LMF100ACN, LMF100CCN	$0^{\circ}C \le T_{A} \le +70^{\circ}C$
LMF100CCWM	0°C ≤ T <sub>A</sub> ≤ +70°C
LMF100CCJ	$-40^{\circ}C \le T_A \le +85^{\circ}C$
LMF100AJ	$-55^{\circ}C \le T_A \le +125^{\circ}C$
Supply Voltage	$4V \leq V^+ - V^- \leq 15V$

## **Electrical Characteristics**

The following specifications apply for Mode 1, Q = 10 ( $R_1 = R_3 = 100k$ ,  $R_2 = 10k$ ),  $V^+ = +5V$  and  $V^- = -5V$  unless otherwise specified. Boldface limits apply for  $T_{MIN}$  to  $T_{MAX}$ ; all other limits  $T_A = T_J = 25^{\circ}C$ .

Symbol	Parameter		Conditions		LMF100ACN, LMF100CCN, LMF100CCWM			L	Units		
					Typical (Note 8)	Tested Limit (Note 9)	Design Limit (Note 10)	Typical (Note 8)	Tested Limit (Note 9)	Design Limit (Note 10)	
ls	Maximum Supply Curre	nt	f <sub>CLK</sub> = 250 kHz No Input Signal		9	13	13	9	13		mA
fo	Center Frequency	MIN			0.1			0.1			Hz
<u></u>	Range	MAX			100			100			kHz
f <sub>CLK</sub>	Clock Frequency	MIN			5.0			5.0			Hz
	Range	MAX			3.5			3.5			MHz
f <sub>CLK</sub> /f <sub>0</sub>	Clock to Center Frequency Ratio Deviat	tion	V <sub>Pin12</sub> = 5V or 0V	LMF100A	±0.2	±0.6	±0.6	±0.2	± 0.6		%
			f <sub>CLK</sub> = 1 MHz	LMF100C	±0.2	±0.8	± 0.8	±0.2	± 0.8		%
$\frac{\Delta Q}{Q}$	Q Error (MAX) (Note 4)		Q = 10, Mode 1 V <sub>Pin12</sub> = 5V	LMF100A	±0.5	± 4	±5	±0.5	± 5		%
			or 0V f <sub>CLK</sub> = 1 MHz	LMF100C	±0.5	±5	±6	±0.5	±6		%
HOBP	Bandpass Gain at fo		f <sub>CLK</sub> = 1 MHz		0	±0.4	±0.4	0	±0.4		dB
H <sub>OLP</sub>	DC Lowpass Gain $R_1 = R_2 = f_{CLK} = 25$		$R_1 = R_2 = 10k$ $f_{CLK} = 250 \text{ kHz}$		0	±0.2	±0.2	0	± 0.2		dB
V <sub>OS1</sub>	DC Offset Voltage (Not	e 5)	f <sub>CLK</sub> = 250 kHz		± 5.0	±15	± 15	±5.0	± 15		mV
V <sub>OS2</sub>	DC Offset Voltage (Not	e 5)	$f_{CLK} = 250 \text{ kHz}$	$S_{A/B} = V^+$	±30	±80	±80	±30	±80		mV
				$S_{A/B} = V^{-}$	±15	±70	±70	± 15	±70		mV
V <sub>OS3</sub>	DC Offset Voltage (Not	e 5)	f <sub>CLK</sub> = 250 kHz		±15	±40	±60	±15	±60		mV
	Crosstalk (Note 6)		A Side to B Side of B Side to A Side	r	-60			-60			dB
	Output Noise (Note 12)	)	$f_{CLK} = 250 \text{ kHz}$	Ν	40			40			
			20 kHz Bandwidth	BP	320			320			μV
			100:1 Mode	LP	300	L		300			
	Clock Feedthrough (Note 13)		$f_{CLK} = 250 \text{ kHz} 10$	00:1 Mode	6		1	6			mV
VOUT	Minimum OutputRL = 5kVoltage Swing(All Outputs)			+ 4.0 - 4.7	±3.8	± 3.7	+ 4.0 - 4.7	± 3.7		v	
			R <sub>L</sub> = 3.5k (All Outputs)		+3.9 -4.6			+3.9 -4.6			v
GBW	Op Amp Gain BW Prod	luct			5			5			MHz
SR	Op Amp Slew Rate				20			20			V/µs

## **Electrical Characteristics**

The following specifications apply for Mode 1, Q = 10 ( $R_1 = R_3 = 100k$ ,  $R_2 = 10k$ ),  $V^+ = +5V$  and  $V^- = -5V$  unless otherwise specified. Boldface limits apply for  $T_{MIN}$  to  $T_{MAX}$ ; all other limits  $T_A = T_J = 25^{\circ}C$ . (Continued)

Symbol	Parameter	Conditions		MF100AC MF100CC MF100CC	N, N, WM		C1 /1	Ilnits	
	Faraniever		Typical (Note 8)	Tested Limit (Note 9)	Design Limit (Note 10)	Typical (Note 8)	Tested Limit (Note 9)	Design Limit (Note 10)	Units
Isc	Maximum Output Short Source	e (All Outputs)	12			12			mA
Circuit Current (Note 7) Sink	7	45		_	45			mA	
IIN	Input Current on Pins: 4, 5, 6, 9, 10, 11, 12, 16, 17			10			10		μA

## **Electrical Characteristics**

The following specifications apply for Mode 1, Q = 10 (R<sub>1</sub> = R<sub>3</sub> = 100k, R<sub>2</sub> = 10k), V<sup>+</sup> = +2.50V and V<sup>-</sup> = -2.50V unless otherwise specified. Boldface limits apply for T<sub>MIN</sub> to T<sub>MAX</sub>; all other limits T<sub>A</sub> = T<sub>J</sub> = 25°C.

Symbol	Parameter		Conditions			LMF100ACN, LMF100CCN, LMF100CCWM			LMF100AJ LMF100CCJ			
					Typical (Note 8)	Tested Limit (Note 9)	Design Limit (Note 10)	Typical (Note 8)	Tested Limit (Note 9)	Design Limit (Note 10)		
I <sub>S</sub>	Maximum Supply Curre	ent	f <sub>CLK</sub> = 250 kHz No Input Signal		8	12	12	8	12		mA	
fo	Center Frequency	MIN			0.1			0.1			Hz	
	Range	MAX			50			50			kHz	
fclk	Clock Frequency	MIN			5.0			5.0			Hz	
	Hange	MAX			1.5			1.5			MHz	
fCLK/fo	Clock to Center Frequency Ratio Devia	tion	V <sub>Pin12</sub> = 2.5V or 0V	LMF100A	±0.2	±0.6	± 0.8	±0.2	± 0.8		%	
			f <sub>CLK</sub> = 1 MHz	LMF100C	±0.2	± 1	± 1	±0.2	± 1		%	
	Q Error (MAX) (Note 4)		Q = 10, Mode 1 V <sub>Pin12</sub> = 5V	LMF100A	±0.5	±4	±6	±0.5	±6		%	
			or 0V f <sub>CLK</sub> = 1 MHz	LMF100C	±0.5	±5	±8	±0.5	±8		%	
HOBP	Bandpass Gain at f <sub>0</sub>		f <sub>CLK</sub> = 1 MHz		0	±0.4	± 0.5	0	± 0.5		dB	
HOLP	DC Lowpass Gain	C Lowpass Gain $R_1 = R_2 = 10k$ $f_{CLK} = 250 \text{ kHz}$			0	±0.2	± 0.2	0	± 0.2		dB	
V <sub>OS1</sub>	DC Offset Voltage (Not	e 5)	$f_{CLK} = 250  \text{kHz}$		±5.0	±15	± 15	±5.0	± 15		mV	
V <sub>OS2</sub>	DC Offset Voltage (Not	e 5)	$f_{CLK} = 250 \text{ kHz}$	$S_{A/B} = V^+$	±20	±60	±60	±20	±60		mV	
				$S_{A/B} = V^-$	± 10	± 50	±60	±10	±60		mν	
V <sub>OS3</sub>	DC Offset Voltage (Not	e 5)	$f_{CLK} = 250 \text{ kHz}$		±10	±25	± 30	±10	± 30		mV	
	Crosstalk (Note 6)		A Side to B Side of B Side to A Side	r	-65			-65			dB	
	Output Noise (Note 12)		$f_{CLK} = 250 \text{ kHz}$	N	25			25				
			20 kHz Bandwidth	BP	250			250			µν	
			100:1 Mode	LP	220			220				
	Clock Feedthrough (Note 13)		f <sub>CLK</sub> = 250 kHz 10	00:1 Mode	2			2			m∨	
Vout	Minimum Output Voltage Swing		R <sub>L</sub> = 5k (All Outputs)		+ 1.6 -2.2	± 1.5	± 1.4	+ 1.6 - 2.2	± 1.4		v	
			R <sub>L</sub> = 3.5k (All outputs)		+ 1.5 - 2.1			+ 1.5 -2.1			v	
GBW	Op Amp Gain BW Prod	uct			5			5			MHz	
SR	Op Amp Slew Rate				18			18			V/µs	
Isc	Maximum Output Short	Source	(All Outputs)		10			10			mA	
	Circuit Current (Note 7)	Sink			20			20	)		l mA	

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## Logic Input Characteristics Boldface limits apply for $T_{MIN}$ to $T_{MAX}$ ; all other limits $T_A = T_J = 25^{\circ}C$ .

Parameter		Conditions	L L	MF100AC MF100CC MF100CC	:N, :N, WM	LMF100AJ, LMF100CCJ			Units
			Typical (Note 8)	Tested Limit (Note 9)	Design Limit (Note 10)	Typical (Note 8)	Tested Limit (Note 9)	Design Limit (Note 10)	
CMOS Clock	MIN Logical "1"	$V^+ = +5V, V^- = -5V,$		+ 3.0	+ 3.0		+ 3.0		v
Input Voltage	MAX Logical "0"	V <sub>LSh</sub> = 0V		-3.0	-3.0		- 3.0		v
	MIN Logical "1"	$V^+ = +10V, V^- = 0V,$		+ 8.0	+ 8.0		+ 8.0		V
	MAX Logical "0"	$V_{LSh} = +5V$		+ 2.0	+ 2.0		+ 2.0		V
TTL Clock	MIN Logical "1"	$V^+ = +5V, V^- = -5V,$		+ 2.0	+ 2.0		+ 2.0		v
Input Voltage	MAX Logical "0"	V <sub>LSh</sub> = 0V		+ 0.8	+ 0.8		+ 0.8		V
	MIN Logical "1"	$V^+ = +10V, V^- = 0V,$		+ 2.0	+ 2.0		+ 2.0		v
	MAX Logical "0"	V <sub>LSh</sub> = 0V		+ 0.8	+ 0.8		+ 0.8		V
CMOS Clock	MIN Logical "1"	$V^+ = +2.5V, V^- = -2.5V,$		+ 1.5	+ 1.5		+ 1.5		.V
Input Voltage	MAX Logical "0"	$V_{LSh} = 0V$		- 1.5	- 1.5		- 1.5		v
	MIN Logical "1"	$V^+ = +5V, V^- = 0V,$		+4.0	+ 4.0		+ 4.0		v
	MAX Logical "0"	$V_{LSh} = +2.5V$		+ 1.0	+ 1.0		+ 1.0		V
TTL Clock	MIN Logical "1"	$V^+ = +5V, V^- = 0V,$		+ 2.0	+ 2.0		+ 2.0		v
Input Voltage	MAX Logical "0"	$V_{LSh} = 0V, V_D^+ = 0V$		+ 0.8	+ 0.8		+ 0.8		V

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional. These ratings do not guarantee specific performance limits, however. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2: When the input voltage (V<sub>IN</sub>) at any pin exceeds the power supply rails (V<sub>IN</sub> < V<sup>-</sup> or V<sub>IN</sub> > V<sup>+</sup>) the absolute value of current at that pin should be limited to 5 mA or less. The sum of the currents at all pins that are driven beyond the power supply voltages should not exceed 20 mA.

Note 3: The maximum power dissipation must be derated at elevated temperatures and is dictated by  $T_{JMAX}$ ,  $\theta_{JA}$ , and the ambient temperature,  $T_A$ . The maximum allowable power dissipation at any temperature is  $P_D = (T_{JMAX} - T_A)/\theta_{JA}$  or the number given in the Absolute Maximum Ratings, whichever is lower. For this device,  $T_{JMAX} = 125^\circ$ C, and the typical junction-to-ambient thermal resistance of the LMF100ACN/CCN when board mounted is 55°C/W. For the LMF100AJ/CCJ, this number increases to 55°C/W and for the LMF100CWM this number is 66°C/W.

Note 4: The accuracy of the Q value is a function of the center frequency (f<sub>0</sub>). This is illustrated in the curves under the heading "Typical Peformance Characteristics".

Note 5: Vos1, Vos2, and Vos3 refer to the internal offsets as discussed in the Applications Information section 3.4.

Note 6: Crosstalk between the internal filter sections is measured by applying a 1 V<sub>RMS</sub> 10 kHz signal to one bandpass filter section input and grounding the input of the other bandpass filter section. The crosstalk is the ratio between the output of the grounded filter section and the 1 V<sub>RMS</sub> input signal of the other section.

Note 7: The short circuit source current is measured by forcing the output that is being tested to its maximum positive voltage swing and then shorting that output to the negative supply. The short circuit sink current is measured by forcing the output that is being tested to its maximum negative voltage swing and then shorting that output to the positive supply. These are the worst case conditions.

Note 8: Typicals are at 25°C and represent most likely parametric norm.

Note 9: Tested limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

Note 10: Design limits are guaranteed to National's AOQL (Average Outgoing Quality Level) but are not 100% tested.

Note 11: Human body model, 100 pF discharged through a 1.5 k $\Omega$  resistor.

Note 12: In 50:1 mode the output noise is 3 dB higher.

Note 13: In 50:1 mode the clock feedthrough is 6 dB higher.



## Typical Performance Characteristics (Continued)



## LMF100 System Block Diagram

![](_page_6_Figure_1.jpeg)

## **Pin Descriptions**

LP(1,20), BP(2,19), N/AP/HP(3,18)	The second order lowpass, band- pass and notch/allpass/highpass outputs. These outputs can typically swing to within 1V of each supply when driving a 5 k $\Omega$ load. For opti- mum performance, capacitive load- ing on these outputs should be mini- mized For signal frequencies above	S <sub>A/B</sub> (6)
	15 kHz the capacitance loading should be kept below 30 pF.	V <sub>A</sub> +(7)
INV(4,17)	The inverting input of the summing opamp of each filter. These are high impedance inputs. The non-inverting input is internally tied to AGND so the opamp can be used only as an	V <sub>D</sub> +(8)

inverting amplifier. S1(5,16) S1 is a signal input pin used in modes 1b, 4, and 5. The input impedance is  $1/f_{CLK} \times 1$  pF. The pin should be driven with a source impedance of less than 1 k $\Omega$ . If S1 is not driven with a signal it should be tied to AGND (mid-supply).

This pin activates a switch that connects one of the inputs of each filter's second summer either to AGND (S<sub>A/B</sub> tied to V<sup>-</sup>) or to the lowpass (LP) output (S<sub>A/B</sub> tied to V<sup>+</sup>). This offers the flexibility needed for configuring the filter in its various modes of operation.

- +(7)\* This is both the analog and digital positive supply.
  - 3)\* This pin needs to be tied to V<sup>+</sup> except when the device is to operate on a single 5V supply and a TTL level clock is applied. For 5V, TTL operation, V<sub>D</sub><sup>+</sup> should be tied to ground (0V).
- $V_A^-(14), V_D^-(13)$  Analog and digital negative supplies.  $V_A^-$  and  $V_D^-$  should be derived from the same source. They have been brought out separately so they can be bypassed by separate capacitors, if desired. They can also be tied together externally and bypassed with a single capacitor.

## Pin Descriptions (Continued)

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LSh(9)

Level shift pin. This is used to accommodate various clock levels with dual or single supply operation. With dual  $\pm$  5V supplies and CMOS ( $\pm$ 5V) or TTL (0V-5V) clock levels, LSh

should be tied to system ground. For 0V-10V single supply operation the AGND pin should be biased at +5V and the LSh pin should be tied to the system ground for TTL clock levels. LSh should be biased at +5V for  $\pm$ 5V CMOS clock levels.

The LSh pin is tied to system ground for  $\pm 2.5$ V operation. For single 5V operation the LSh and V<sub>D</sub> + pins are tied to system ground for TTL clock levels.

CLK(10,11)

Clock inputs for the two switched capacitor filter sections. Unipolar or bipolar clock levels may be applied to the CLK inputs according to the programming voltage applied to the LSh pin. The duty cycle of the clock should be close to 50%, especially when clock frequencies above 200 kHz are used. This allows the maximum time for the internal opamps to settle, which yields optimum filter performance.

50/100(12)\*

By tying this pin to V<sup>+</sup> a 50:1 clock to filter center frequency ratio is obtained. Tying this pin at mid-supply (i.e., system ground with dual supplies) or to V<sup>-</sup> allows the filter to operate at a 100:1 clock to center frequency ratio.

AGND(15)

quency ratio. This is the analog ground pin. This pin should be connected to the system ground for dual supply operation or biased to mid-supply for single supply operation. For a further discussion of mid-supply biasing techniques see the Applications Information (Section 3.2). For optimum filter performance a "clean" ground must be provided.

\*This device is pin-for-pin compatible with the MF10 except for the following changes:

1. Unlike the MF10, the LMF100 has a single positive supply pin (V<sub>A</sub>+).

2. On the LMF100  $V_{\rm D}^+$  is a control pin and is not the digital positive supply as on the MF10.

3. Unlike the MF10, the LMF100 does not support the current limiting mode. When the 50/100 pin is tied to V- the LMF100 will remain in the 100:1 mode.

## 1.0 Definitions of Terms

 $f_{\mbox{CLK}}$  the frequency of the external clock signal applied to pin 10 or 11.

 $f_0$ : center frequency of the second order function complex pole pair.  $f_0$  is measured at the bandpass outputs of the LMF100, and is the frequency of maximum bandpass gain. *(Figure 1).* 

fnotch: the frequency of minimum (ideally zero) gain at the notch outputs.

 $f_2$ : the center frequency of the second order complex zero pair, if any. If  $f_2$  is different from  $f_0$  and if  $Q_2$  is high, it can be observed as the frequency of a notch at the allpass output. *(Figure 13).* 

**Q:** "quality factor" of the 2nd order filter. Q is measured at the bandpass outputs of the LMF100 and is equal to  $f_0$  divided by the -3 dB bandwidth of the 2nd order bandpass filter (*Figure 1*). The value of Q determines the shape of the 2nd order filter responses as shown in *Figure 6*.

 $\mathbf{Q}_{z}$ : the quality factor of the second order complex zero pair, if any.  $\mathbf{Q}_{Z}$  is related to the allpass characteristic, which is written:

$$H_{AP}(s) = \frac{H_{OAP}\left(s^2 - \frac{s\omega_0}{Q_z} + \omega_0^2\right)}{s^2 + \frac{s\omega_0}{Q} + \omega_0^2}$$

where  $Q_Z = Q$  for an all-pass response.

**HOBP:** the gain (in V/V) of the bandpass output at  $f = f_0$ . **HOLP:** the gain (in V/V) of the lowpass output as  $f \rightarrow 0$  Hz (*Figure 2*).

**HOHP:** the gain (in V/V) of the highpass output as  $f \rightarrow f_{CLK}/2$  (*Figure 3*).

**HON:** the gain (in V/V) of the notch output as  $f \rightarrow 0$  Hz and as  $f \rightarrow f_{CLK}/2$ , when the notch filter has equal gain above and below the center frequency (*Figure 4*). When the low-frequency gain differs from the high-frequency gain, as in modes 2 and 3a (*Figures 10* and *12*), the two quantities below are used in place of H<sub>ON</sub>.

**H**<sub>ON1</sub>: the gain (in V/V) of the notch output as  $f \rightarrow 0$  Hz. **H**<sub>ON2</sub>: the gain (in V/V) of the notch output as  $f \rightarrow f_{CLK}/2$ .

![](_page_8_Figure_0.jpeg)

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![](_page_9_Figure_1.jpeg)

## 2.0 Modes of Operation

The LMF100 is a switched capacitor (sampled data) filter. To fully describe its transfer functions, a time domain analysis is appropriate. Since this is cumbersome, and since the LMF100 closely approximates continuous filters, the following discussion is based on the well-known frequency domain. Each LMF100 can produce two full 2nd order functions. See Table I for a summary of the characteristics of the various modes.

#### MODE 1: Notch 1, Bandpass, Lowpass Outputs:

 $f_{notch} = f_0$  (See Figure 7)

- $f_0$  = center frequency of the complex pole pair
  - $=\frac{f_{CLK}}{100} \text{ or } \frac{f_{CLK}}{50}$

 $f_{notch}$  = center frequency of the imaginary zero pair =  $f_0$ .

 $H_{OLP}$  = Lowpass gain (as f  $\rightarrow$  0) =  $-\frac{R2}{R1}$  $H_{OBP}$  = Bandpass gain (at f = f<sub>0</sub>) =  $-\frac{R3}{R1}$ 

$$H_{ON} = \text{Notch output gain as } f \rightarrow 0 \\ f \rightarrow f_{CLK/2} = \frac{-R_2}{R_1}$$

$$Q = \frac{f_0}{BW} = \frac{Ha}{Ra}$$

= quality factor of the complex pole pair

BW = the -3 dB bandwidth of the bandpass output.

Circuit dynamics:

$$\begin{aligned} \mathsf{H}_{\mathsf{OLP}} &= \frac{\mathsf{H}_{\mathsf{OBP}}}{\mathsf{Q}} \, \mathsf{or} \, \mathsf{H}_{\mathsf{OBP}} = \mathsf{H}_{\mathsf{OLP}} \times \mathsf{Q} \\ &= \mathsf{H}_{\mathsf{ON}} \times \mathsf{Q}. \end{aligned}$$

 $H_{OLP(peak)} \cong Q \times H_{OLP}$  (for high Q's) MODE 1a: Non-Inverting BP, LP (See *Figure 8*)

$$f_0 = \frac{f_{CLK}}{100} \text{ or } \frac{f_{CLK}}{50}$$
$$Q = \frac{R3}{R2}$$

 $H_{OLP} = -1; H_{OLP(peak)} \cong Q \times H_{OLP}$  (for high Q's)

$$H_{OBP_1} = -\frac{R3}{R2}$$

 $H_{OBP_2} = 1$  (non-inverting)

Circuit dynamics:  $H_{OBP_1} = Q$ Note:  $V_{IN}$  should be driven from a low impedance (<1 k $\Omega$ ) source.

![](_page_10_Figure_20.jpeg)

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### 2.0 Modes of Operation (Continued) MODE 1b: Notch 1, Bandpass, Lowpass Outputs: $f_{notch} = f_0$ (See Figure 9) = center frequency of the complex pole pair fo $=\frac{f_{CLK}}{100}\times\sqrt{2} \text{ or } \frac{f_{CLK}}{50}\times\sqrt{2}$ $f_{notch}$ = center frequency of the imaginary zero pair = $f_0$ . $H_{OLP}$ = Lowpass gain (as f $\rightarrow$ 0) = $-\frac{R2}{2R1}$ $H_{OBP}$ = Bandpass gain (at f = f\_0) = $-\frac{R3}{R1}$ = Notch output gain as $f \rightarrow 0$ $f \rightarrow f_{CLK}/2 = \frac{-R_2}{R_1}$ HON $=\frac{f_0}{BW}=\frac{R3}{R2}\times\sqrt{2}$ Q = quality factor of the complex pole pair = the -3 dB bandwidth of the bandpass output. ВW Circuit dynamics: $= \frac{H_{OBP}}{\sqrt{2} Q} \text{ or } H_{OBP} = H_{OLP} \times Q \times \sqrt{2}$ HOLP $=\frac{H_{ON} \times Q}{\sqrt{2}}$ HOBP $H_{OLP(peak)} \cong Q \times H_{OLP}$ (for high Q's)

MODE 2: Notch 2, Bandpass, Lowpass: f<sub>notch</sub> < f<sub>0</sub> (See *Figure 10*)

= center frequency  
= 
$$\frac{f_{CLK}}{100} \sqrt{\frac{R2}{R4} + 1}$$
 or  $\frac{f_{CLK}}{50} \sqrt{\frac{R2}{R4} + 1}$ 

$$f_{notch} = \frac{f_{CLK}}{100} \text{ or } \frac{f_{CLK}}{50}$$

fo

Q = quality factor of the complex pole pair  
= 
$$\frac{\sqrt{R2/R4 + 1}}{R2/R3}$$

$$H_{OLP} = \text{Lowpass output gain (as f \rightarrow 0)}$$
$$= -\frac{R2/R1}{R2/R4 + 1}$$

$$H_{OBP}$$
 = Bandpass output gain (at f = f<sub>0</sub>) = - R3/R1

$$H_{ON_1} = \text{Notch output gain (as f \rightarrow 0)}$$
$$= -\frac{R2/R1}{R2/R4 + 1}$$

$$H_{ON_2}$$
 = Notch output gain  $\left(as f \rightarrow \frac{f_{CLK}}{2}\right) = -R2/R1$   
Filter dynamics:  $H_{OBP} = Q\sqrt{H_{OLP}H_{ON_2}} = \sqrt{H_{ON_1}H_{ON_2}}$ 

![](_page_11_Figure_10.jpeg)

![](_page_11_Figure_11.jpeg)

 $R^{A}$   $R^{A$ 

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![](_page_11_Figure_14.jpeg)

![](_page_12_Figure_0.jpeg)

#### 2.0 Modes of Operation (Continued) MODE 4: Allpass, Bandpass, Lowpass Outputs

(See Figure 13)

 $\begin{array}{ll} H_{OBP} & = \text{ Bandpass gain (at f = f_0)} \\ & = -\frac{R3}{R2} \left(1 + \frac{R2}{R1}\right) = -2 \left(\frac{R3}{R2}\right) \end{array}$ 

Circuit dynamics:  $H_{OBP} = (H_{OLP}) \times Q = (H_{OAP} + 1)Q$ \*Due to the sampled data nature of the filter, a slight mismatch of  $f_z$  and  $f_0$  occurs causing a 0.4 dB peaking around  $f_0$  of the allpass filter amplitude response (which theoretically should be a straight line). If this is unacceptable, Mode 5 is recommended.

![](_page_13_Figure_7.jpeg)

![](_page_13_Figure_8.jpeg)

VIN  $H_{A}$   $R_{A}$   $R_{A}$  $R_{A}$ 

#### FIGURE 14. MODE 5

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![](_page_14_Figure_0.jpeg)

![](_page_15_Figure_0.jpeg)

## 2.0 Modes of Operation (Continued)

TABLE I. Summary of Modes. Realizable filter types (e.g. low-pass) denoted by asterisks. Unless otherwise noted, gains of various filter outputs are inverting and adjustable by resistor ratios.

Mode	BP	LP	HP	N	АР	Number of Resistors	Adjustable f <sub>CLK</sub> /f <sub>0</sub>	Notes
1	*	*		*		3	No	
1a	(2) $H_{OBP1} = -Q$ $H_{OBP2} = +1$	$H_{OLP} = + 1$				2	No	May need input buf- fer. Poor dynamics for high Q.
1b	*	*		*		3	No	Useful for high frequency applications.
2	•	*		*		3	Yes (above f <sub>CLK</sub> /50 or f <sub>CLK</sub> /100)	
3	*	*	*			4	Yes	Universal State- Variable Filter. Best general-purpose mode.
За	*		*	*		7	Yes	As above, but also includes resistor- tuneable notch.
4	*	*			*	3	No	Gives Allpass response with $H_{OAP} = -1$ and $H_{OLP} = -2$ .
5	*	*			*	4	Yes	Gives flatter allpass response than above if $R_1 = R_2 = 0.02R_4$ .
6a		*	*			3	Yes	Single pole.
6b		(2) $H_{OLP1} = + 1$ $H_{OLP2} = \frac{-R3}{R2}$				2	Yes	Single pole.
6c		*			*	3	No	Single pole.
7						2	Yes	Summing integrator with adjustable time constant.

## **3.0 Applications Information**

The LMF100 is a general purpose dual second-order state variable filter whose center frequency is proportional to the frequency of the square wave applied to the clock input ( $f_{CLK}$ ). The various clocking options are summarized in the following table.

Power Supply	Clock Levels	LSh	V <sub>D</sub> +				
-5V and +5V -5V and +5V	TTL (0V to +5V) CMOS (-5V to +5V)	0V 0V	+ 5V + 5V				
0V and 10V 0V and 10V	TTL (0V to 5V) CMOS (0V to + 10V)	0V + 5V	+ 10V + 10V				
-2.5V and +2.5V	CMOS (-2.5V to +2.5V)	ov	+ 2.5V				
0V and 5V	TTL (0V to +5V)	ov	0V				
0V and 5V	CMOS (0V to +5V)	+ 2.5V	+5V				

**Clocking Options** 

By connecting pin 12 to the appropriate dc voltage, the filter center frequency,  $f_0$ , can be made equal to either  $f_{CLK}/100$  or  $f_{CLK}/50$ .  $f_0$  can be very accurately set (within  $\pm 0.6\%$ ) by using a crystal clock oscillator, or can be easily varied over a wide frequency range by adjusting the clock frequency. If desired, the  $f_{CLK}/f_0$  ratio can be altered by external resistors as in *Figures 10, 11, 12, 13, 14, 15* and *16*. This is useful when high-order filters (greater than two) are to be realized by cascading the second-order sections. This allows each stage to be stagger tuned while using only one clock. The filter Q and gain are set by external resistor ratios.

All of the five second-order filter types can be built using either section of the LMF100. These are illustrated in *Figures 1* through 5 along with their transfer functions and some related equations. *Figure 6* shows the effect of Q on the shapes of these curves.

## 3.0 Applications Information (Continued)

#### 3.1 DESIGN EXAMPLE

In order to design a filter using the LMF100, we must define the necessary values of three parameters for each secondorder section:  $f_0$ , the filter section's center frequency;  $H_0$ , the passband gain; and the filter's Q. These are determined by the characteristics required of the filter being designed.

As an example, let's assume that a system requires a fourth-order Chebyshev low-pass filter with 1 dB ripple, unity gain at dc, and 1000 Hz cutoff frequency. As the system order is four, it is realizable using both second-order sections of an LMF100. Many filter design texts (and National's Switched Capacitor Filter Handbook) include tables that list the characteristics ( $f_0$  and Q) of each of the second-order filter sections needed to synthesize a given higher-order filter. For the Chebyshev filter defined above, such a table yields the following characteristics:

For unity gain at dc, we also specify:

 $H_{0A} = 1$ 

 $H_{0B} = 1$ 

The desired clock-to-cutoff-frequency ratio for the overall filter of this example is 100 and a 100 kHz clock signal is available. Note that the required center frequencies for the two second-order sections will not be obtainable with clock-to-center-frequency ratios of 50 or 100. It will be necessary

to adjust  $\frac{f_{CLK}}{f_0}$  externally. From Table I, we see that Mode 3

can be used to produce a low-pass filter with resistor-adjustable center frequency. In most filter designs involving multiple second-order stages, it is best to place the stages with lower Q values ahead of stages with higher Q, especially when the higher Q is greater than 0.707. This is due to the higher relative gain at the center frequency of a higher-Q stage. Placing a stage with lower Q ahead of a higher-Q stage will provide some attenuation at the center frequency and thus help avoid clipping of signals near this frequency. For this example, stage A has the lower Q (0.785) so it will be placed ahead of the other stage.

For the first section, we begin the design by choosing a convenient value for the input resistance:  $R_{1A} = 20k$ . The absolute value of the passband gain  $H_{OLPA}$  is made equal to 1 by choosing  $R_{4A}$  such that:  $R_{4A} = -H_{OLPA}R_{1A} = R_{1A} = 20k$ . If the 50/100/CL pin is connected to mid-supply for nominal 100:1 clock-to-center-frequency ratio, we find  $R_{2A}$  by:

$$R_{2A} = R_{4A} \frac{f_{0A}^2}{(f_{CLK}/100)^2} = 2 \times 10^4 \times \frac{(529)^2}{(1000)^2} = 5.6k \text{ and}$$

 $R_{3A}=Q_A\sqrt{R_{2A}R_{4A}}=0.785\sqrt{5.6\times10^3\times2\times10^4}=8.3k$  The resistors for the second section are found in a similar fashion:

$$R_{1B} = 20k$$

$$\mathsf{R}_{4\mathsf{B}} = \mathsf{R}_{1\mathsf{B}} = 20\mathsf{k}$$

$$R_{2B} = R_{4B} \frac{f_{0B}^2}{(f_{CLK}/100)^2} = 20k \frac{(993)^2}{(1000)^2} = 19.7k$$

 $\begin{array}{l} \mathsf{R}_{3B} = \mathsf{Q}_{B} \sqrt{\mathsf{R}_{2B} \mathsf{R}_{4B}} = 3.559 \sqrt{1.97 \times 10^4 \times 2 \times 10^4} = 70.6 \mathsf{k} \\ \text{The complete circuit is shown in Figure 19 for split } \pm 5 \mathsf{V} \\ \text{power supplies. Supply bypass capacitors are highly recommended.} \end{array}$ 

![](_page_17_Figure_20.jpeg)

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![](_page_17_Figure_22.jpeg)

![](_page_18_Figure_0.jpeg)

## 3.0 Applications Information (Continued) 3.2 SINGLE SUPPLY OPERATION

The LMF100 can also operate with a single-ended power supply. Figure 20 shows the example filter with a single-ended power supply.  $V_A^+$  and  $V_D^+$  are again connected to the positive power supply (4 to 15 volts), and  $V_A^-$  and  $V_D^-$  are connected to ground. The AGND pin must be tied to V+/2 for single supply operation. This half-supply point should be very "clean", as any noise appearing on it will be treated as an input to the filter. It can be derived from the supply voltage with a pair of resistors and a bypass capacitor (Figure 21a), or a low-impedance half-supply voltage can be made using a three-terminal voltage regulator or an operational amplifier (Figures 21b and 21c). The passive resistor divider with a bypass capacitor is sufficient for many applications. provided that the time constant is long enough to reject any power supply noise. It is also important that the half-supply reference present a low impedance to the clock frequency, so at very low clock frequencies the regulator or op-amp approaches may be preferable because they will require smaller capacitors to filter the clock frequency. The main power supply voltage should be clean (preferably regulated) and bypassed with 0.1 µF.

#### 3.3 DYNAMIC CONSIDERATIONS

The maximum signal handling capability of the LMF100, like that of any active filter, is limited by the power supply voltages used. The amplifiers in the LMF100 are able to swing to within about 1 volt of the supplies, so the input signals must be kept small enough that none of the outputs will exceed these limits. If the LMF100 is operating on  $\pm 5$  volts, for example, the outputs will clip at about  $8V_{p-p}$ . The maximum input voltage multiplied by the filter gain should therefore be less than  $8V_{p-p}$ .

Note that if the filter Q is high, the gain at the lowpass or highpass outputs will be much greater than the nominal filter gain (*Figure 6*). As an example, a lowpass filter with a Q of 10 will have a 20 dB peak in its amplitude response at f<sub>0</sub>. If the nominal gain of the filter (H<sub>OLP</sub>) is equal to 1, the gain at f<sub>0</sub> will be 10. The maximum input signal at f<sub>0</sub> must therefore be less than 800 mV<sub>p-p</sub> when the circuit is operated on  $\pm 5$  volt supplies.

Also note that one output can have a reasonable small voltage on it while another is saturated. This is most likely for a circuit such as the notch in Mode 1 (*Figure 7*). The notch output will be very small at  $f_0$ , so it might appear safe to apply a large signal to the input. However, the bandpass will have its maximum gain at  $f_0$  and can clip if overdriven. If one output clips, the performance at the other outputs will be degraded, so avoid overdriving any filter section, even ones whose outputs are not being directly used. Accompanying *Figures 7* through *17* are equations labeled "circuit dynamics", which relate the Q and the gains at the various outputs. These should be consulted to determine peak circuit gains and maximum allowable signals for a given application.

#### 3.4 OFFSET VOLTAGE

The LMF100's switched capacitor integrators have a slightly higher input offset voltage than found in a typical continuous time active filter integrator. Because of National's new LMCMOS process and new design techniques the internal offsets have been minimized, compared to the industry standard MF10. *Figure 22* shows an equivalent circuit of the LMF100 from which the output dc offsets can be calculated.

Typical values for these offsets with  $S_{\mbox{A/B}}$  tied to V+ are:

$$V_{OS1} = opamp offset = \pm 5 \text{ mV}$$

 $V_{OS2} = \pm 30 \text{ mV} \text{ at } 50:1 \text{ or } 100:1$ 

 $V_{OS3} = \pm 15 \text{ mV} \text{ at 50:1 or 100:1}$ 

When  $S_{A/B}$  is tied to V<sup>-</sup>, V<sub>OS2</sub> will approximately halve. The dc offset at the BP output is equal to the input offset of the lowpass integrator (V<sub>OS3</sub>). The offsets at the other outputs depend on the mode of operation and the resistor ratios, as described in the following expressions.

#### Mode 1 and Mode 4

Vos(N)	$= V_{OS1} \left( \frac{1}{Q} + 1 + \left\  H_{OLP} \right\  \right) - \frac{V_{OS3}}{Q}$
V <sub>OS(BP)</sub>	= V <sub>OS3</sub>
VOS(LP)	$= V_{OS(N)} - V_{OS2}$
Mode 1a	
V <sub>OS</sub> (N.INV.BP)	$= \left(1 + \frac{1}{Q}\right) V_{OS1} - \frac{V_{OS3}}{Q}$
V <sub>OS</sub> (INV.BP) V <sub>OS</sub> (LP)	$= V_{OS3}$ = V_{OS}(N.INV.BP) - V_{OS2}
Mode 1b	
Vos(N)	$= V_{OS1} \left( 1 + \frac{R2}{R3} + \frac{R2}{R1} \right) - \frac{R2}{R3} V_{OS3}$
V <sub>OS(BP)</sub>	= V <sub>OS3</sub>
V <sub>OS(LP)</sub>	$=\frac{V_{OS(N)}}{2}-\frac{V_{OS2}}{2}$
Mode 2 and Mo	ode 5
V <sub>OS(N)</sub>	$= \left(\frac{R2}{Rp} + 1\right) V_{OS1} \times \frac{1}{1 + R2/R4}$
	+ $V_{OS2} \frac{1}{1 + R4/R2} - \frac{V_{OS3}}{Q\sqrt{1 + R2/R4}}$ : R <sub>p</sub> = R1  R3  R4
V <sub>OS(BP)</sub>	= V <sub>OS3</sub>
V <sub>OS(LP)</sub>	= V <sub>OS(N)</sub> $-$ V <sub>OS2</sub>
Mode 3	
V <sub>OS(HP)</sub>	=V <sub>OS2</sub>
V <sub>OS(BP)</sub>	$=V_{OS3}$
V <sub>OS(LP)</sub>	$= V_{OS1} \left[ 1 + \frac{H4}{R_p} \right] - V_{OS2} \left( \frac{H4}{R2} \right)$
	$- V_{OS3} \left( \frac{R4}{R3} \right)$
	$R_{p} = R1   R2  R3$
Mode 6a and 6	c
V <sub>OS(HP)</sub>	= V <sub>OS2</sub>
V <sub>OS(LP)</sub>	$= V_{OS1} \left( 1 + \frac{R_3}{R_2} + \frac{R_3}{R_1} \right) - \frac{R_3}{R_2} V_{OS2}$
Mode 6b	
VOS(LP (N.INV))	= V <sub>OS2</sub>
V <sub>OS(LP (INV))</sub>	$= V_{OS1} \left( 1 + \frac{R_3}{R_2} \right) - \frac{R_3}{R_2} V_{OS2}$

![](_page_20_Figure_0.jpeg)

FIGURE 22. Offset Voltage Sources

In many applications, the outputs are ac coupled and dc offsets are not bothersome unless large signals are applied to the filter input. However, larger offset voltages will cause clipping to occur at lower ac signal levels, and clipping at any of the outputs will cause gain nonlinearities and will change fo and Q. When operating in Mode 3, offsets can become excessively large if R2 and R4 are used to make f<sub>CLK</sub>/f<sub>0</sub> significantly higher than the nominal value, especially if Q is also high.

For example, Figure 23 shows a second-order 60 Hz notch filter. This circuit yields a notch with about 40 dB of attenuation at 60 Hz. A notch is formed by subtracting the bandpass output of a mode 3 configuration from the input using

the unused side B opamp. The Q is 10 and the gain is 1 V/V in the passband. However,  $f_{CLK}/f_0 = 1000$  to allow for a wide input spectrum. This means that for pin 12 tied to ground (100:1 mode), R4/R2 = 100. The offset voltage at the lowpass output (LP) will be about 3V. However, this is an extreme case and the resistor ratio is usually much smaller. Where necessary, the offset voltage can be adjusted by using the circuit of Figure 24. This allows adjustment of VOS1, which will have varying effects on the different outputs as described in the above equations. Some outputs cannot be adjusted this way in some modes, however (VOS(BP) in modes 1a and 3, for example).

![](_page_20_Figure_6.jpeg)

FIGURE 23. Second-Order Notch Filter

#### 3.0 Applications Information (Continued)

![](_page_21_Figure_2.jpeg)

FIGURE 24. Method for Trimming VOS

#### 3.5 SAMPLED DATA SYSTEM CONSIDERATIONS

The LMF100 is a sampled data filter, and as such, differs in many ways from conventional continuous-time filters. An important characteristic of sampled-data systems is their effect on signals at frequencies greater than one-half the sampling frequency. (The LMF100's sampling frequency is the same as its clock frequency.) If a signal with a frequency greater than one-half the sampling frequency is applied to the input of a sampled data system, it will be "reflected" to a frequency less than one-half the sampling frequency. Thus, an input signal whose frequency is  $f_s/2 + 100$  Hz will cause the system to respond as though the input frequency was f<sub>s</sub>/2 - 100 Hz. This phenomenon is known as "aliasing", and can be reduced or eliminated by limiting the input signal spectrum to less than fs/2. This may in some cases require the use of a bandwidth-limiting filter ahead of the LMF100 to limit the input spectrum. However, since the clock frequency is much higher than the center frequency, this will often not be necessary.

Another characteristic of sampled-data circuits is that the output signal changes amplitude once every sampling period, resulting in "steps" in the output voltage which occur at the clock rate (*Figure 25*). If necessary, these can be "smoothed" with a simple R-C low-pass filter at the LMF100 output.

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The ratio of  $f_{CLK}$  to  $f_c$  (normally either 50:1 or 100:1) will also affect performance. A ratio of 100:1 will reduce any aliasing problems and is usually recommended for wideband input signals. In noise-sensitive applications, a ratio of 100:1 will result in 3 dB lower output noise for the same filter configuration.

The accuracy of the f<sub>CLK</sub>/f<sub>0</sub> ratio is dependent on the value of Q. This is illustrated in the curves under the heading "Typical Performance Characteristics". As Q is changed, the true value of the ratio changes as well. Unless the Q is low, the error in f<sub>CLK</sub>/f<sub>0</sub> will be small. If the error is too large for a specific application, use a mode that allows adjustment of the ratio with external resistors.

![](_page_21_Figure_9.jpeg)

FIGURE 25. The Sampled-Data Output Waveform