LMH6601/LMH6601Q 250 MHz, 2.4V CMOS Operational Amplifier with Shutdown

Check for Samples: LMH6601

FEATURES

- V_S = 3.3V, T_A = 25°C, A_V = 2 V/V, R_L = 150Ω to V^-, unless specified.
- 125 MHz −3 dB small signal bandwidth
- 75 MHz −3 dB large signal bandwidth
- 30 MHz large signal 0.1 dB gain flatness
- 260 V/μs slew rate
- 0.25%/0.25° differential gain/differential phase
- Rail-to-rail output
- 2.4V – 5.5V single supply operating range
- 6-Pin SC70 Package
- LMH6601Q is AEC-Q100 grade 3 qualified and is manufactured on an automotive grade flow

APPLICATIONS

- Video amplifier
- Charge amplifier
- Set-top box
- Sample & hold
- Transimpedance amplifier
- Line driver
- High impedance buffer
- Automotive

DESCRIPTION

The LMH6601 is a low voltage (2.4V – 5.5V), high speed voltage feedback operational amplifier suitable for use in a variety of consumer and industrial applications. With a bandwidth of 125 MHz at a gain of +2 and guaranteed high output current of 100 mA, the LMH6601 is an ideal choice for video line driver applications including HDTV. Low input bias current (50 pA maximum), rail-to-rail output, and low current noise allow the LMH6601 to be used in various industrial applications such as transimpedance amplifiers, active filters, or high-impedance buffers. The LMH6601 is an attractive solution for systems which require high performance at low supply voltages. The LMH6601 is available in a 6-pin SC70 package, and includes a micropower shutdown feature.

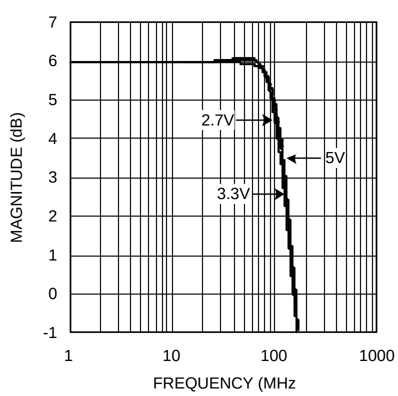


Figure 1. Response at a Gain of +2 for Various Supply Voltages

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1)

ESD Tolerance (2)	
Human Body Model	2 kV
Machine Model	200V
V_{IN} Differential	±2.5V
Input Current (3)	±10 mA
Output Current	200 mA (4)
Supply Voltage (V^+ – $V^−$)	6.0V
Voltage at Input/Output Pins	V^++0.5V, $V^−$−0.5V
Storage Temperature Range	−65°C to +150°C
Junction Temperature	+150°C
Soldering Information	
Infrared or Convection (20 sec.)	235°C
Wave Soldering (10 sec.)	260°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics.
(2) Human Body Model, applicable std. MIL-STD-883, Method 3015.7. Machine Model, applicable std. JESD22-A115-A (ESD MM std. of JEDEC)Field-Induced Charge-Device Model, applicable std. JESD22-C101-C (ESD FICDM std. of JEDEC).
(3) Negative input current implies current flowing out of the device.
(4) The maximum continuous output current (I_{OUT}) is determined by device power dissipation limitations.

Operating Ratings (1)

Supply Voltage (V^+ – $V^−$)	2.4V to 5.5V
Operating Temperature Range	−40°C to +85°C
Package Thermal Resistance (θ_{JA})	
6-pin SC70	414°C/W

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics.

5V Electrical Characteristics

Single Supply with V_S= 5V, A_V = +2, R_F = 604Ω, $\overline{SD}$ tied to V^+, V_{OUT} = V_S/2, R_L = 150Ω to V^- unless otherwise specified. **Boldface** limits apply at temperature extremes. (1)

Symbol	Parameter	Condition	Min (2)	Typ (2)	Max (2)	Units
Frequency Domain Response						
SSBW	–3 dB Bandwidth Small Signal	V_{OUT} = 0.25 V_{PP}		130		MHz
SSBW_1		V_{OUT} = 0.25 V_{PP}, A_V = +1		250		
Peak	Peaking	V_{OUT} = 0.25 V_{PP}, A_V = +1		2.5		dB
Peak_1	Peaking	V_{OUT} = 0.25 V_{PP}		0		dB
LSBW	–3 dB Bandwidth Large Signal	V_{OUT} = 2 V_{PP}		81		MHz
Peak_2	Peaking	V_{OUT} = 2 V_{PP}		0		dB
0.1 dB BW	0.1 dB Bandwidth	V_{OUT} = 2 V_{PP}		30		MHz
GBWP_1k	Gain Bandwidth Product	Unity Gain, R_L = 1 kΩ to V_S/2		155		MHz
GBWP_150		Unity Gain, R_L = 150Ω to V_S/2		125		
A_{VOL}	Large Signal Open Loop Gain	0.5V < V_{OUT} < 4.5V	56	66		dB
PBW	Full Power BW	–1 dB, A_V = +4, V_{OUT} = 4.2 V_{PP}, R_L = 150Ω to V_S/2		30		MHz
DG	Differential Gain	4.43 MHz, 1.7V ≤ V_{OUT} ≤ 3.3V, R_L = 150Ω to V^-		0.06		%
DP	Differential Phase	4.43 MHz, 1.7V ≤ V_{OUT} ≤ 3.3V R_L = 150Ω to V^-		0.10		deg
Time Domain Response						
TRS/TRL	Rise & Fall Time	0.25V Step		2.6		ns
OS	Overshoot	0.25V Step		10		%
SR	Slew Rate	2V Step		275		V/μs
T_S	Settling Time	1V Step, ±0.1%		50		ns
T_{S_1}		1V Step, ±0.02%		220		
PD	Propagation Delay	Input to Output, 250 mV Step, 50%		2.4		ns
C_L	Cap Load Tolerance	A_V = −1, 10% Overshoot, 75Ω in Series		50		pF
Distortion & Noise Performance						
HD2	Harmonic Distortion (2nd)	2 V_{PP}, 10 MHz		−56		dBc
HD2_1		4 V_{PP}, 10 MHz, R_L = 1 kΩ to V_S/2		−61		
HD3	Harmonic Distortion (3rd)	2 V_{PP}, 10 MHz		−73		dBc
HD3_1		4 V_{PP}, 10 MHz, R_L = 1 kΩ to V_S/2		−64		
THD	Total Harmonic Distortion	4 V_{PP}, 10 MHz, R_L = 1 kΩ to V_S/2		−58		
V_{N1}	Input Voltage Noise	>10 MHz		7		$nV/\sqrt{Hz}$
V_{N2}		1 MHz		10		
I_N	Input Current Noise	>1 MHz		50		$fA/\sqrt{Hz}$
Static, DC Performance						
V_{IO}	Input Offset Voltage			±1	±2.4 **±5.0**	mV
DV_{IO}	Input Offset Voltage Average Drift	(3)		−5		μV/°C
I_B	Input Bias Current	(4)		5	50	pA
I_{OS}	Input Offset Current	(4)		2	25	pA

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that $T_J = T_A$. No guarantee of parametric performance is indicated in the electrical tables under conditions of internal self-heating where $T_J > T_A$.
(2) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not guaranteed on shipped production material.
(3) Drift determined by dividing the change in parameter at temperature extremes by the total temperature change.
(4) This parameter is guaranteed by design and/or characterization and is not tested in production.

5V Electrical Characteristics (continued)

Single Supply with V_S= 5V, A_V = +2, R_F = 604Ω, $\overline{SD}$ tied to V^+, V_{OUT} = V_S/2, R_L = 150Ω to V^- unless otherwise specified. **Boldface** limits apply at temperature extremes. (1)

Symbol	Parameter	Condition	Min (2)	Typ (2)	Max (2)	Units
R_{IN}	Input Resistance	0V ≤ V_{IN} ≤ 3.5V		10		TΩ
C_{IN}	Input Capacitance			1.3		pF
+PSRR	Positive Power Supply Rejection Ratio	DC	55 **51**	59		dB
−PSRR	Negative Power Supply Rejection Ratio	DC	53 **50**	61		dB
CMRR	Common Mode Rejection Ratio	DC	56 **53**	68		dB
CMVR	Input Voltage Range	CMRR > 50 dB	**V^- -0.20**	–	**V^+ - 1.5**	V
I_{CC}	Supply Current	Normal Operation V_{OUT} = V_S/2		9.6	11.5 **13.5**	mA
		Shutdown $\overline{SD}$ tied to ≤ 0.5V (5)		100		nA
VOH1	Output High Voltage (Relative to V^+)	R_L = 150Ω to V^-	–210 **–480**	–190		mV
VOH2		R_L = 75Ω to V_S/2		–190		mV
VOH3		R_L = 10 kΩ to V^-	–60 **–110**	–12		mV
VOL1	Output Low Voltage (Relative to V^-)	R_L = 150Ω to V^-		+5	+45 **+125**	mV
VOL2		R_L = 75Ω to V_S/2		+120		mV
VOL3		R_L = 10 kΩ to V^-		+5	+45 **+125**	mV
I_O	Output Current	V_{OUT} < 0.6V from Respective Supply — Source		150		mA
		V_{OUT} < 0.6V from Respective Supply — Sink		180		mA
I_O_1		V_{OUT} = V_S/2, V_{ID} = ±18 mV (6)	±100			mA
Load	Output Load Rating	THD < −30 dBc, f = 200 kHz, R_L tied to V_S/2, V_{OUT} = 4 V_{PP}		20		Ω
R_O_Enabled	Output Resistance	Enabled, A_V = +1		0.2		Ω
R_O_Disabled	Output Resistance	Shutdown		>100		MΩ
C_O_Disabled	Output Capacitance	Shutdown		5.0		pF
Miscellaneous Performance						
VDMAX	Voltage Limit for Disable (Pin 5)	(5)	**0**		**0.5**	V
VDMIN	Voltage Limit for Enable (Pin 5)	(5)	**4.5**		**5.0**	V
I_i	Logic Input Current (Pin 5)	$\overline{SD}$ = 5V (5)		10		pA
$V_{\_glitch}$	Turn-on Glitch			2.2		V
T_{on}	Turn-on Time			1.4		µs
T_{off}	Turn-off Time			520		ns
$Isolation_{OFF}$	Off Isolation	1 MHz, R_L = 1 kΩ		60		dB
T_OL	Overload Recovery			<20		ns

(5) $\overline{SD}$ logic is CMOS compatible. To ensure proper logic level and to minimize power supply current, $\overline{SD}$ should typically be less than 10% of total supply voltage away from either supply rail.
(6) "V_{ID}" is input differential voltage (input overdrive).

3.3V Electrical Characteristics

Single Supply with V_S= 3.3V, A_V = +2, R_F = 604Ω, $\overline{SD}$ tied to V^+, V_{OUT} = V_S/2, R_L = 150Ω to V^- unless otherwise specified. **Boldface** limits apply at temperature extremes. (1)

Symbol	Parameter	Condition	Min (2)	Typ (2)	Max (2)	Units
Frequency Domain Response						
SSBW	–3 dB Bandwidth Small Signal	V_{OUT} = 0.25 V_{PP}		125		MHz
SSBW_1		V_{OUT} = 0.25 V_{PP}, A_V = +1		250		
Peak	Peaking	V_{OUT} = 0.25 V_{PP}, A_V = +1		3		dB
Peak_1	Peaking	V_{OUT} = 0.25 V_{PP}		0.05		dB
LSBW	–3 dB Bandwidth Large Signal	V_{OUT} = 2 V_{PP}		75		MHz
Peak_2	Peaking	V_{OUT} = 2 V_{PP}		0		dB
0.1 dB BW	0.1 dB Bandwidth	V_{OUT} = 2 V_{PP}		30		MHz
GBWP_1k	Gain Bandwidth Product	Unity Gain, R_L = 1 kΩ to V_S/2		115		MHz
GBWP_150		Unity Gain, R_L = 150Ω to V_S/2		105		
A_{VOL}	Large Signal Open Loop Gain	0.3V < V_{OUT} < 3V	56	67		dB
PBW	Full Power BW	–1 dB, A_V = +4, V_{OUT} = 2.8V_{PP}, R_L = 150Ω to V_S/2		30		MHz
DG	Differential Gain	4.43 MHz, 0.85V ≤ V_{OUT} ≤ 2.45V, R_L = 150Ω to V^-		0.06		%
DP	Differential Phase	4.43 MHz, 0.85V ≤ V_{OUT} ≤ 2.45V R_L = 150Ω to V^-		0.23		deg
Time Domain Response						
TRS/TRL	Rise & Fall Time	0.25V Step		2.7		ns
OS	Overshoot	0.25V Step		10		%
SR	Slew Rate	2V Step		260		V/μs
T_S	Settling Time	1V Step, ±0.1%		70		ns
T_{S_1}		1V Step, ±0.02%		300		
PD	Propagation Delay	Input to Output, 250 mV Step, 50%		2.6		ns
C_L	Cap Load Tolerance	A_V = −1, 10% Overshoot, 82Ω in Series		50		pF
Distortion & Noise Performance						
HD2	Harmonic Distortion (2nd)	2 V_{PP}, 10 MHz		−61		dBc
HD2_1		2 V_{PP}, 10 MHz R_L = 1 kΩ to V_S/2		−79		
HD3	Harmonic Distortion (3rd)	2 V_{PP}, 10 MHz		−53		dBc
HD3_2		2 V_{PP}, 10 MHz R_L = 1 kΩ to V_S/2		−69		
THD	Total Harmonic Distortion	2 V_{PP}, 10 MHz R_L = 1 kΩ to V_S/2		−66		dBc
V_{N1}	Input Voltage Noise	>10 MHz		7		$nV/\sqrt{Hz}$
V_{N2}		1 MHz		10		
I_N	Input Current Noise	>1 MHz		50		$fA/\sqrt{Hz}$
Static, DC Performance						
V_{IO}	Input Offset Voltage			±1	±2.6 **±5.5**	mV
DV_{IO}	Input Offset Voltage Average Drift	(3)		−4.5		μV/°C

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that T_J = T_A. No guarantee of parametric performance is indicated in the electrical tables under conditions of internal self-heating where T_J > T_A.
(2) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not guaranteed on shipped production material.
(3) Drift determined by dividing the change in parameter at temperature extremes by the total temperature change.

3.3V Electrical Characteristics (continued)

Single Supply with V_S= 3.3V, A_V = +2, R_F = 604Ω, $\overline{SD}$ tied to V^+, V_{OUT} = V_S/2, R_L = 150Ω to V^- unless otherwise specified. **Boldface** limits apply at temperature extremes. (1)

Symbol	Parameter	Condition		Min (2)	Typ (2)	Max (2)	Units
I_B	Input Bias Current	(4)			5	50	pA
I_{OS}	Input Offset Current	(4)			2	25	pA
R_{IN}	Input Resistance	0V ≤ V_{IN} ≤ 1.8V			15		TΩ
C_{IN}	Input Capacitance				1.4		pF
+PSRR	Positive Power Supply Rejection Ratio	DC		61 **51**	80		dB
−PSRR	Negative Power Supply Rejection Ratio	DC		57 **52**	72		dB
CMRR	Common Mode Rejection Ratio	DC		58 **55**	73		dB
CMVR	Input Voltage Range	CMRR > 50 dB		**V^- -0.20**	–	**V^+ -1.5**	V
I_{CC}	Supply Current	Normal Operation V_{OUT} = V_S/2			9.2	11 **13**	mA
		Shutdown $\overline{SD}$ tied to ≤ 0.33V (5)			100		nA
VOH1	Output High Voltage (Relative to V^+)	R_L = 150Ω to V^-		–210 **–360**	–190		mV
VOH2		R_L = 75Ω to V_S/2			–190		
VOH3		R_L = 10 kΩ to V^-		–50 **–100**	–10		
VOL1	Output Low Voltage (Relative to V^-)	R_L = 150Ω to V^-			+4	+45 **+125**	mV
VOL2		R_L = 75Ω to V_S/2			+105		
VOL3		R_L = 10 kΩ to V^-			+4	+45 **+125**	
I_O	Output Current	V_{OUT} < 0.6V from Respective Supply	Source		50		mA
			Sink		75		
I_O_1		V_{OUT} = V_S/2, V_{ID} = ±18 mV (6)		±75			
Load	Output Load Rating	THD < −30 dBc, f = 200 kHz, R_L tied to V_S/2, V_{OUT} = 2.6 V_{PP}			25		Ω
R_O_Enabled	Output Resistance	Enabled, A_V = +1			0.2		Ω
R_O_Disabled	Output Resistance	Shutdown			>100		MΩ
C_O_Disabled	Output Capacitance	Shutdown			5.6		pF
Miscellaneous Performance							
VDMAX	Voltage Limit for Disable (Pin 5)	(5)		**0**		**0.33**	V
VDMIN	Voltage Limit for Enable (Pin 5)	(5)		**2.97**		**3.3**	V
I_i	Logic Input Current (Pin 5)	$\overline{SD}$ = 3.3V (5)			8		pA
$V_{\_glitch}$	Turn-on Glitch				1.6		V
T_{on}	Turn-on Time				3.5		µs
T_{off}	Turn-off Time				500		ns
$Isolation_{OFF}$	Off Isolation	1 MHz, R_L = 1 kΩ			60		dB

(4) This parameter is guaranteed by design and/or characterization and is not tested in production.
(5) $\overline{SD}$ logic is CMOS compatible. To ensure proper logic level and to minimize power supply current, $\overline{SD}$ should typically be less than 10% of total supply voltage away from either supply rail.
(6) "V_{ID}" is input differential voltage (input overdrive).

2.7V Electrical Characteristics

Single Supply with V_S = 2.7V, A_V = +2, R_F = 604Ω, $\overline{SD}$ tied to V^+, V_{OUT} = V_S/2, R_L = 150Ω to V^- unless otherwise specified. **Boldface** limits apply at temperature extremes. (1)

Symbol	Parameter	Condition	Min (2)	Typ (2)	Max (2)	Units
Frequency Domain Response						
SSBW	–3 dB Bandwidth Small Signal	V_{OUT} = 0.25 V_{PP}		120		MHz
SSBW_1		V_{OUT} = 0.25 V_{PP}, A_V = +1		250		
Peak	Peaking	V_{OUT} = 0.25 V_{PP}, A_V = +1		3.1		dB
Peak_1	Peaking	V_{OUT} = 0.25 V_{PP}		0.1		dB
LSBW	–3 dB Bandwidth Large Signal	V_{OUT} = 2 V_{PP}		73		MHz
Peak_2	Peaking	V_{OUT} = 2 V_{PP}		0		dB
0.1 dB BW	0.1 dB Bandwidth	V_{OUT} = 2V_{PP}		30		MHz
GBWP_1k	Gain Bandwidth Product	Unity Gain, R_L = 1 kΩ to V_S/2		110		MHz
GBWP_150		Unity Gain, R_L = 150Ω to V_S/2		81		
A_{VOL}	Large Signal Open Loop Gain	0.25V < V_{OUT} < 2.5V	56	65		dB
PBW	Full Power BW	–1 dB, A_V = +4, V_{OUT} = 2 V_{PP}, R_L = 150Ω to V_S/2		13		MHz
DG	Differential Gain	4.43 MHz, 0.45V ≤ V_{OUT} ≤ 2.05V R_L = 150Ω to V^-		0.12		%
DP	Differential Phase	4.43 MHz, 0.45V ≤ V_{OUT} ≤ 2.05V R_L = 150Ω to V^-		0.62		deg
Time Domain Response						
TRS/TRL	Rise & Fall Time	0.25V Step		2.7		ns
OS	Overshoot	0.25V Step		10		%
SR	Slew Rate	2V Step		260		V/μs
T_S	Settling Time	1V Step, ±0.1%		147		ns
T_{S_1}		1V Step, ±0.02%		410		
PD	Propagation Delay	Input to Output, 250 mV Step, 50%		3.4		ns
Distortion & Noise Performance						
HD2	Harmonic Distortion (2^{nd})	1 V_{PP}, 10 MHz		−58		dBc
HD3	Harmonic Distortion (3^{rd})	1 V_{PP}, 10 MHz		−60		dBc
V_{N1}	Input Voltage Noise	>10 MHz		8.4		nV/$\sqrt{Hz}$
V_{N2}		1 MHz		12		
I_N	Input Current Noise	>1 MHz		50		fA/$\sqrt{Hz}$
Static, DC Performance						
V_{IO}	Input Offset Voltage			±1	±3.5 **±6.5**	mV
DV_{IO}	Input Offset Voltage Average Drift	(3)		−6.5		μV/°C
I_B	Input Bias Current	(4)		5	50	pA
I_{OS}	Input Offset Current	(4)		2	**25**	pA
R_{IN}	Input Resistance	0V ≤ V_{IN} ≤ 1.2V		20		TΩ
C_{IN}	Input Capacitance			1.6		pF
+PSRR	Positive Power Supply Rejection Ratio	DC	58 **53**	68		dB

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that T_J = T_A. No guarantee of parametric performance is indicated in the electrical tables under conditions of internal self-heating where T_J > T_A.
(2) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not guaranteed on shipped production material.
(3) Drift determined by dividing the change in parameter at temperature extremes by the total temperature change.
(4) This parameter is guaranteed by design and/or characterization and is not tested in production.

2.7V Electrical Characteristics (continued)

Single Supply with V_S = 2.7V, A_V = +2, R_F = 604Ω, $\overline{SD}$ tied to V^+, V_{OUT} = V_S/2, R_L = 150Ω to V^- unless otherwise specified. **Boldface** limits apply at temperature extremes. (1)

Symbol	Parameter	Condition		Min (2)	Typ (2)	Max (2)	Units
−PSRR	Negative Power Supply Rejection Ratio	DC		56 **53**	69		dB
CMRR	Common Mode Rejection Ratio	DC		57 **52**	77		dB
CMVR	Input Voltage Range	CMRR > 50 dB		**V^- -0.20**	–	**V^+ -1.5**	V
I_{CC}	Supply Current	Normal Operation V_{OUT} = V_S/2			9.0	10.6 **12.5**	mA
		Shutdown $\overline{SD}$ tied to ≤ 0.27V (5)			100		nA
VOH1	Output High Voltage (Relative to V^+)	R_L = 150Ω to V^-		–260 **–420**	–200		mV
VOH2		R_L = 75Ω to V_S/2			–200		mV
VOH3		R_L = 10 kΩ to V^-		–50 **100**	–10		mV
VOL1	Output Low Voltage (Relative to V^-)	R_L = 150Ω to V^-			+4	+45 **+125**	mV
VOL2		R_L = 75Ω to V_S/2			+125		mV
VOL3		R_L = 10 kΩ to V^-			+4	+45 **125**	mV
I_O	Output Current	V_{OUT} ≤ 0.6V from Respective Supply	Source		25		mA
			Sink		62		mA
I_O_1		V_{OUT} = V_S/2, V_{ID} = ±18 mV (6)	Source	25			mA
			Sink	35			mA
Load	Output Load Rating	THD < −30 dBc, f = 200 kHz, R_L tied to V_S/2, V_{OUT} = 2.2 V_{PP}			40		Ω
R_O_Enable	Output Resistance	Enabled, A_V = +1			0.2		Ω
R_O_Disabled	Output Resistance	Shutdown			>100		MΩ
C_O_Disabled	Output Capacitance	Shutdown			5.6		pF
Miscellaneous Performance							
VDMAX	Voltage Limit for Disable (Pin 5)	(5)		**0**		**0.27**	V
VDMIN	Voltage Limit for Enable (Pin 5)	(5)		**2.43**		**2.7**	V
I_i	Logic Input Current (Pin 5)	$\overline{SD}$ = 2.7V (5)			4		pA
$V_{\_glitch}$	Turn-on Glitch				1.2		V
T_{on}	Turn-on Time				5.2		µs
T_{off}	Turn-off Time				760		ns
$Isolation_{OFF}$	Off Isolation	1 MHz, R_L = 1 kΩ			60		dB

(5) $\overline{SD}$ logic is CMOS compatible. To ensure proper logic level and to minimize power supply current, $\overline{SD}$ should typically be less than 10% of total supply voltage away from either supply rail.
(6) "V_{ID}" is input differential voltage (input overdrive).

Connection Diagram

6-Pin SC70

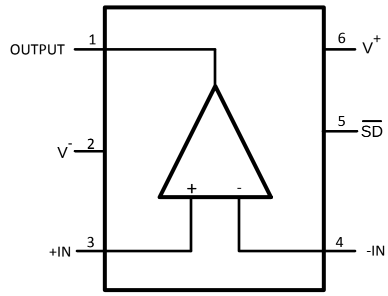
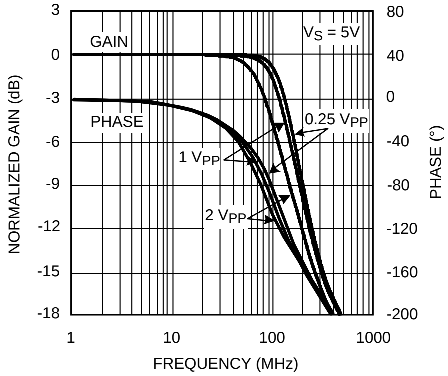


Figure 2. Top View

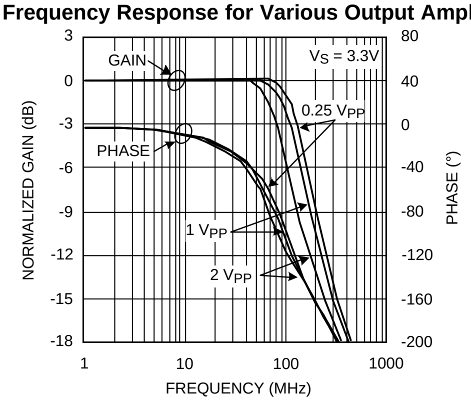
Typical Performance Characteristics

Unless otherwise noted, all data is with A_V = +2, R_F = R_G = 604Ω, V_S = 3.3V, V_{OUT} = V_S/2, $\overline{SD}$ tied to V^+, R_L = 150Ω to V^-, T = 25°C.

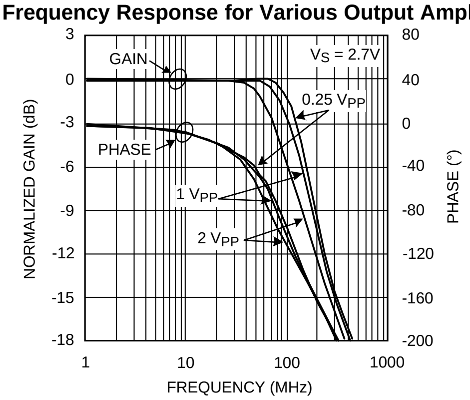
Frequency Response for Various Output Amplitudes



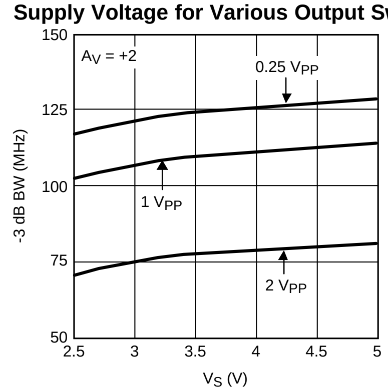
Frequency Response for Various Output Amplitudes



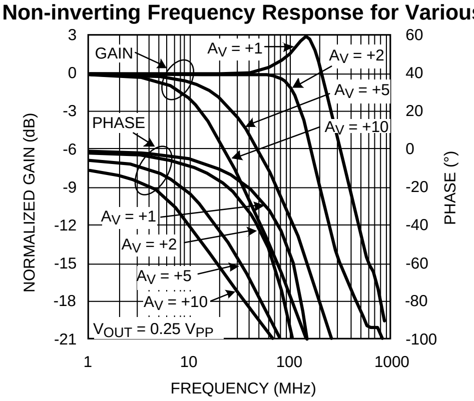
Frequency Response for Various Output Amplitudes



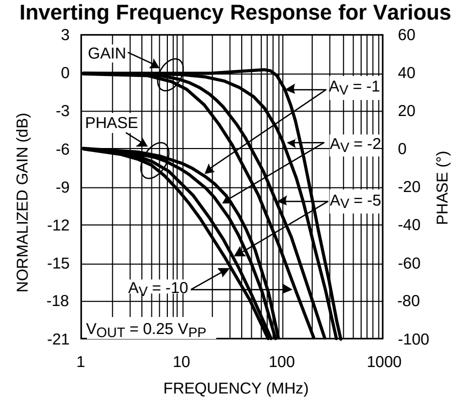
−3 dB BW vs. Supply Voltage for Various Output Swings



Non-inverting Frequency Response for Various Gain



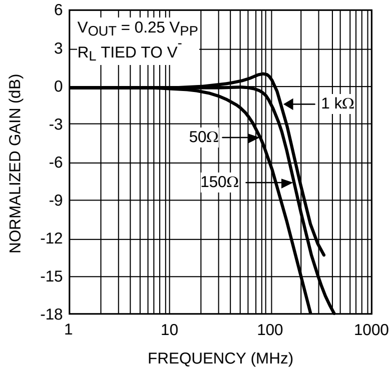
Inverting Frequency Response for Various Gain



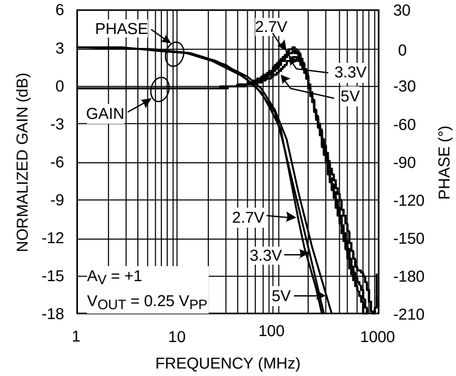
Typical Performance Characteristics (continued)

Unless otherwise noted, all data is with A_V = +2, R_F = R_G = 604Ω, V_S = 3.3V, V_{OUT} = V_S/2, $\overline{SD}$ tied to V^+, R_L = 150Ω to V^-, T = 25°C.

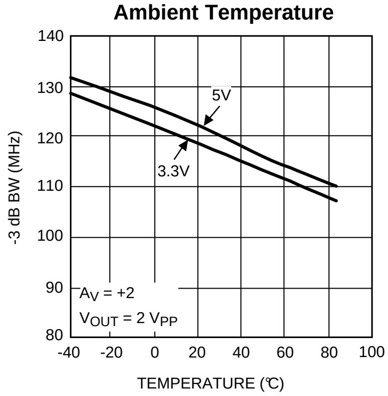
Frequency Response for Various Loads



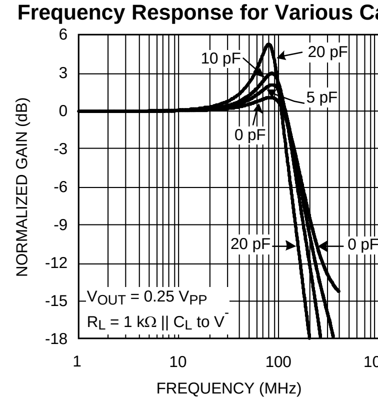
Frequency Response for Various Supply Voltages



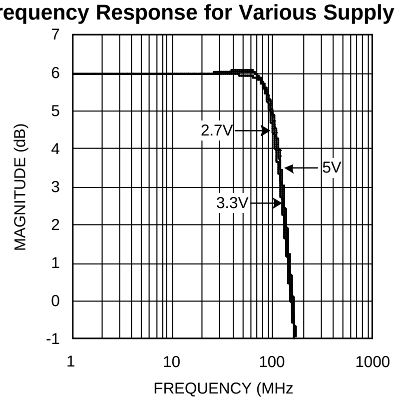
−3 dB BW vs. Ambient Temperature



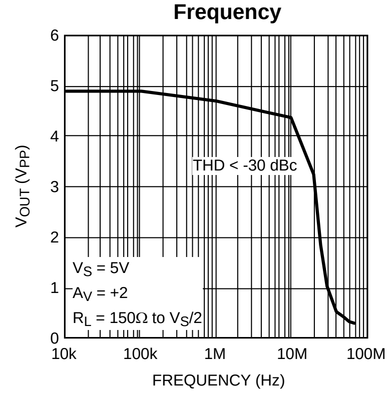
Frequency Response for Various Cap Load



Frequency Response for Various Supply Voltage



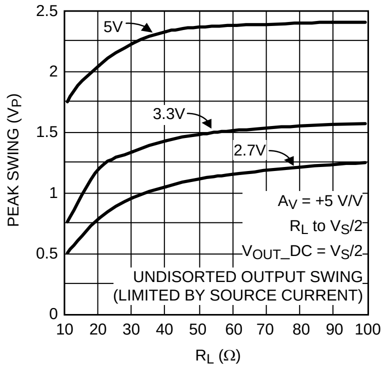
Max Output Swing vs. Frequency



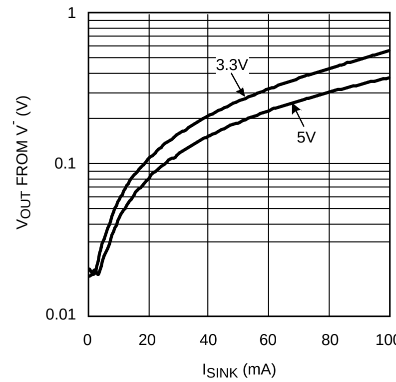
Typical Performance Characteristics (continued)

Unless otherwise noted, all data is with A_V = +2, R_F = R_G = 604Ω, V_S = 3.3V, V_{OUT} = V_S/2, $\overline{SD}$ tied to V^+, R_L = 150Ω to V^-, T = 25°C.

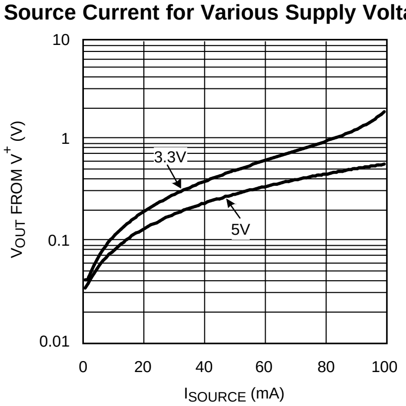
Peak Output Swing vs. R_L



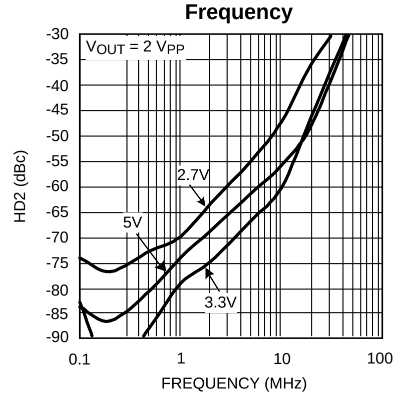
Output Swing vs. Sink Current for Various Supply Voltages



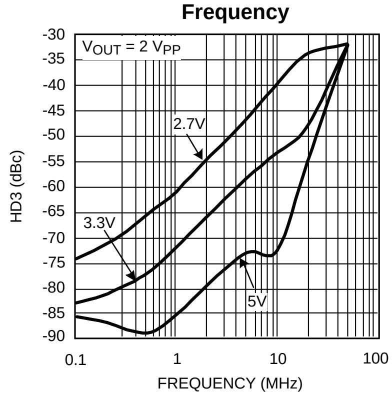
Output Swing vs. Source Current for Various Supply Voltages



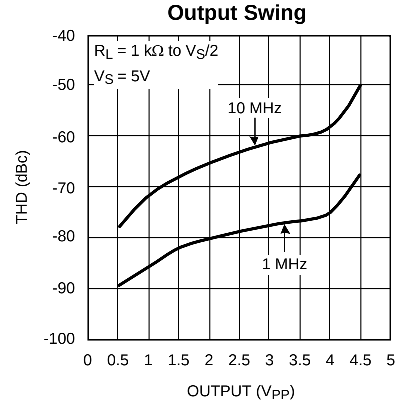
HD2 vs. Frequency



HD3 vs. Frequency



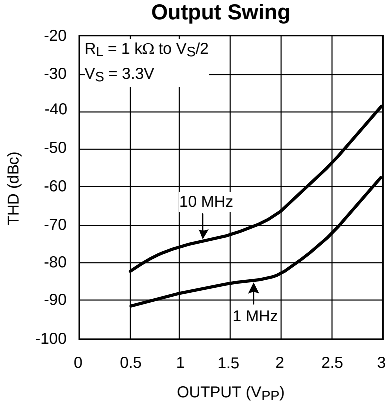
THD vs. Output Swing



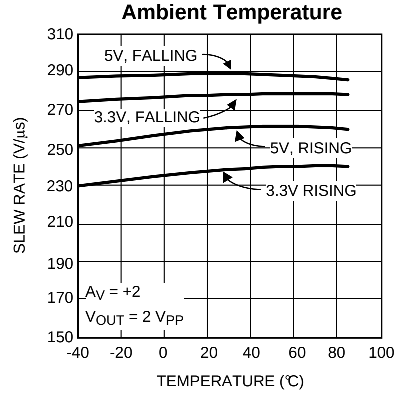
Typical Performance Characteristics (continued)

Unless otherwise noted, all data is with A_V = +2, R_F = R_G = 604Ω, V_S = 3.3V, V_{OUT} = V_S/2, $\overline{SD}$ tied to V^+, R_L = 150Ω to V^-, T = 25°C.

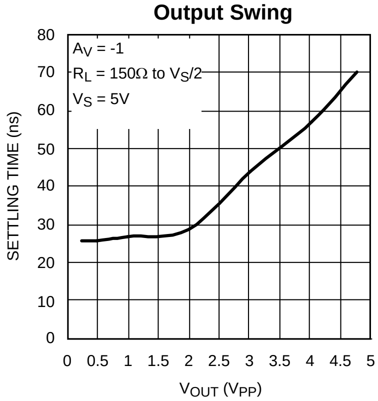
THD vs. Output Swing



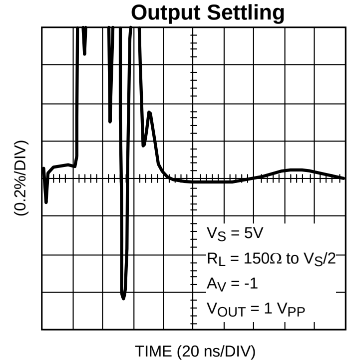
Slew Rate vs. Ambient Temperature



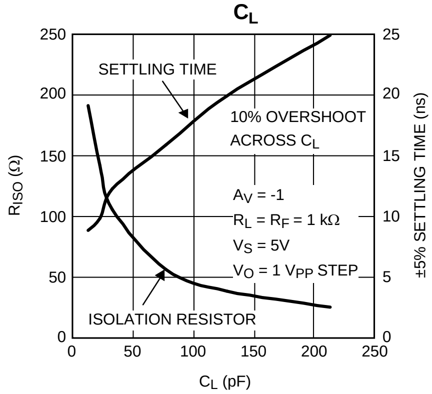
Settling Time (±1%) vs. Output Swing



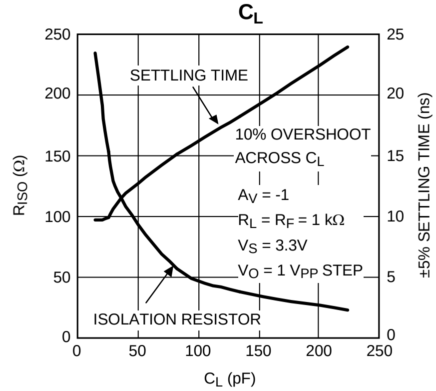
Output Settling



Isolation Resistor & Settling Time vs. C_L



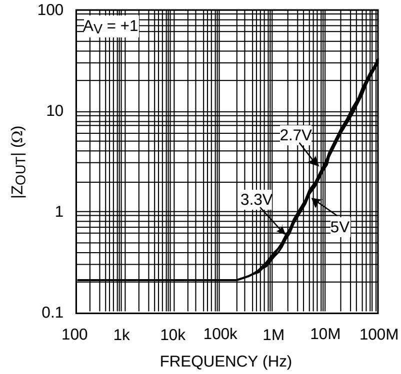
Isolation Resistor & Settling Time vs. C_L



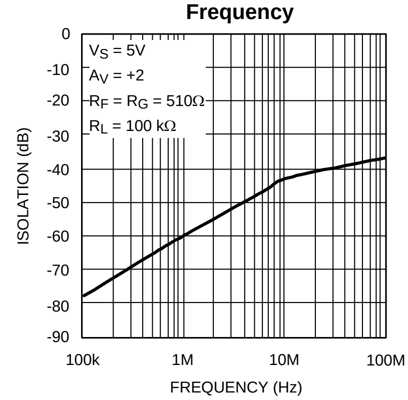
Typical Performance Characteristics (continued)

Unless otherwise noted, all data is with A_V = +2, R_F = R_G = 604Ω, V_S = 3.3V, V_{OUT} = V_S/2, $\overline{SD}$ tied to V^+, R_L = 150Ω to V^-, T = 25°C.

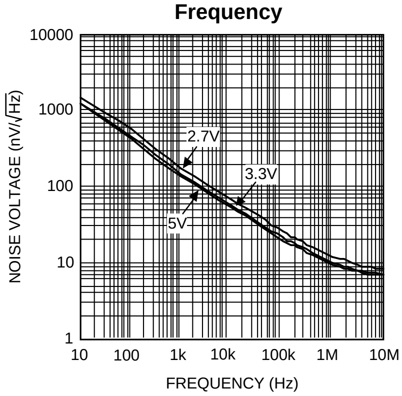
Closed Loop Output Impedance vs. Frequency for Various Supply Voltages



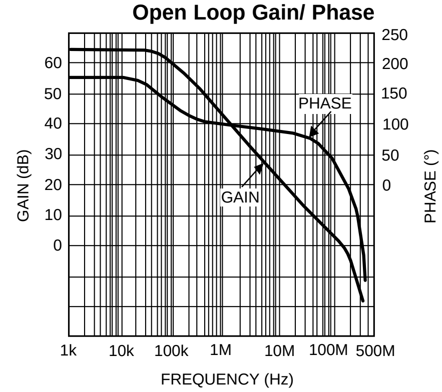
Off Isolation vs. Frequency



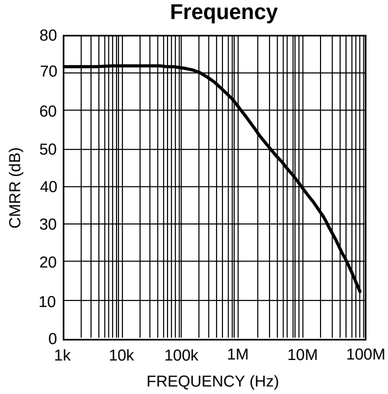
Noise Voltage vs. Frequency



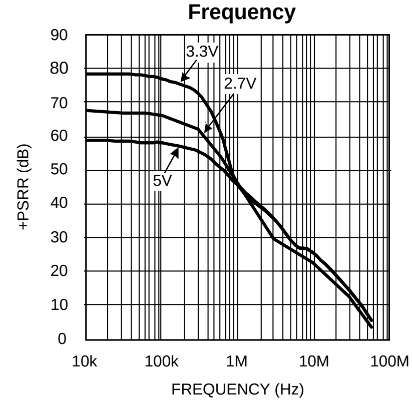
Open Loop Gain/ Phase



CMRR vs. Frequency



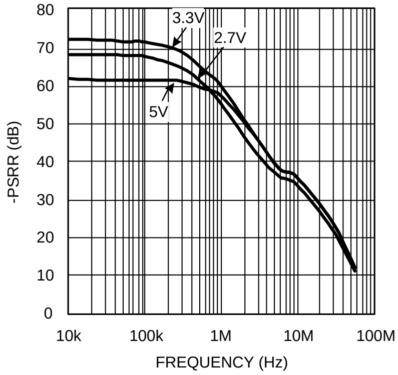
+PSRR vs. Frequency



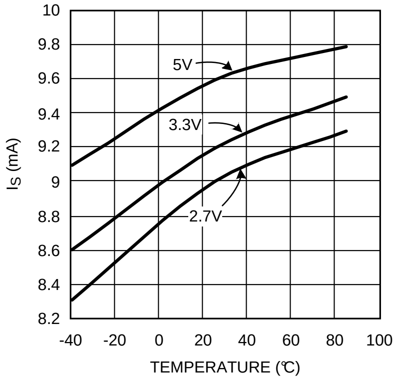
Typical Performance Characteristics (continued)

Unless otherwise noted, all data is with A_V = +2, R_F = R_G = 604Ω, V_S = 3.3V, V_{OUT} = V_S/2, $\overline{SD}$ tied to V^+, R_L = 150Ω to V^-, T = 25°C.

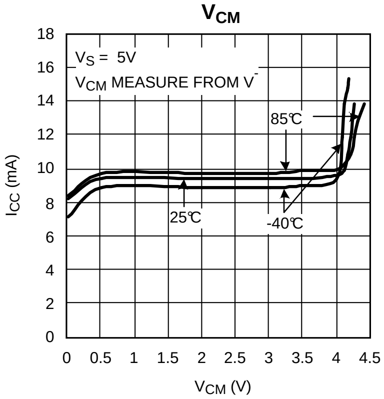
−PSRR vs. Frequency



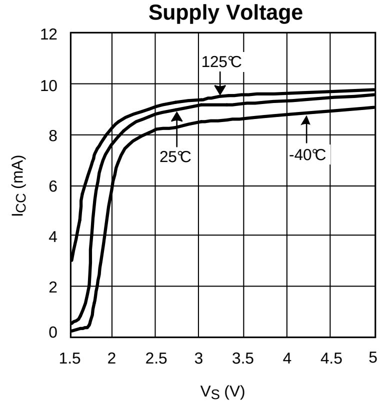
Supply Current vs. Ambient Temperature



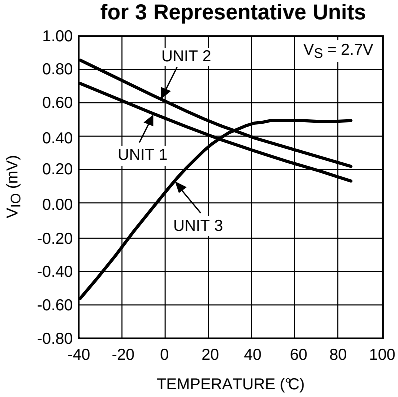
Supply Current vs. V_{CM}



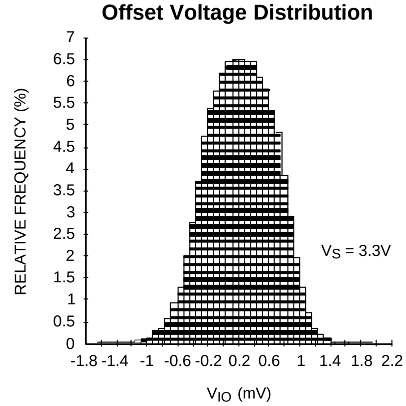
Supply Current vs. Supply Voltage



Offset Voltage vs. Ambient Temperature for 3 Representative Units



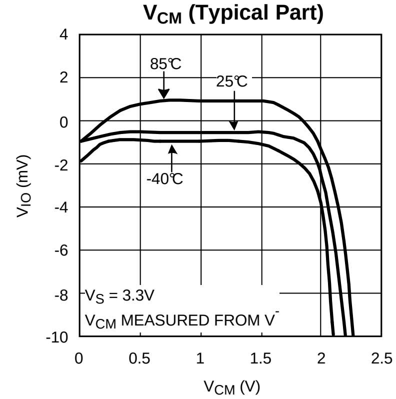
Offset Voltage Distribution



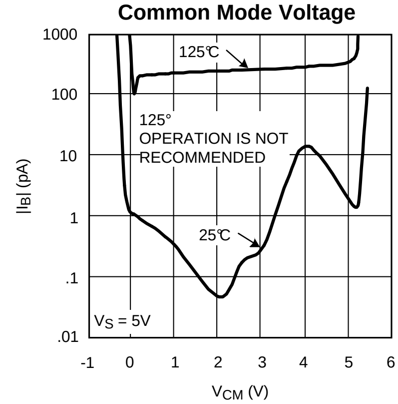
Typical Performance Characteristics (continued)

Unless otherwise noted, all data is with A_V = +2, R_F = R_G = 604Ω, V_S = 3.3V, V_{OUT} = V_S/2, $\overline{SD}$ tied to V^+, R_L = 150Ω to V^-, T = 25°C.

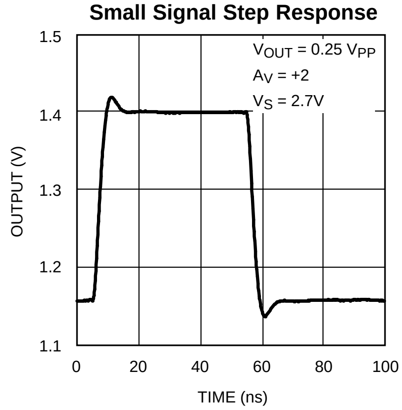
Offset Voltage vs. V_{CM} (Typical Part)



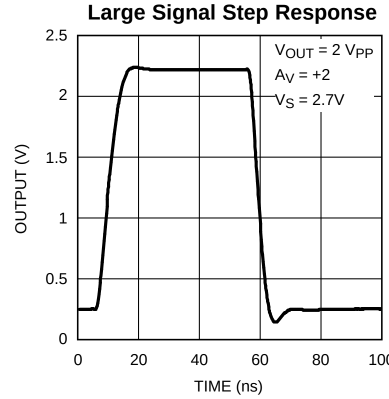
Input Bias Current vs. Common Mode Voltage



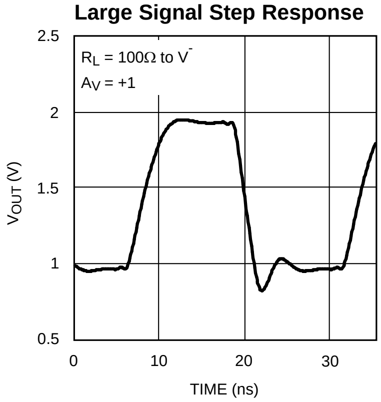
Small Signal Step Response



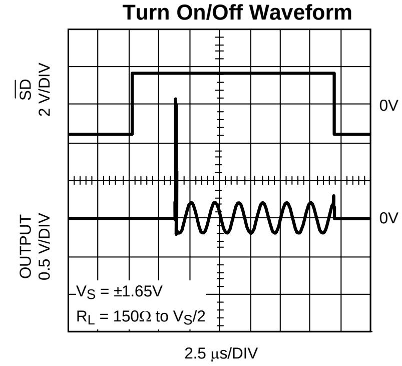
Large Signal Step Response



Large Signal Step Response



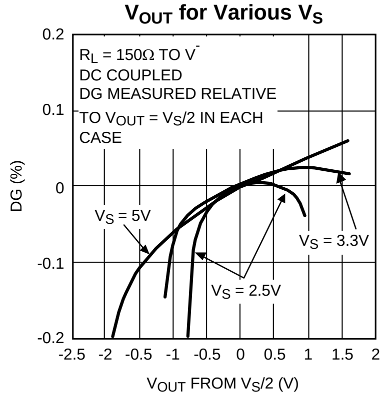
Turn On/Off Waveform



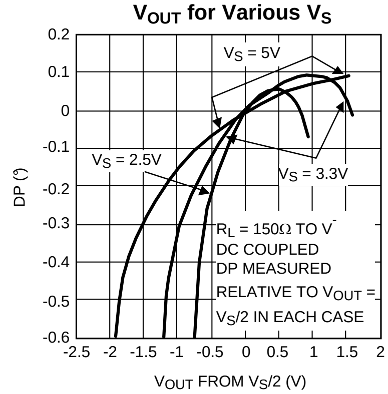
Typical Performance Characteristics (continued)

Unless otherwise noted, all data is with A_V = +2, R_F = R_G = 604Ω, V_S = 3.3V, V_{OUT} = V_S/2, $\overline{SD}$ tied to V^+, R_L = 150Ω to V^-, T = 25°C.

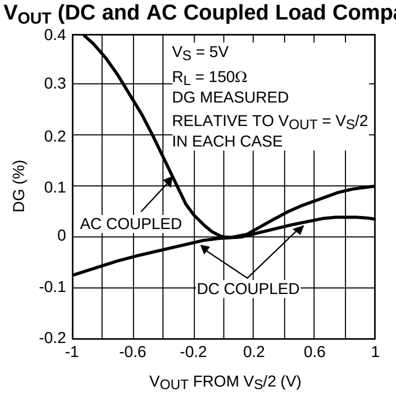
DG vs. V_{OUT} for Various V_S



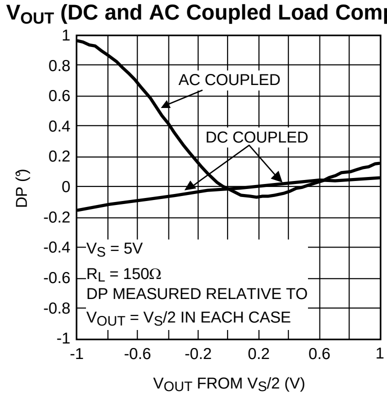
DP vs. V_{OUT} for Various V_S



DG vs. V_{OUT} (DC and AC Coupled Load Compared)



DP vs. V_{OUT} (DC and AC Coupled Load Compared)



Application Information

OPTIMIZING PERFORMANCE

With many op amps, additional device non-linearity and sometimes less loop stability arises when the output has to switch from current-source mode to current-sink mode or vice versa. When it comes to achieving the lowest distortion and the best Differential Gain/ Differential Phase (DG/ DP, broadcast video specs), the LMH6601 is optimized for single supply DC coupled output applications where the load current is returned to the negative rail (V^-). That is where the output stage is most linear (lowest distortion) and which corresponds to unipolar current flowing out of this device. To that effect, it is easy to see that the distortion specifications improve when the output is only sourcing current which is the distortion-optimized mode of operation for the LMH6601. In application where the LMH6601 output is AC coupled or when it is powered by separate dual supplies for V^+ and V^-, the output stage supplies both source and sink current to the load and results in less than optimum distortion (and DG/DP). Figure 3 compares the distortion results between a DC and an AC coupled load to show the magnitude of this difference. See the DG/DP plots in the Typical Performance Characteristics section for a comparison between DC and AC coupling of the video load.

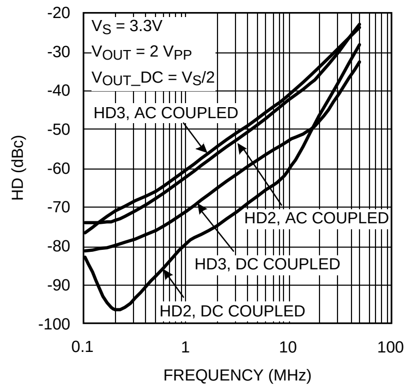


Figure 3. Distortion Comparison between DC & AC Coupling of the Load

In certain applications, it may be possible to optimize the LMH6601 for best distortion (and DG/DP) even though the load may require bipolar output current by adding a pull-down resistor to the output. Adding an output pull-down resistance of appropriate value could change the LMH6601 output loading into source-only. This comes at the price of higher total power dissipation and increased output current requirement.

Figure 4 shows how to calculate the pull-down resistor value for both the dual supply and for the AC coupled load applications.

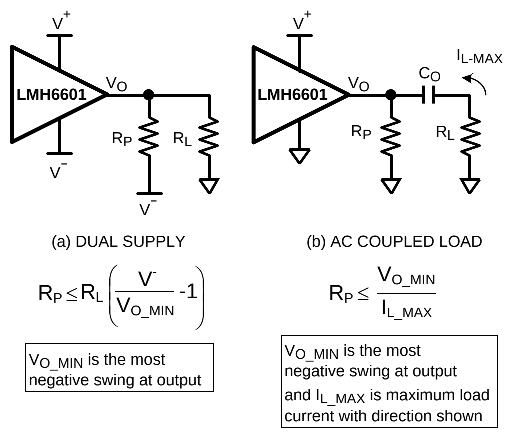


Figure 4. Output Pull-Down Value for Dual Supply & AC Coupling

Furthermore, with a combination of low closed loop gain setting (i.e. A_V = +1 for example where device bandwidth is the highest), light output loading (R_L > 1 kΩ) , and with a significant capacitive load (C_L > 10 pF) , the LMH6601 is most stable if output sink current is kept to less than about 5 mA. The pull-down method described in Figure 4 is applicable in these cases as well where the current that would normally be sunk by the op amp is diverted to the R_P path instead.

SHUTDOWN CAPABILITY AND TURN ON/ OFF BEHAVIOR

With the device in shutdown mode, the output goes into high impedance (R_{OUT} > 100 MΩ) mode. In this mode, the only path between the inputs and the output pin is through the external components around the device. So, for applications where there is active signal connection to the inverting input, with the LMH6601 in shutdown, the output could show signal swings due to current flow through these external components. For non-inverting amplifiers in shutdown, no output swings would occur, because of complete input-output isolation, with the exception of capacitive coupling.

For maximum power saving, the LMH6601 supply current drops to around 0.1 µA in shutdown. All significant power consumption within the device is disabled for this purpose. Because of this, the LMH6601 turn on time is measured in micro-seconds whereas its turn off is fast (nano-seconds) as would be expected from a high speed device like this.

The LMH6601 $\overline{SD}$ pin is a CMOS compatible input with a pico-ampere range input current drive requirement. This pin needs to be tied to a level or otherwise the device state would be indeterminate. The device shutdown threshold is half way between the V^+ and V^- pin potentials at any supply voltage. For example, with V^+ tied to 10V and V^- equal to 5V, you can expect the threshold to be at 7.5V. The state of the device (shutdown or normal operation) is guaranteed over temperature as longs as the $\overline{SD}$ pin is held to within 10% of the total supply voltage.

For V^+ = 10V, V^- = 5V, as an example:

- Shutdown Range 5V ≤ $\overline{SD}$ ≤ 5.5V
- Normal Operation Range 9.5V ≤ $\overline{SD}$ ≤ 10V

OVERLOAD RECOVERY AND SWING CLOSE TO RAILS

The LMH6601 can recover from an output overload in less than 20 ns. See Figure 5 below for the input and output scope photos:

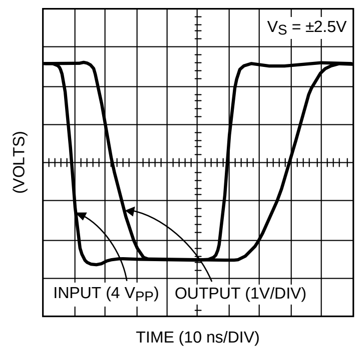


Figure 5. LMH6601 Output Overload Recovery Waveform

In Figure 5, the input step function is set so that the output is driven to one rail and then the other and then the output recovery is measured from the time the input crosses 0V to when the output reaches this point.

Also, when the LMH6601 input voltage range is exceeded near the V^+ rail, the output does not experience output phase reversal, as some op amps do. This is particularly advantageous in applications where output phase reversal has to be avoided at all costs, such as in servo loop control among others. This adds to the LMH6601's set of features which make this device easy to use.

In addition, the LMH6601's output swing close to either rail is well-behaved as can be seen in the scope photo of Figure 6.

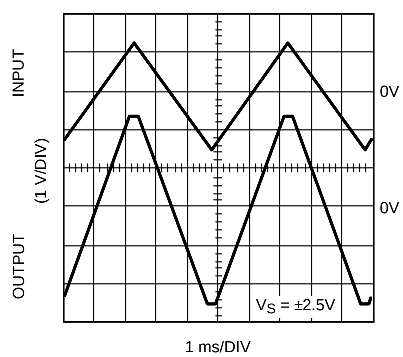


Figure 6. LMH6601's "Clean" Swing to Either Rail

With some op amps, when the output approaches either one or both rails and saturation starts to set in, there is significant increase in the transistor parasitic capacitances which leads to loss of Phase Margin. That is why with these devices, there are sometimes hints of instability with output close to the rails. With the LMH6601, as can be seen in Figure 6, the output waveform remains free of instability throughout its range of voltages.

SINGLE SUPPLY VIDEO APPLICATION

The LMH6601's high speed and fast slew rate make it an ideal choice for video amplifier and buffering applications. There are cost benefits in having a single operating supply. Single supply video systems can take advantage of the LMH6601's low supply voltage operation along with its ability to operate with input common mode voltages at or slightly below the V^- rail. Additional cost savings can be achieved by eliminating or reducing the value of the input and output AC coupling capacitors commonly employed in single supply video applications. This Application section shows some circuit techniques used to help in doing just that.

DC COUPLED, SINGLE SUPPLY BASEBAND VIDEO AMPLIFIER/DRIVER

The LMH6601 output can swing very close to either rail to maximize the output dynamic range which is of particular interest when operating in a low voltage single supply environment. Under light output load conditions, the output can swing as close as a few milli-volts of either rail. This also allows a video amplifier to preserve the video black level for excellent video integrity. In the example shown below in Figure 7, the baseband video output is amplified and buffered by the LMH6601 which then drives the 75Ω back terminated video cable for an overall gain of +1 delivered to the 75Ω load. The input video would normally have a level between 0V to approximately 0.75V.

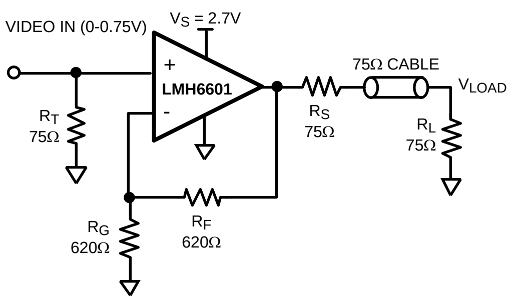


Figure 7. Single Supply Video Driver Capable of Maintaining Accurate Video Black Level

With the LMH6601 input common mode range including the V^- (ground) rail, there will be no need for AC coupling or level shifting and the input can directly drive the non-inverting input which has the additional advantage of high amplifier input impedance. With LMH6601's wide rail-to-rail output swing, as stated earlier, the video black level of 0V is maintained at the load with minimal circuit complexity and using no AC coupling capacitors. Without true rail-to-rail output swing of the LMH6601, and more importantly without the LMH6601's ability of exceedingly close swing to V^-, the circuit would not operate properly as shown at the expense of more complexity. This circuit will also work for higher input voltages. The only significant requirement is that there is at least 1.8V from the maximum input voltage to the positive supply (V^+).

The Composite Video Output of some low cost consumer video equipment consists of a current source which develops the video waveform across a load resistor (usually 75Ω), as shown in Figure 8 below. With these applications, the same circuit configuration just described and shown in Figure 8 will be able to buffer and drive the Composite Video waveform which includes sync and video combined. However, with this arrangement, the LMH6601 supply voltage needs to be at least 3.3V or higher in order to allow proper input common mode voltage headroom because the input can be as high as 1V peak.

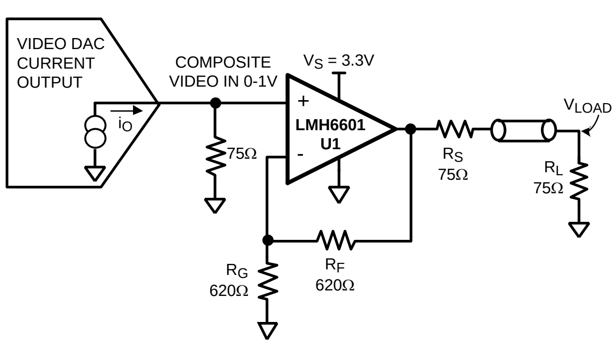


Figure 8. Single Supply Composite Video Driver for Consumer Video Outputs

If the “Video In” signal is Composite Video with negative going Sync tip, a variation of the previous configurations should be used. This circuit produces a unipolar (above 0V) DC coupled single supply video signal as shown in Figure 9.

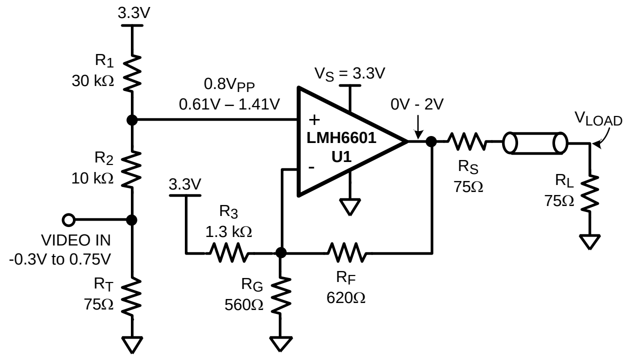


Figure 9. Single Supply DC Coupled Composite Video Driver for Negative Going Sync Tip

In the circuit of Figure 9, the input is shifted positive by means of R_1, R_2, and R_T in order to satisfy U1’s Common Mode input range. The signal will loose 20% of its amplitude in the process. The closed loop gain of U1 will need to be set to make up for this 20% loss in amplitude. This gives rise to the gain expression shown below which is based on a getting a 2 V_{PP} output with a 0.8 V_{PP} input:

$$\frac{R_F}{R_G||R_3} = \frac{2V}{0.8V} - 1 = 1.5V/V \quad (1)$$

R_3 will produce a negative shift at the output due to V_S (3.3V in this case). R_3 will need to be set so that the “Video In” sync tip (−0.3V at R_T or 0.61V at U1 non-inverting input) corresponds to near 0V at the output.

$$\frac{R_F}{R_3} = \frac{0.61}{3.3V - 0.61}\left(1 + \frac{R_F}{R_G}\right) = 0.227\left(1 + \frac{R_F}{R_G}\right) \quad (2)$$

Equation 1 and Equation 2 need to be solved simultaneously to arrive at the values of R_3, R_F, and R_G which will satisfy both. From the datasheet, one can set R_F = 620Ω to be close to the recommended value for a gain of +2. It is easier to solve for R_G and R_3 by starting with a good estimate for one and iteratively solving Equation and Equation 2 to arrive at the results. Here is one possible iteration cycle for reference:

R_F = 620Ω

Table 1. Finding Figure 9 External Resistor Values by Iteration

Estimate R_G (Ω)	Calculated (from Equation 2) R3 (Ω)	Equation 1 LHS Calculated	Comment (Compare Equation 1 LHS Calculated to RHS)
1k	1.69k	0.988	Increase Equation 1 LHS by reducing R_G
820	1.56k	1.15	Increase Equation 1 LHS by reducing R_G
620	1.37k	1.45	Increase Equation 1 LHS by reducing R_G
390	239	4.18	Reduce Equation 1 LHS by increasing R_G
560	**1.30k**	1.59	Close to target value of 1.5V/V for Equation 1

The final set of values for R_G and R_3 in Table 1 are values which will result in the proper gain and correct video levels (0V to 1V) at the output (V_{LOAD}).

AC COUPLED VIDEO

Many monitors and displays accept AC coupled inputs. This simplifies the amplification and buffering task in some respects. As can be seen in Figure 10, R_1 and R_2 simply set the input to the center of the input linear range while C_{IN} AC couples the video onto the op amp's input. The op amp is set for a closed loop gain of 2 with R_F and R_G. C_G is there to make sure the device output is also biased at mid-supply. Because of the DC bias at the output, the load needs to be AC coupled as well through C_O. Some applications implement a small valued ceramic capacitor (not shown) in parallel with C_O which is electrolytic. The reason for this is that the ceramic capacitor will tend to shunt the inductive behavior of the Electrolytic capacitor at higher frequencies for an improved overall low impedance output.

C_{G2} is intended to boost the high frequency gain in order to improve the video frequency response. This value is to be set and trimmed on the board to meet the application's specific system requirements.

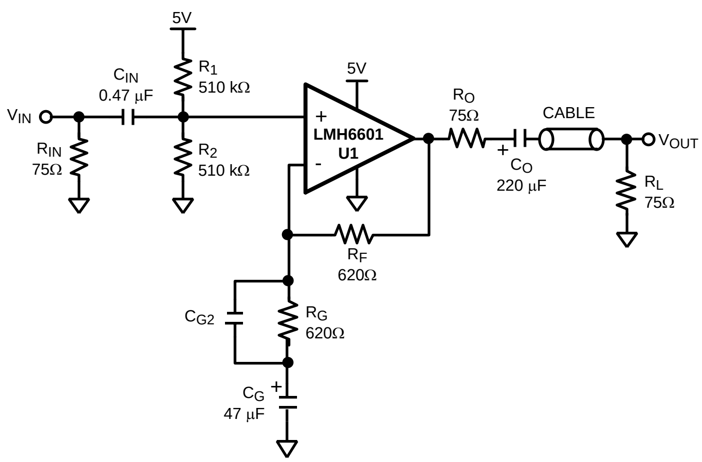


Figure 10. AC Coupled Video Amplifier/Driver

SAG COMPENSATION

The capacitors shown in Figure 10 (except C_{G2}), and especially C_O, are the large electrolytic type which are considerably costly and take up valuable real estate on the board. It is possible to reduce the value of the output coupling capacitor, C_O, which is the largest of all, by using what is called SAG compensation. SAG refers to what the output video experiences due to the low frequency video content it contains which cannot adequately go through the output AC coupling scheme due to the low frequency limit of this circuit. The −3 dB low frequency limit of the output circuit is given by:

f_low_frequency (−3 dB)= 1/ (2*pi* 75*2(Ω) * C_O) = ~ 4.82 Hz For C_O = 220 µF (3)

A possible implementation of the SAG compensation is shown in Figure 11.

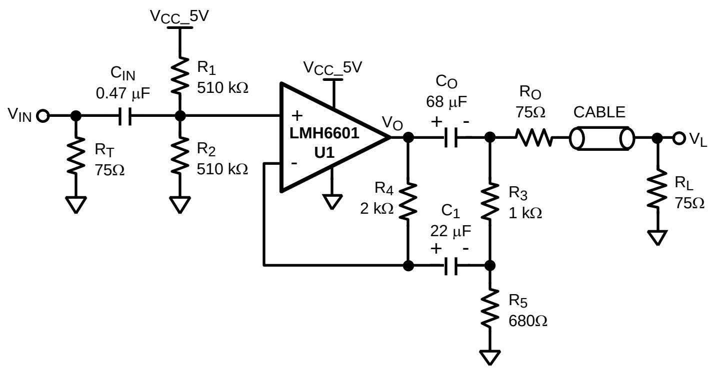


Figure 11. AC Coupled Video Amplifier/Driver with SAG Compensation

In this circuit, the output coupling capacitor value and size is reduced at the expense of a slightly more complicated circuitry. Note that C1 is not only part of the SAG compensation, but it also sets the amplifier's DC gain to 0 dB so that the output is set to mid-rail for linearity purposes. Also note that exceptionally high values are chosen for the R1 and R2 biasing resistors (510 kΩ). The LMH6601 has extremely low input bias current which allows this selection thereby reducing the C_{IN} value in this circuit such that C_{IN} can even be a non-polar capacitors which will reduce cost.

At high enough frequencies where both C_O and C_1 can be considered to be shorted out, R_3 shunts R_4 and the closed loop gain is determined by:

$$\text{Closed\_loop\_Gain (V/V)} = V_L/V_{IN} = (1 + (R_3||R_4)/R_5) \times [R_L/(R_L+R_O)] = 0.99\text{V/V} \quad (4)$$

At intermediate frequencies, where the C_O, R_O, R_L path experiences low frequency gain loss, the R_3, R_5, C_1 path provides feedback from the load side of C_O. With the load side gain reduced at these lower frequencies, the feedback to the op amp inverting node reduces, causing an increase at the op amp's output as a response.

For NTSC video, low values of C_O influence how much video black level shift occurs during the vertical blanking interval (~1.5 ms) which has no video activity and thus is sensitive to C_O's charge dissipation through the load which could cause output SAG. An especially tough pattern is the NTSC pattern called "Pulse & Bar." With this pattern the entire top and bottom portion of the field is black level video where, for about 11 ms, C_O is discharging through the load with no video activity to replenish that charge.

Figure 12 shows the output of the Figure 11 circuit highlighting the SAG.

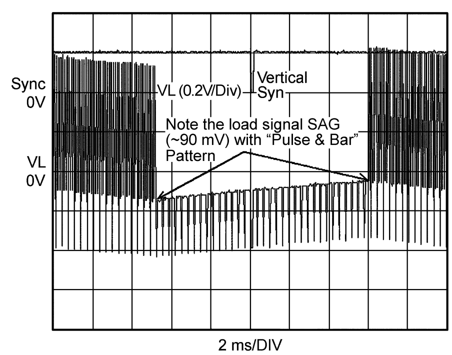


Figure 12. AC Coupled Video Amplifier/Driver Output Scope Photo Showing Video SAG

With the circuit of Figure 11 and any other AC coupled pulse amplifier, the waveform duty cycle variations exert additional restrictions on voltage swing at any node. This is illustrated in the waveforms shown in Figure 13.

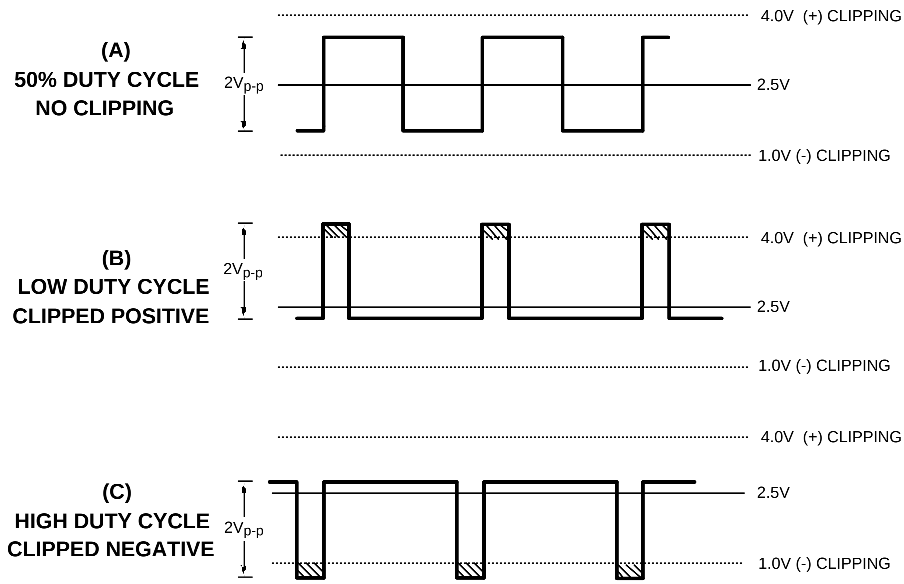


Figure 13. Headroom Considerations with AC Coupled Amplifiers

If a stage has a 3 V_{PP} unclipped swing capability available at a given node, as shown in Figure 13, the maximum allowable amplitude for an arbitrary waveform is ½ of 3V or 1.5 V_{PP}. This is due to the shift in the average value of the waveform as the duty cycle varies. Figure 13 shows what would happen if a 2 V_{PP} signal were applied. A low duty cycle waveform, such as the one in Figure 13*B*, would have high positive excursions. At low enough duty cycles, the waveform could get clipped on the top, as shown, or a more subtle loss of linearity could occur prior to full-blown clipping. The converse of this occurs with high duty cycle waveforms and negative clipping, as depicted in Figure 13*C*.

HOW TO PICK THE RIGHT VIDEO AMPLIFIER

Apart from output current drive and voltage swing, the op amp used for a video amplifier/cable driver should also possess the minimum requirement for speed and slew rate. For video type loads, it is best to consider Large Signal Bandwidth (or LSBW in the National Semiconductor data sheet tables) as video signals could be as large as 2 V_{PP} when applied to the commonly used gain of +2 configuration. Because of this relatively large swing, the op amp Slew Rate (SR) limitation should also be considered. Table 2 shows these requirements for various video line rates calculated using a rudimentary technique and intended as a first order estimate only.

Table 2. Rise Time, −3 dB BW, and Slew Rate Requirements for Various Video Line Rates

Video Standard	Line Rate (HxV)	Refresh Rate (Hz)	Horizontal Active (KH%)	Vertical Active (KV%)	Pixel Time (ns)	Rise Time (ns)	LSBW (MHz)	SR (V/μs)
TV_NTSC	451x483	30	84	92	118.3	39.4	9	41
VGA	640x480	75	80	95	33.0	11.0	32	146
SVGA	800x600	75	76	96	20.3	6.8	52	237
XGA	1024x768	75	77	95	12.4	4.1	85	387
SXGA	1280x1024	75	75	96	7.3	2.4	143	655
UXGA	1600x1200	75	74	96	4.9	1.6	213	973

For any video line rate (HxV corresponding to the number of Active horizontal and vertical lines), the speed requirements can be estimated if the Horizontal Active (KH%) and Vertical Active (KV%) numbers are known. These percentages correspond to the percentages of the active number of lines (horizontal or vertical) to the total number of lines as set by VESA standards. Here are the general expressions and the specific calculations for the SVGA line rate shown in Table 2.

$$\text{PIXEL\_TIME (ns)} = \frac{\frac{1}{\text{REFRESH\_RATE}} \times \text{KH} \times \text{KV}}{\text{H} \times \text{V}} \times 1 \times 10^5$$

$$= \frac{\frac{1}{75\text{ Hz}} \times 76 \times 96}{800 \times 600} \times 1 \times 10^5 = 20.3\text{ ns} \quad (5)$$

Requiring that an "On" pixel is illuminated to at least 90% of its final value before changing state will result in the rise/fall time equal to, at most, ⅓ the pixel time as shown below:

$$\text{RISE/FALL\_TIME} = \frac{\text{PIXEL\_TIME}}{3} = \frac{20.3\text{ ns}}{3} = 6.8\text{ ns} \quad (6)$$

Assuming a single pole frequency response roll-off characteristic for the closed loop amplifier used, we have:

$$-3\text{ dB\_BW} = \frac{0.35}{\text{RISE/FALL\_TIME}} = \frac{0.35}{6.8\text{ ns}} = 52\text{ MHz} \quad (7)$$

Rise/Fall times are 10%-90% transition times, which for a 2 V_{PP} video step would correspond to a total voltage shift of 1.6V (80% of 2V). So, the Slew Rate requirement can be calculated as follows:

$$\text{SR(V/}\mu\text{s)} = \frac{1.6\text{V}}{\text{RISE/FALL\_TIME (ns)}} \times 1 \times 10^3 = \frac{1.6\text{V}}{6.8\text{ ns}} = 237\text{(V/}\mu\text{s)} \quad (8)$$

The LMH6601 specifications show that it would be a suitable choice for video amplifiers up to and including the SVGA line rate as demonstrated above.

For more information about this topic and others relating to video amplifiers, please see Application Note 1013:

http://www.national.com/an/AN/AN-1013.pdf#page=1

CURRENT TO VOLTAGE CONVERSION (TRANSIMPEDANCE AMPLIFIER (TIA))

Being capable of high speed and having ultra low input bias current makes the LMH6601 a natural choice for Current to Voltage applications such as photodiode I-V conversion. In these type of applications, as shown in Figure 14 below, the photodiode is tied to the inverting input of the amplifier with R_F set to the proper gain (gain is measured in Ohms).

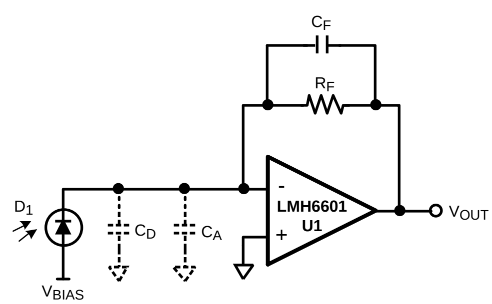


Figure 14. Typical Connection of a Photodiode Detector to an op amp

With the LMH6601 input bias current in the femto-amperes range, even large values of gain (R_F) do not increase the output error term appreciably. This allows circuit operation to a lower light intensity level which is always of special importance in these applications. Most photo-diodes have a relatively large capacitance (C_D) which would be even larger for a photo-diode designed for higher sensitivity to light because of its larger area. Some applications may run the photodiode with a reverse bias in order to reduce its capacitance with the disadvantage of increased contributions from both dark current and noise current. Figure 15 shows a typical photodiode capacitance plot vs. reverse bias for reference.

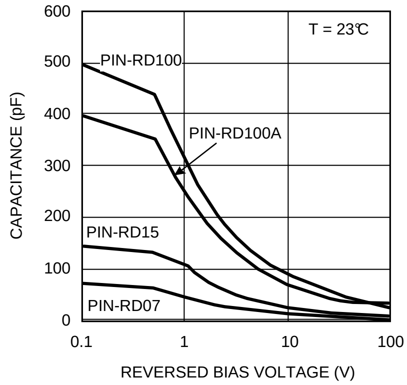


Figure 15. Typical Capacitance vs. Reverse Bias (Source: OSI Optoelectronics)

The diode capacitance (C_D) along with the input capacitance of the LMH6601 (C_A) has a bearing on the stability of this circuit and how it is compensated. With large transimpedance gain values (R_F), the total combined capacitance on the amplifier inverting input ($C_{IN} = C_D + C_A$) will work against R_F to create a zero in the Noise Gain (NG) function (see Figure 16). If left untreated, at higher frequencies where NG equals the open loop transfer function there will be excess phase shift around the loop (approaching 180°) and therefore, the circuit could be unstable. This is illustrated in Figure 16.

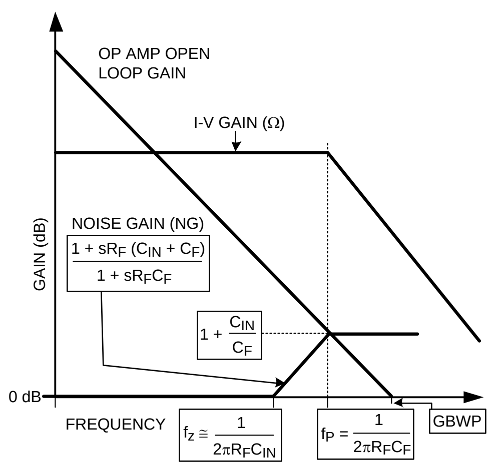


Figure 16. Transimpedance Amplifier Graphical Stability Analysis and Compensation

Figure 16 shows that placing a capacitor, C_F, with the proper value, across R_F will create a pole in the NG function at f_P. For optimum performance, this capacitor is usually picked so that NG is equal to the op amp's open loop gain at f_P. This will cause a “flattening” of the NG slope beyond the point of intercept of the two plots (open loop gain and NG) and will results in a Phase Margin (PM) of 45° assuming f_P and f_Z are at least a decade apart. This is because at the point of intercept, the NG pole at f_P will have a 45° phase lead contribution which leaves 45° of PM. For reference, Figure 16 also shows the transimpedance gain (I-V (Ω))

Here is the theoretical expression for the optimum C_F value and the expected −3 dB bandwidth:

$$C_F = \sqrt{\frac{C_{IN}}{2\pi(GBWP)R_F}} \quad (9)$$

$$f_{-3\,dB} \cong \sqrt{\frac{GBWP}{2\pi R_F C_{IN}}} \quad (10)$$

Table 3, below, lists the results, along with the assumptions and conditions, of testing the LMH6601 with various photodiodes having different capacitances (C_D) at a transimpedance gain (R_F) of 10 kΩ.

Table 3. Transimpedance Amplifier Figure 14 Compensation and Performance Results

C_D (pF)	C_{IN} (pF)	C_F_Calculated (pF)	C_F used (pF)	−3 dB BW Calculated (MHz)	−3 dB BW Measured (MHz)	Step Response Overshoot (%)
10	12	1.1	1	14	15	6
50	52	2.3	3	7	7.0	4
500	502	7.2	8	2	2.5	9

$$C_A = 2\text{ pF GBWP} = 155\text{ MHz } V_S = 5V \quad (11)$$

TRANSIMPEDANCE AMPLIFIER NOISE CONSIDERATIONS

When analyzing the noise at the output of the I-V converter, it is important to note that the various noise sources (i.e. op amp noise voltage, feedback resistor thermal noise, input noise current, photodiode noise current) do not all operate over the same frequency band. Therefore, when the noise at the output is calculated, this should be taken into account.

The op amp noise voltage will be gained up in the region between the noise gain's "zero" and its "pole" (f_z and f_p in Figure 16). The higher the values of R_F and C_{IN}, the sooner the noise gain peaking starts and therefore its contribution to the total output noise would be larger. It is obvious to note that it is advantageous to minimize C_{IN} (e.g. by proper choice of op amp, by applying a reverse bias across the diode at the expense of excess dark current and noise). However, most low noise op amps have a higher input capacitance compared to ordinary op amps. This is due to the low noise op amp's larger input stage.

OTHER APPLICATIONS

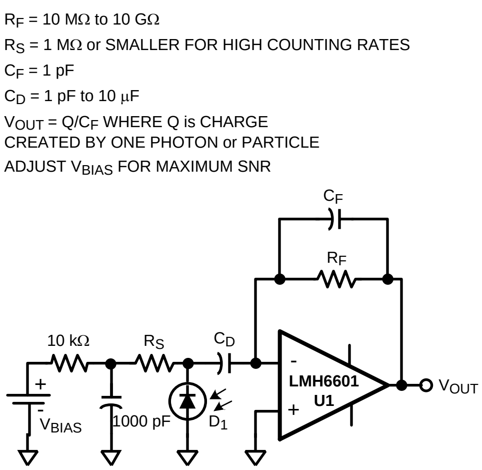


Figure 17. Charge Preamplifier Taking Advantage of LMH6601's Femto-Ampere Range Input Bias Current

CAPACITIVE LOAD

The LMH6601 can drive a capacitive load of up to 1000 pF with correct isolation and compensation. Figure 18 illustrates the in-loop compensation technique to drive a large capacitive load.

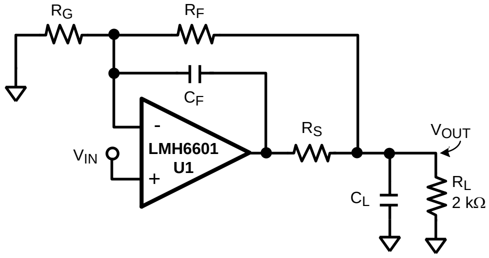


Figure 18. In-Loop Compensation Circuit for Driving a Heavy Capacitive Load

When driving a high capacitive load, an isolation resistor (R_S) should be connected in series between the op amp output and the capacitive load to provide isolation and to avoid oscillations. A small value capacitor (C_F) is inserted between the op amp output and the inverting input as shown such that this capacitor becomes the dominant feedback path at higher frequency. Together these components allow heavy capacitive loading while keeping the loop stable.

There are few factors which affect the driving capability of the op amp:

- Op amp internal architecture
- Closed loop gain and output capacitor loading

Table 4 shows the measured step response for various values of load capacitors (C_L), series resistor (R_S) and feedback resistor (C_F) with gain of +2 ($R_F = R_G = 604\Omega$) and R_L = 2 kΩ:

Table 4. LMH6601 Step Response Summary for the Circuit of Figure 18

C_L (pF)	R_S (Ω)	C_F (pF)	t_{rise}/ t_{fall} (ns)	Overshoot (%)
10	0	1	6 (1)	8
50	0	1	7 (2)	6
110	47	1	10	16
300	6	10	12	20
500	80	10	33	10
910	192	10	65	10

(1) Response limited by input step generator rise time of 5 ns
(2) Response limited by input step generator rise time of 5 ns

Figure 19 shows the increase in rise/fall time (bandwidth decrease) at V_{OUT} with larger capacitive loads, illustrating the trade-off between the two:

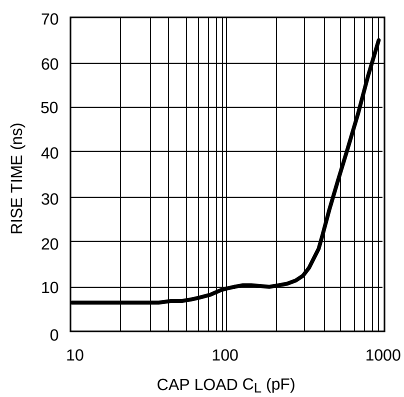


Figure 19. LMH6601 In-Loop Compensation Response

EVALUATION BOARD

National Semiconductor provides the following evaluation board as a guide for high frequency layout and as an aid in device testing and characterization. Many of the datasheet plots were measured with this board:

Device	Package	Board Part #
LMH6601MG	SC70-6	LMH730165

This evaluation board can be shipped when a device sample request is placed with National Semiconductor.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
LMH6601MG/NOPB	ACTIVE	SC70	DCK	6	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	
LMH6601MGX/NOPB	ACTIVE	SC70	DCK	6	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	
LMH6601QMG/NOPB	ACTIVE	SC70	DCK	6	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	
LMH6601QMGX/NOPB	ACTIVE	SC70	DCK	6	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF LMH6601, LMH6601-Q1 :

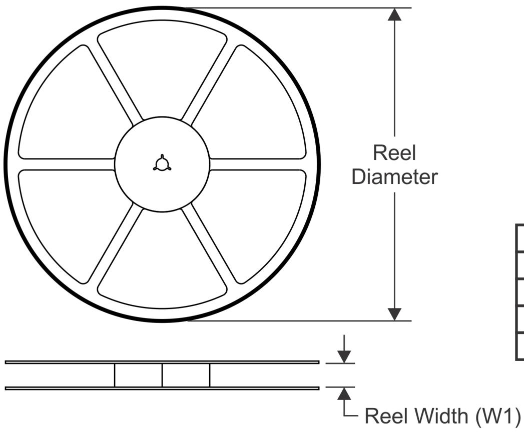
- Catalog: LMH6601
- Automotive: LMH6601-Q1

NOTE: Qualified Version Definitions:

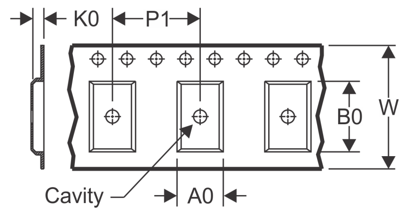
- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

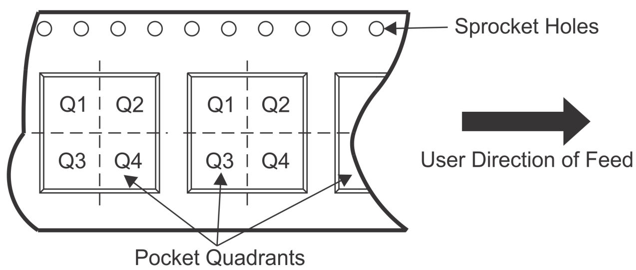


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

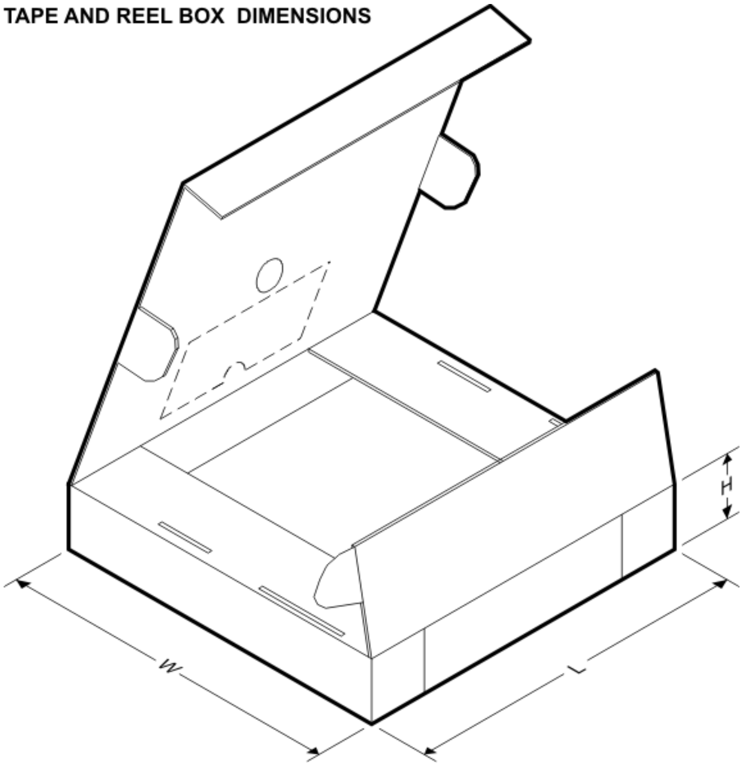
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMH6601MG/NOPB	SC70	DCK	6	1000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
LMH6601MGX/NOPB	SC70	DCK	6	3000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
LMH6601QMG/NOPB	SC70	DCK	6	1000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
LMH6601QMGX/NOPB	SC70	DCK	6	3000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3

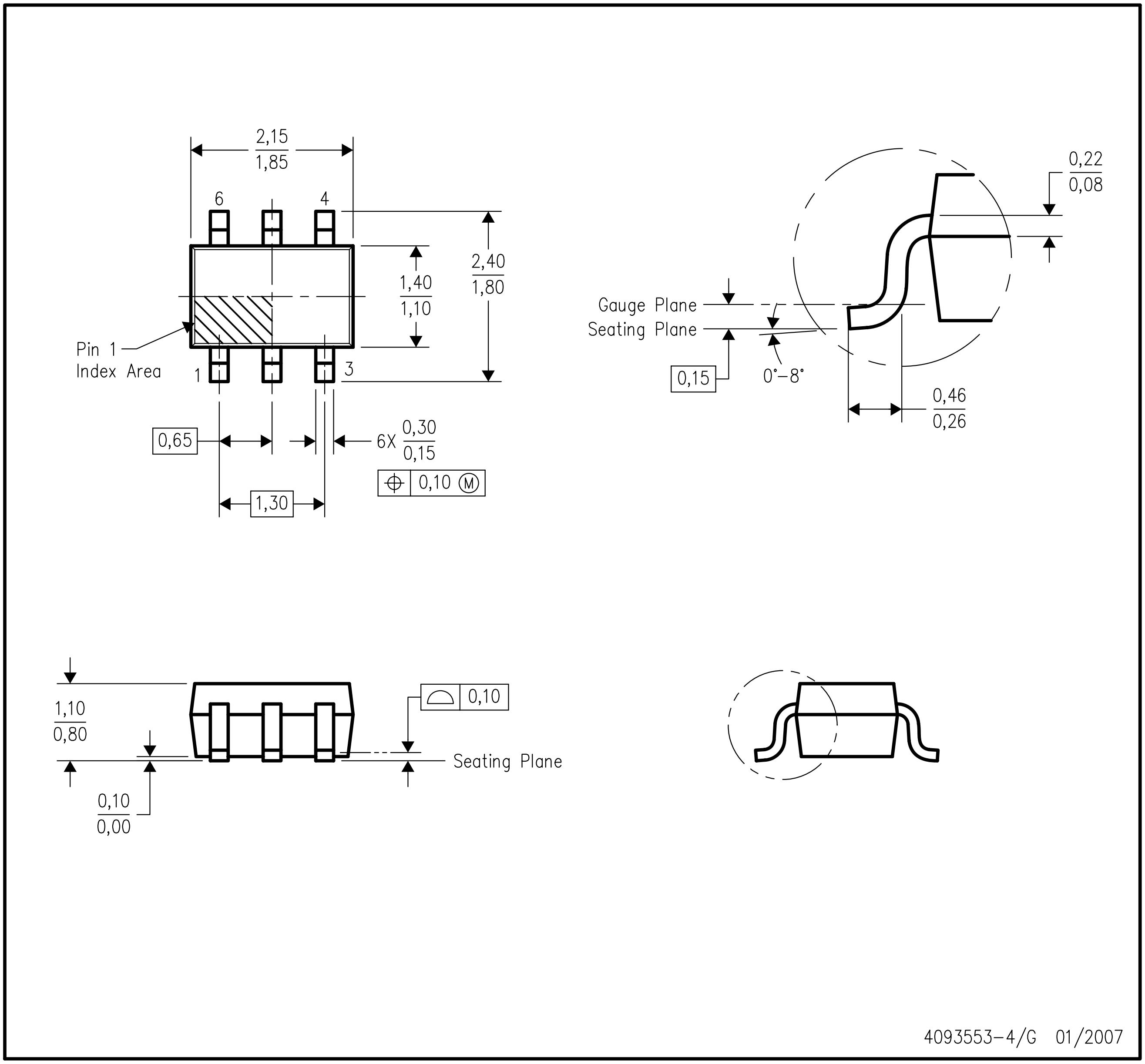
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMH6601MG/NOPB	SC70	DCK	6	1000	203.0	190.0	41.0
LMH6601MGX/NOPB	SC70	DCK	6	3000	206.0	191.0	90.0
LMH6601QMG/NOPB	SC70	DCK	6	1000	203.0	190.0	41.0
LMH6601QMGX/NOPB	SC70	DCK	6	3000	206.0	191.0	90.0

DCK (R-PDSO-G6) PLASTIC SMALL-OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO-203 variation AB.

IMPORTANT NOTICE

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