LMH6642EP/LMH6643EP/LMH6644EP Enhanced Plastic Low Power, 130MHz, 75mA Rail-to-Rail Output Amplifiers

Check for Samples: LMH6642EP, LMH6643EP, LMH6644EP

FEATURES

- **(V_S = ±5V, T_A = 25°C, R_L = 2kΩ, A_V = +1. Typical values unless specified).**
- **−3dB BW (A_V = +1) 130MHz**
- **Supply voltage range 2.7V to 12.8V**
- **Slew rate (1), (A_V = −1) 130V/µs**
- **Supply current (no load) 2.7mA/amp**
- **Output short circuit current +115mA/−145mA**
- **Linear output current ±75mA**
- **Input common mode volt. 0.5V beyond V^-, 1V from V^+**
- **Output voltage swing 40mV from rails**
- **Input voltage noise (100kHz) 17nV/$\sqrt{Hz}$**
- **Input current noise (100kHz) 0.9pA/$\sqrt{Hz}$**
- **THD (5MHz, R_L = 2kΩ, V_O = $2V_{PP}$, A_V = +2) −62dBc**
- **Settling time 68ns**
- **Fully characterized for 3V, 5V, and ±5V**
- **Overdrive recovery 100ns**
- **Output short circuit protected (2)**
- **No output phase reversal with CMVR exceeded**

(1) Slew rate is the average of the rising and falling slew rates.

(2) Output short circuit duration is infinite for V_S < 6V at room temperature and below. For V_S > 6V, allowable short circuit duration is 1.5ms.

APPLICATIONS

- **Selected Military Applications**
- **Selected Avionics Applications**

DESCRIPTION

The LMH664XEP family true single supply voltage feedback amplifiers offer high speed (130MHz), low distortion (−62dBc), and exceptionally high output current (approximately 75mA) at low cost and with reduced power consumption when compared against existing devices with similar performance.

Input common mode voltage range extends to 0.5V below V^- and 1V from V^+. Output voltage range extends to within 40mV of either supply rail, allowing wide dynamic range especially desirable in low voltage applications. The output stage is capable of approximately 75mA in order to drive heavy loads. Fast output Slew Rate (130V/µs) ensures large peak-to-peak output swings can be maintained even at higher speeds, resulting in exceptional full power bandwidth of 40MHz with a 3V supply. These characteristics, along with low cost, are ideal features for a multitude of industrial and commercial applications.

Careful attention has been paid to ensure device stability under all operating voltages and modes. The result is a very well behaved frequency response characteristic (0.1dB gain flatness up the 12MHz under 150Ω load and A_V = +2) with minimal peaking (typically 2dB maximum) for any gain setting and under both heavy and light loads. This along with fast settling time (68ns) and low distortion allows the device to operate well in ADC buffer, and high frequency filter applications as well as other applications.

This device family offers professional quality video performance with low DG (0.01%) and DP (0.01°) characteristics. Differential Gain and Differential Phase characteristics are also well maintained under heavy loads (150Ω) and throughout the output voltage range. The LMH664XEP family is offered in single (LMH6642EP), dual (LMH6643EP), and quad (LMH6644EP) options. See ordering information for packages offered.

ENHANCED PLASTIC

- Extended Temperature Performance of −40°C to +85°C
- Baseline Control - Single Fab & Assembly Site
- Process Change Notification (PCN)
- Qualification & Reliability Data
- Solder (PbSn) Lead Finish is standard

- Enhanced Diminishing Manufacturing Sources (DMS) Support

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings [(1)]

ESD Tolerance	2KV [(2)]
	200V [(3)]
V_{IN} Differential	±2.5V
Output Short Circuit Duration	[(4)], [(5)]
Supply Voltage (V^+ - V^-)	13.5V
Voltage at Input/Output pins	V^+ +0.8V, V^- −0.8V
Input Current	±10mA
Storage Temperature Range	−65°C to +150°C
Junction Temperature [(6)]	+150°C
Soldering Information	
Infrared or Convection Reflow(20 sec)	235°C
Wave Soldering Lead Temp.(10 sec)	260°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics.
(2) Human body model, 1.5kΩ in series with 100pF.
(3) Machine Model, 0Ω in series with 200pF.
(4) Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C.
(5) Output short circuit duration is infinite for V_S < 6V at room temperature and below. For V_S > 6V, allowable short circuit duration is 1.5ms.
(6) The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly onto a PC board.

Operating Ratings [(1)]

Supply Voltage (V^+ – V^-)	2.7V to 12.8V
Junction Temperature Range [(2)]	−40°C to +85°C
Package Thermal Resistance [(2)] (θ_{JA})	
SOT23-5	265°C/W
SOIC-8	190°C/W
MSOP-8	235°C/W
SOIC-14	145°C/W
TSSOP-14	155°C/W

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics.
(2) The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly onto a PC board.

3V Electrical Characteristics

Unless otherwise specified, all limits guaranteed for at T_J = 25°C, V^+ = 3V, V^- = 0V, V_{CM} = V_O = $V^+/2$, and R_L = 2kΩ to $V^+/2$. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (1)	Typ (2)	Max (1)	Units
BW	−3dB BW	A_V = +1, V_{OUT} = 200mV_{PP}	80	115		MHz
		A_V = +2, −1, V_{OUT} = 200mV_{PP}		46		
$BW_{0.1dB}$	0.1dB Gain Flatness	A_V = +2, R_L = 150Ω to V+/2, R_L = 402Ω, V_{OUT} = 200mV_{PP}		19		MHz
PBW	Full Power Bandwidth	A_V = +1, −1dB, V_{OUT} = 1V_{PP}		40		MHz
e_n	Input-Referred Voltage Noise	f = 100kHz		17		nV/$\sqrt{Hz}$
		f = 1kHz		48		
i_n	Input-Referred Current Noise	f = 100kHz		0.90		pA/$\sqrt{Hz}$
		f = 1kHz		3.3		
THD	Total Harmonic Distortion	f = 5MHz, V_O = 2V_{PP}, A_V = −1, R_L = 100Ω to $V^+/2$		−48		dBc
DG	Differential Gain	V_{CM} = 1V, NTSC, A_V = +2 R_L =150Ω to $V^+/2$		0.17		%
		R_L =1kΩ to $V^+/2$		0.03		
DP	Differential Phase	V_{CM} = 1V, NTSC, A_V = +2 R_L =150Ω to $V^+/2$		0.05		deg
		R_L =1kΩ to $V^+/2$		0.03		
CT Rej.	Cross-Talk Rejection	f = 5MHz, Receiver: R_f = R_g = 510Ω, A_V = +2		47		dB
T_S	Settling Time	V_O = 2V_{PP}, ±0.1%, 8pF Load, V_S = 5V		68		ns
SR	Slew Rate (3)	A_V = −1, V_I = 2V_{PP}	90	120		V/μs
V_{OS}	Input Offset Voltage			±1	±5 **±7**	mV
TC V_{OS}	Input Offset Average Drift	(4)		±5		μV/°C
I_B	Input Bias Current	(5)		−1.50	−2.60 **−3.25**	μA
I_{OS}	Input Offset Current			20	800 **1000**	nA
R_{IN}	Common Mode Input Resistance			3		MΩ
C_{IN}	Common Mode Input Capacitance			2		pF
CMVR	Input Common-Mode Voltage Range	CMRR ≥ 50dB		−0.5	−0.2 **−0.1**	V
			1.8 **1.6**	2.0		
CMRR	Common Mode Rejection Ratio	V_{CM} Stepped from 0V to 1.5V	72	95		dB
A_{VOL}	Large Signal Voltage Gain	V_O = 0.5V to 2.5V R_L = 2kΩ to $V^+/2$	80 **75**	96		dB
		V_O = 0.5V to 2.5V R_L = 150Ω to $V^+/2$	74 **70**	82		
V_O	Output Swing High	R_L = 2kΩ to $V^+/2$, V_{ID} = 200mV	2.90	2.98		V
		R_L = 150Ω to $V^+/2$, V_{ID} = 200mV	2.80	2.93		
	Output Swing Low	R_L = 2kΩ to $V^+/2$, V_{ID} = −200mV		25	75	mV
		R_L = 150Ω to $V^+/2$, V_{ID} = −200mV		75	150	

(1) All limits are guaranteed by testing or statistical analysis.
(2) Typical values represent the most likely parametric norm.
(3) Slew rate is the average of the rising and falling slew rates.
(4) Offset voltage average drift determined by dividing the change in V_{OS} at temperature extremes by the total temperature change.
(5) Positive current corresponds to current flowing into the device.

3V Electrical Characteristics (continued)

Unless otherwise specified, all limits guaranteed for at T_J = 25°C, V^+ = 3V, V^- = 0V, V_{CM} = V_O = V^+/2, and R_L = 2kΩ to V^+/2. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (1)	Typ (2)	Max (1)	Units
I_{SC}	Output Short Circuit Current	Sourcing to V^+/2 V_{ID} = 200mV (6)	50 **35**	95		mA
		Sinking to V^+/2 V_{ID} = −200mV (6)	55 **40**	110		
I_{OUT}	Output Current	V_{OUT} = 0.5V from either supply		±65		mA
+PSRR	Positive Power Supply Rejection Ratio	V^+ = 3.0V to 3.5V, V_{CM} = 1.5V	75	85		dB
I_S	Supply Current (per channel)	No Load		2.70	4.00 **4.50**	mA

(6) Short circuit test is a momentary test. See Note 14.

5V Electrical Characteristics

Unless otherwise specified, all limits guaranteed for at T_J = 25°C, V^+ = 5V, V^- = 0V, V_{CM} = V_O = V^+/2, and R_L = 2kΩ to V^+/2. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (1)	Typ (2)	Max (1)	Units
BW	−3dB BW	A_V = +1, V_{OUT} = 200mV_{PP}	90	120		MHz
		A_V = +2, −1, V_{OUT} = 200mV_{PP}		46		
$BW_{0.1dB}$	0.1dB Gain Flatness	A_V = +2, R_L = 150Ω to V+/2, R_f = 402Ω, V_{OUT} = 200mV_{PP}		15		MHz
PBW	Full Power Bandwidth	A_V = +1, −1dB, V_{OUT} = 2V_{PP}		22		MHz
e_n	Input-Referred Voltage Noise	f = 100kHz		17		$nV/\sqrt{Hz}$
		f = 1kHz		48		
i_n	Input-Referred Current Noise	f = 100kHz		0.90		$pA/\sqrt{Hz}$
		f = 1kHz		3.3		
THD	Total Harmonic Distortion	f = 5MHz, V_O = 2V_{PP}, A_V = +2		−60		dBc
DG	Differential Gain	NTSC, A_V = +2 R_L =150Ω to V^+/2		0.16		%
		R_L =1kΩ to V^+/2		0.05		
DP	Differential Phase	NTSC, A_V = +2 R_L =150Ω to V^+/2		0.05		deg
		R_L =1kΩ to V^+/2		0.01		
CT Rej.	Cross-Talk Rejection	f = 5MHz, Receiver: R_f = R_g = 510Ω, A_V = +2		47		dB
T_S	Settling Time	V_O = 2V_{PP}, ±0.1%, 8pF Load		68		ns
SR	Slew Rate (3)	A_V = −1, V_I = 2V_{PP}	95	125		V/µs
V_{OS}	Input Offset Voltage			±1	±5 **±7**	mV
TC V_{OS}	Input Offset Average Drift	(4)		±5		µV/°C
I_B	Input Bias Current	(5)		−1.70	−2.60 **−3.25**	µA
I_{OS}	Input Offset Current			20	800 **1000**	nA
R_{IN}	Common Mode Input Resistance			3		MΩ
C_{IN}	Common Mode Input Capacitance			2		pF
CMVR	Input Common-Mode Voltage Range	CMRR ≥ 50dB		−0.5	−0.2 **−0.1**	V
			3.8 **3.6**	4.0		
CMRR	Common Mode Rejection Ratio	V_{CM} Stepped from 0V to 3.5V	72	95		dB
A_{VOL}	Large Signal Voltage Gain	V_O = 0.5V to 4.50V R_L = 2kΩ to V^+/2	86 **82**	98		dB
		V_O = 0.5V to 4.25V R_L = 150Ω to V^+/2	76 **72**	82		
V_O	Output Swing High	R_L = 2kΩ to V^+/2, V_{ID} = 200mV	4.90	4.98		V
		R_L = 150Ω to V^+/2, V_{ID} = 200mV	4.65	4.90		
	Output Swing Low	R_L = 2kΩ to V^+/2, V_{ID} = −200mV		25	100	mV
		R_L = 150Ω to V^+/2, V_{ID} = −200mV		100	150	

(1) All limits are guaranteed by testing or statistical analysis.
(2) Typical values represent the most likely parametric norm.
(3) Slew rate is the average of the rising and falling slew rates.
(4) Offset voltage average drift determined by dividing the change in V_{OS} at temperature extremes by the total temperature change.
(5) Positive current corresponds to current flowing into the device.

5V Electrical Characteristics (continued)

Unless otherwise specified, all limits guaranteed for at T_J = 25°C, V^+ = 5V, V^- = 0V, V_{CM} = V_O = V^+/2, and R_L = 2kΩ to V^+/2. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (1)	Typ (2)	Max (1)	Units
I_{SC}	Output Short Circuit Current	Sourcing to V^+/2 V_{ID} = 200mV (6)	55 **40**	115		mA
		Sinking to V^+/2 V_{ID} = −200mV (6)	70 **55**	140		
I_{OUT}	Output Current	V_O = 0.5V from either supply		±70		mA
+PSRR	Positive Power Supply Rejection Ratio	V^+ = 4.0V to 6V	79	90		dB
I_S	Supply Current (per channel)	No Load		2.70	4.25 **5.00**	mA

(6) Short circuit test is a momentary test. See Note 14.

±5V Electrical Characteristics

Unless otherwise specified, all limits guaranteed for at T_J = 25°C, V^+ = 5V, V^- = −5V, V_{CM} = V_O = 0V and R_L = 2kΩ to ground. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (1)	Typ (2)	Max (1)	Units
BW	−3dB BW	A_V = +1, V_{OUT} = 200mV_{PP}	95	130		MHz
		A_V = +2, −1, V_{OUT} = 200mV_{PP}		46		
$BW_{0.1dB}$	0.1dB Gain Flatness	A_V = +2, R_L = 150Ω to V+/2, R_f = 806Ω, V_{OUT} = 200mV_{PP}		12		MHz
PBW	Full Power Bandwidth	A_V = +1, −1dB, V_{OUT} = 2V_{PP}		24		MHz
e_n	Input-Referred Voltage Noise	f = 100kHz		17		$nV/\sqrt{Hz}$
		f = 1kHz		48		
i_n	Input-Referred Current Noise	f = 100kHz		0.90		$pA/\sqrt{Hz}$
		f = 1kHz		3.3		
THD	Total Harmonic Distortion	f = 5MHz, V_O = 2V_{PP}, A_V = +2		−62		dBc
DG	Differential Gain	NTSC, A_V = +2 R_L =150Ω to V^+/2		0.15		%
		R_L =1kΩ to V^+/2		0.01		
DP	Differential Phase	NTSC, A_V = +2 R_L =150Ω to V^+/2		0.04		deg
		R_L =1kΩ to V^+/2		0.01		
CT Rej.	Cross-Talk Rejection	f = 5MHz, Receiver: R_f = R_g = 510Ω, A_V = +2		47		dB
T_S	Settling Time	V_O = 2V_{PP}, ±0.1%, 8pF Load, V_S = 5V		68		ns
SR	Slew Rate (3)	A_V = −1, V_I = 2V_{PP}	100	135		V/μs
V_{OS}	Input Offset Voltage			±1	±5 **±7**	mV
TC V_{OS}	Input Offset Average Drift	(4)		±5		μV/°C
I_B	Input Bias Current	(5)		−1.60	−2.60 **−3.25**	μA
I_{OS}	Input Offset Current			20	800 **1000**	nA
R_{IN}	Common Mode Input Resistance			3		MΩ
C_{IN}	Common Mode Input Capacitance			2		pF
CMVR	Input Common-Mode Voltage Range	CMRR ≥ 50dB		−5.5	−5.2 **−5.1**	V
			3.8 **3.6**	4.0		
CMRR	Common Mode Rejection Ratio	V_{CM} Stepped from −5V to 3.5V	74	95		dB
A_{VOL}	Large Signal Voltage Gain	V_O = −4.5V to 4.5V, R_L = 2kΩ	88 **84**	96		dB
		V_O = −4.0V to 4.0V, R_L = 150Ω	78 **74**	82		
V_O	Output Swing High	R_L = 2kΩ, V_{ID} = 200mV	4.90	4.96		V
		R_L = 150Ω, V_{ID} = 200mV	4.65	4.80		
	Output Swing Low	R_L = 2kΩ, V_{ID} = −200mV		−4.96	−4.90	V
		R_L = 150Ω, V_{ID} = −200mV		−4.80	−4.65	

(1) All limits are guaranteed by testing or statistical analysis.
(2) Typical values represent the most likely parametric norm.
(3) Slew rate is the average of the rising and falling slew rates.
(4) Offset voltage average drift determined by dividing the change in V_{OS} at temperature extremes by the total temperature change.
(5) Positive current corresponds to current flowing into the device.

±5V Electrical Characteristics (continued)

Unless otherwise specified, all limits guaranteed for at T_J = 25°C, V^+ = 5V, V^- = −5V, V_{CM} = V_O = 0V and R_L = 2kΩ to ground. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (1)	Typ (2)	Max (1)	Units
I_{SC}	Output Short Circuit Current	Sourcing to Ground V_{ID} = 200mV (6)	60 **35**	115		mA
		Sinking to Ground V_{ID} = −200mV (6)	85 **65**	145		
I_{OUT}	Output Current	V_O = 0.5V from either supply	±75			mA
PSRR	Power Supply Rejection Ratio	(V^+, V^-) = (4.5V, −4.5V) to (5.5V, −5.5V)	78	90		dB
I_S	Supply Current (per channel)	No Load		2.70	4.50 **5.50**	mA

(6) Short circuit test is a momentary test. See Note 14.

Connection Diagram

SOT23-5 (LMH6642)

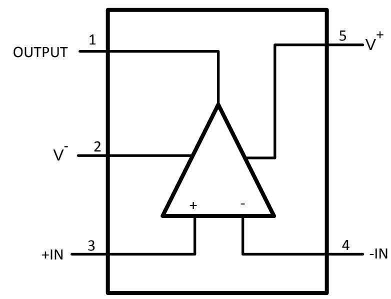


Figure 1. Top View

SOIC-8 (LMH6642)

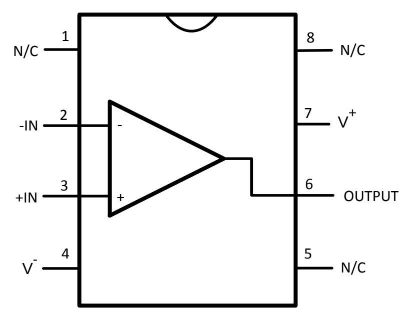


Figure 2. Top View

SOIC-8 and MSOP-8 (LMH6643)

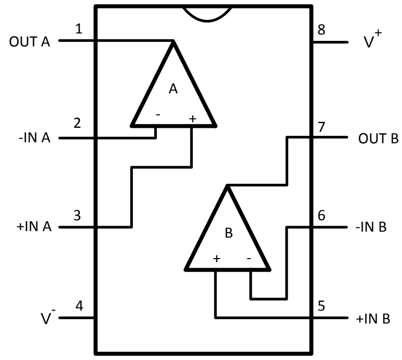


Figure 3. Top View

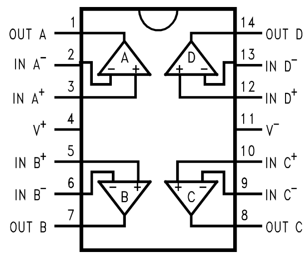
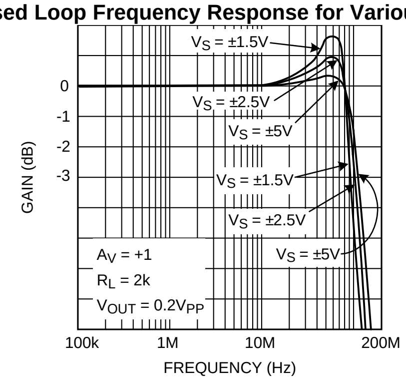


Figure 4. SOIC-14 and TSSOP-14, (LMH6644) - Top View

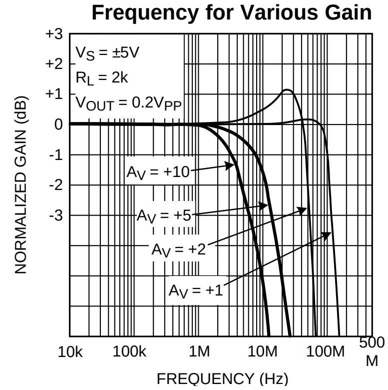
Typical Performance Characteristics

At T_J = 25°C, V^+ = +5, V^- = −5V, R_F = R_L = 2kΩ. Unless otherwise specified.

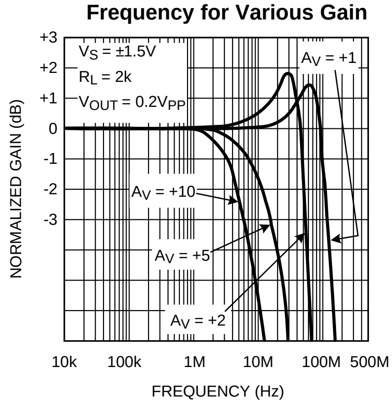
Closed Loop Frequency Response for Various Supplies



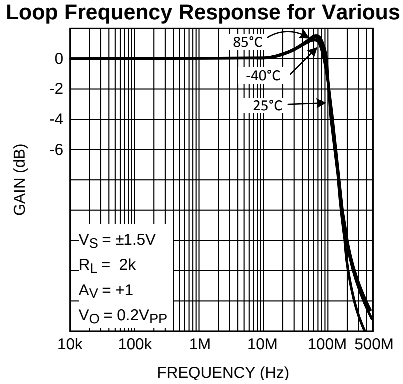
Closed Loop Gain vs. Frequency for Various Gain



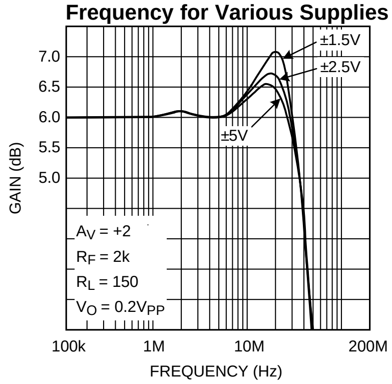
Closed Loop Gain vs. Frequency for Various Gain



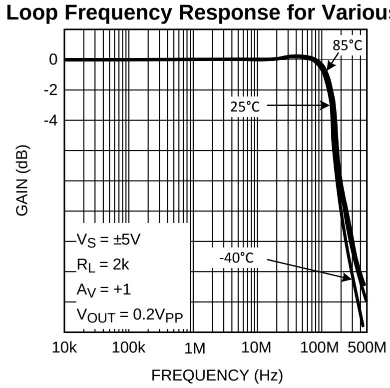
Closed Loop Frequency Response for Various Temperature



Closed Loop Gain vs. Frequency for Various Supplies



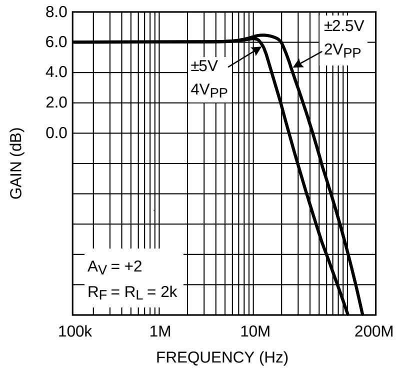
Closed Loop Frequency Response for Various Temperature



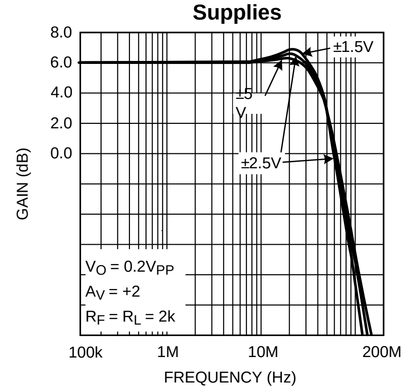
Typical Performance Characteristics (continued)

At T_J = 25°C, V^+ = +5, V^- = −5V, R_F = R_L = 2kΩ. Unless otherwise specified.

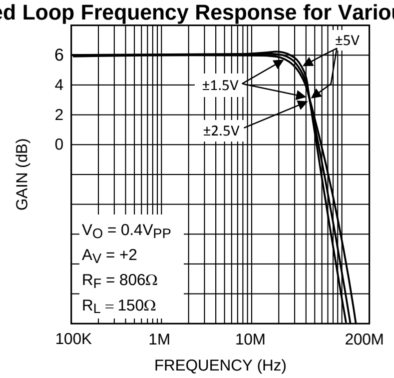
Large Signal Frequency Response



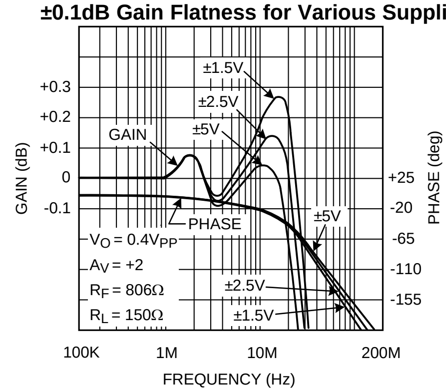
Closed Loop Small Signal Frequency Response for Various Supplies



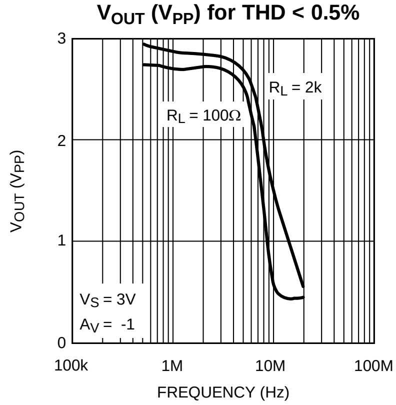
Closed Loop Frequency Response for Various Supplies



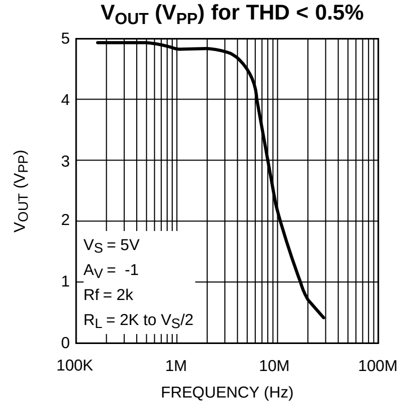
±0.1dB Gain Flatness for Various Supplies



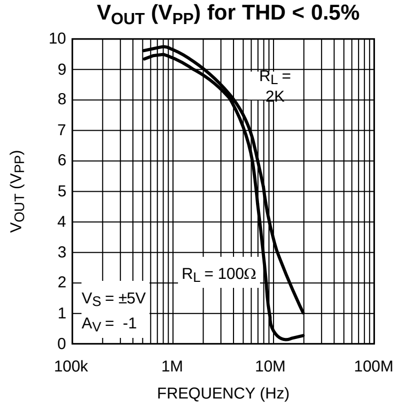
V_{OUT} (V_{PP}) for THD < 0.5%



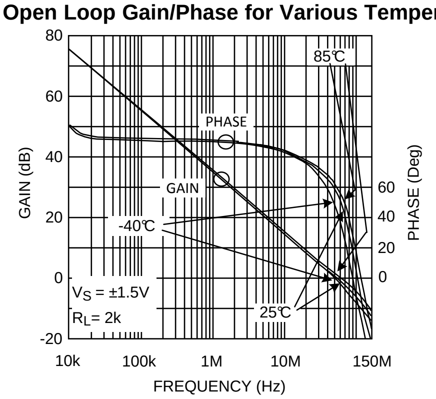
V_{OUT} (V_{PP}) for THD < 0.5%



V_{OUT} (V_{PP}) for THD < 0.5%



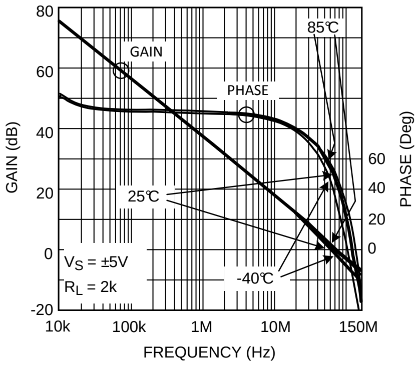
Open Loop Gain/Phase for Various Temperature



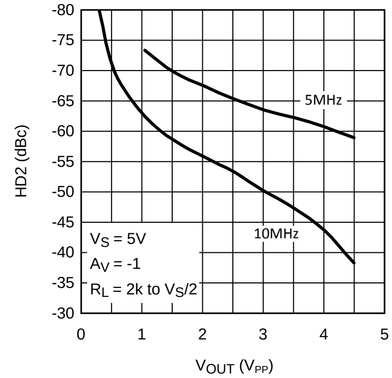
Typical Performance Characteristics (continued)

At T_J = 25°C, V^+ = +5, V^- = −5V, R_F = R_L = 2kΩ. Unless otherwise specified.

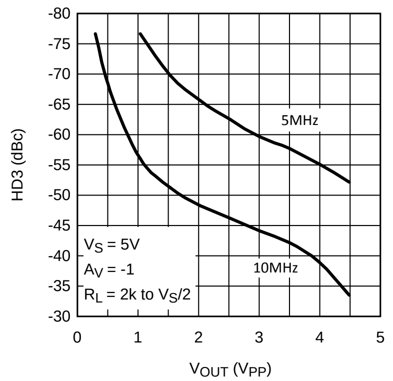
Open Loop Gain/Phase for Various Temperature



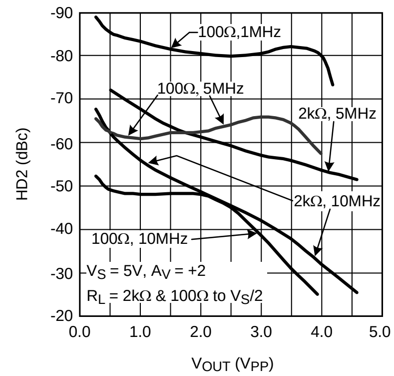
HD2 (dBc) vs. Output Swing



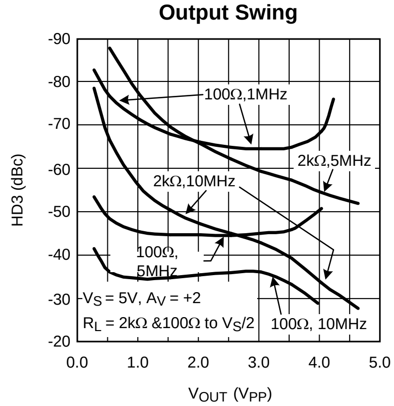
HD3 (dBc) vs. Output Swing



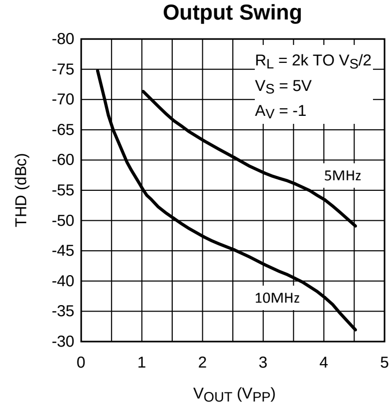
HD2 vs. Output Swing



HD3 vs. Output Swing



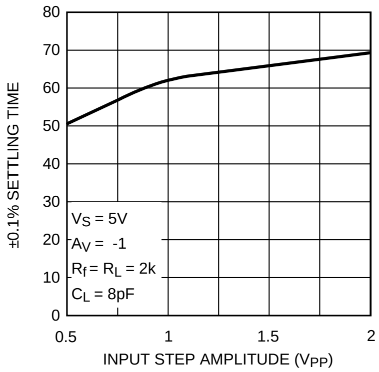
THD (dBc) vs. Output Swing



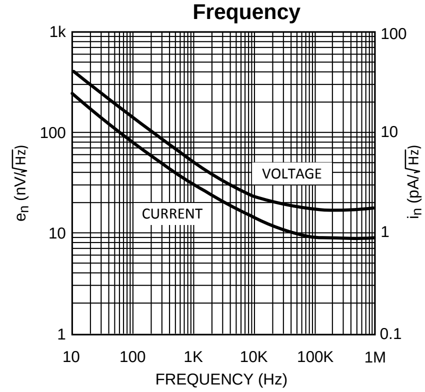
Typical Performance Characteristics (continued)

At T_J = 25°C, V^+ = +5, V^- = −5V, R_F = R_L = 2kΩ. Unless otherwise specified.

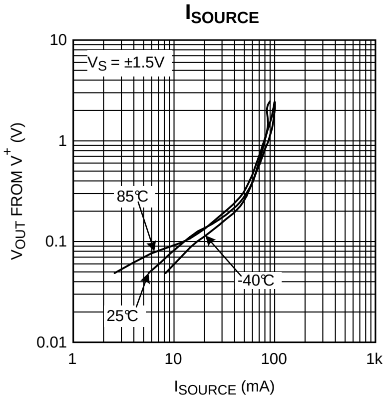
Settling Time vs. Input Step Amplitude (Output Slew and Settle Time)



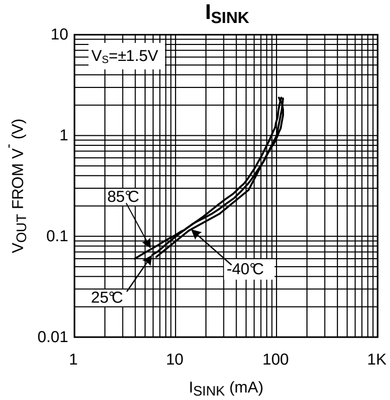
Input Noise vs. Frequency



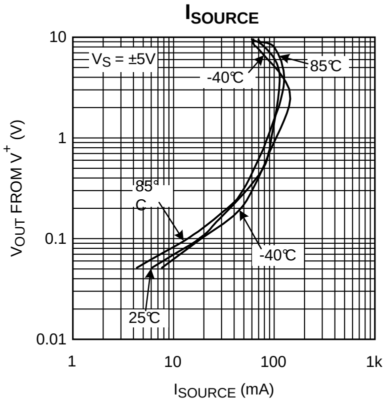
V_{OUT} from V^+ vs. I_{SOURCE}



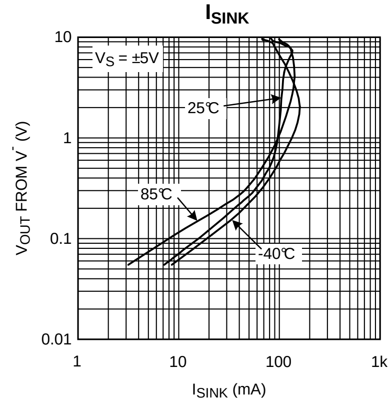
V_{OUT} from V^- vs. I_{SINK}



V_{OUT} from V^+ vs. I_{SOURCE}



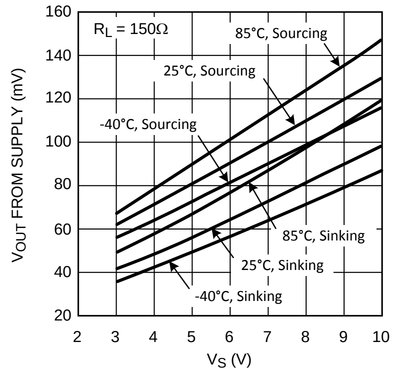
V_{OUT} from V^- vs. I_{SINK}



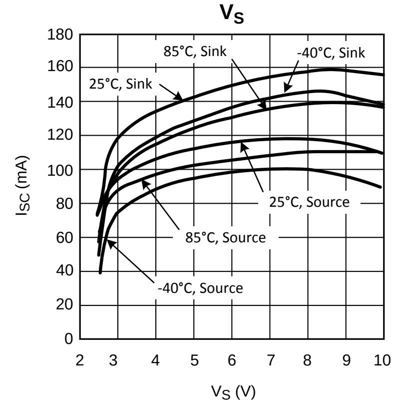
Typical Performance Characteristics (continued)

At T_J = 25°C, V^+ = +5, V^- = −5V, R_F = R_L = 2kΩ. Unless otherwise specified.

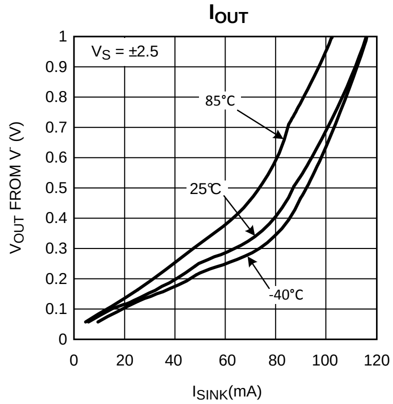
Swing vs. V_S



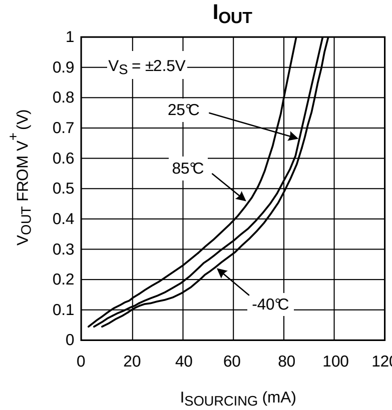
Short Circuit Current (to V_S/2) vs. V_S



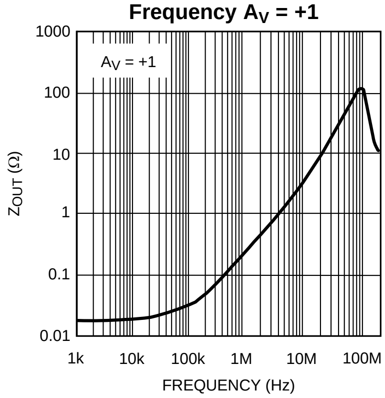
Output Sinking Saturation Voltage vs. I_{OUT}



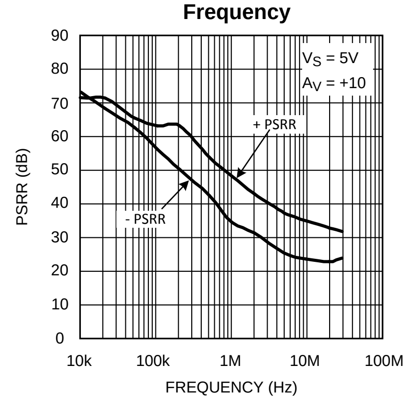
Output Sourcing Saturation Voltage vs. I_{OUT}



Closed Loop Output Impedance vs. Frequency A_V = +1



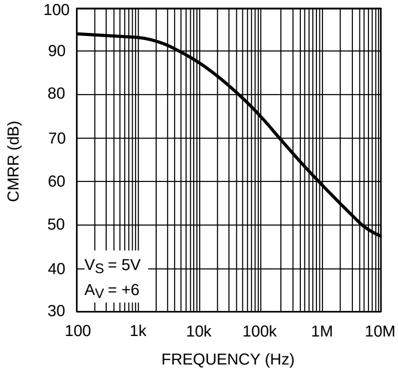
PSRR vs. Frequency



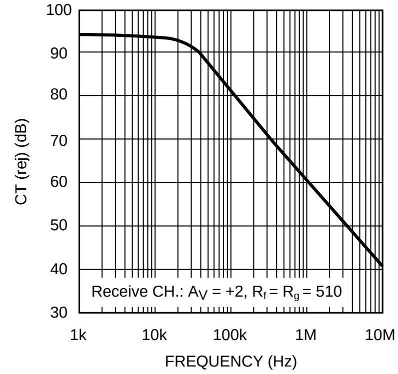
Typical Performance Characteristics (continued)

At T_J = 25°C, V^+ = +5, V^- = −5V, R_F = R_L = 2kΩ. Unless otherwise specified.

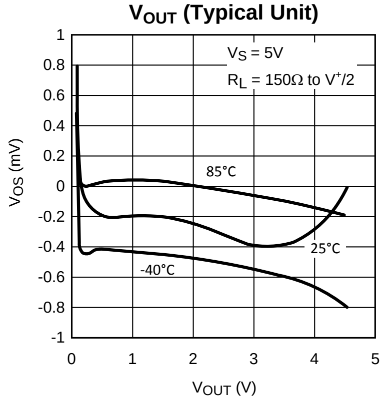
CMRR vs. Frequency



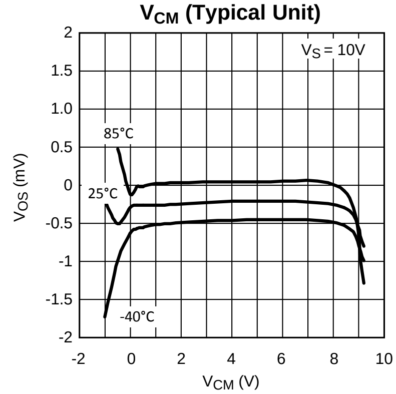
Crosstalk Rejection vs. Frequency (Output to Output)



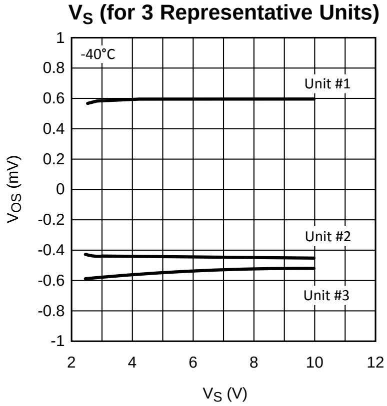
V_{OS} vs. V_{OUT} (Typical Unit)



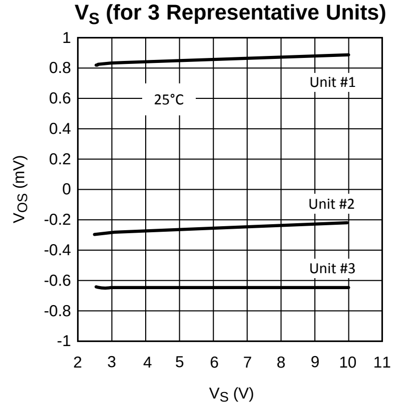
V_{OS} vs. V_{CM} (Typical Unit)



V_{OS} vs. V_S (for 3 Representative Units)



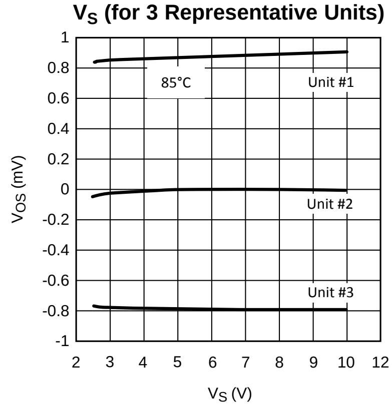
V_{OS} vs. V_S (for 3 Representative Units)



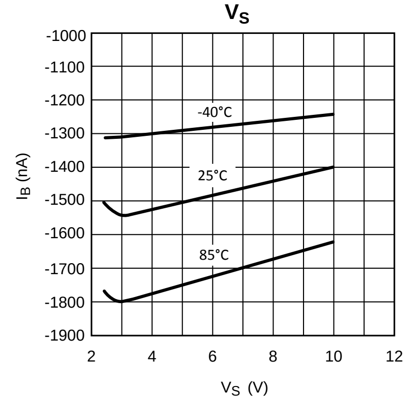
Typical Performance Characteristics (continued)

At T_J = 25°C, V^+ = +5, V^- = −5V, R_F = R_L = 2kΩ. Unless otherwise specified.

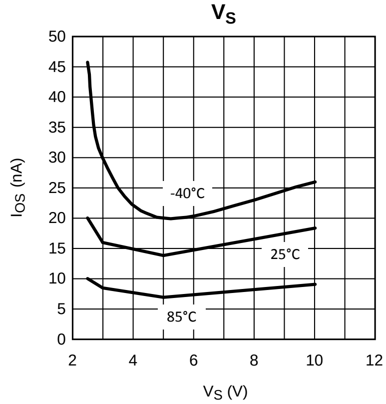
V_{OS} vs. V_S (for 3 Representative Units)



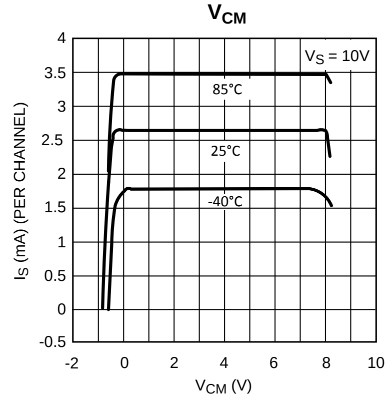
I_B vs. V_S



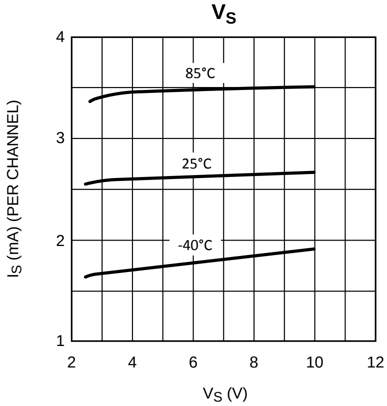
I_{OS} vs. V_S



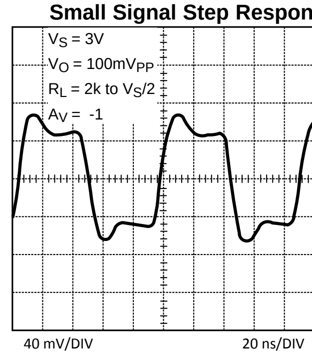
I_S vs. V_{CM}



I_S vs. V_S



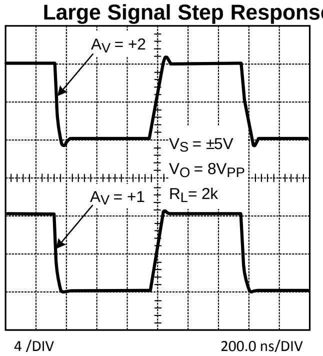
Small Signal Step Response



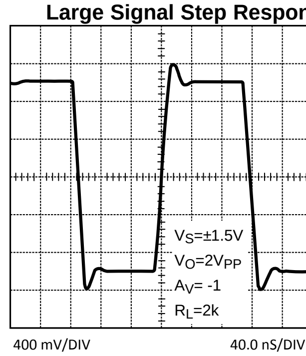
Typical Performance Characteristics (continued)

At T_J = 25°C, V^+ = +5, V^- = −5V, R_F = R_L = 2kΩ. Unless otherwise specified.

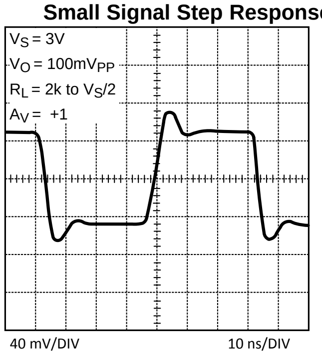
Large Signal Step Response



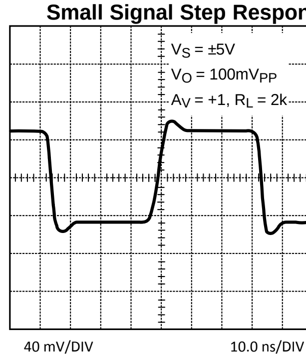
Large Signal Step Response



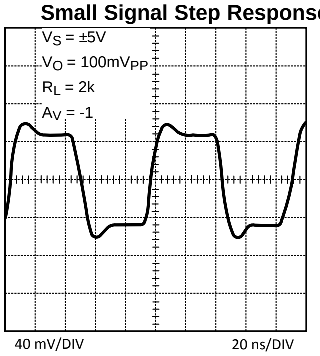
Small Signal Step Response



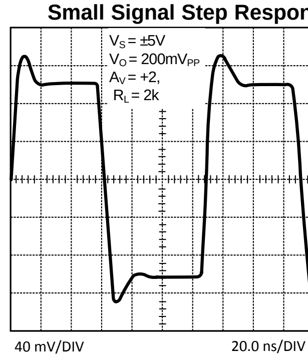
Small Signal Step Response



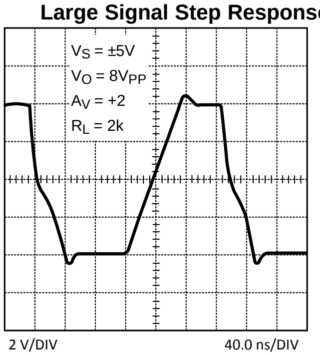
Small Signal Step Response



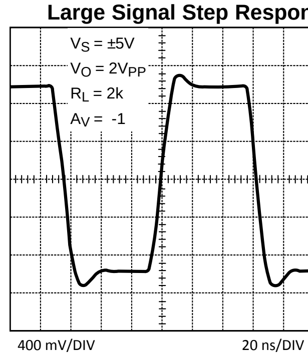
Small Signal Step Response



Large Signal Step Response



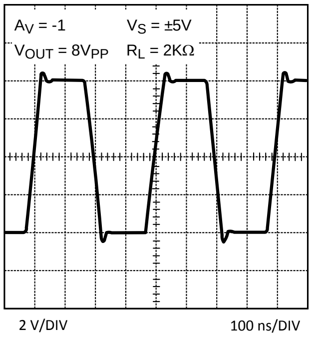
Large Signal Step Response



Typical Performance Characteristics (continued)

At T_J = 25°C, V^+ = +5, V^- = −5V, R_F = R_L = 2kΩ. Unless otherwise specified.

Large Signal Step Response



Application Notes

CIRCUIT DESCRIPTION

The LMH664XEP family is based on National Semiconductor's proprietary VIP10 dielectrically isolated bipolar process.

This device family architecture features the following:

- Complimentary bipolar devices with exceptionally high f_t (~8GHz) even under low supply voltage (2.7V) and low bias current.
- A class A-B "turn-around" stage with improved noise, offset, and reduced power dissipation compared to similar speed devices (patent pending).
- Common Emitter push-push output stage capable of 75mA output current (at 0.5V from the supply rails) while consuming only 2.7mA of total supply current per channel. This architecture allows output to reach within milli-volts of either supply rail.
- Consistent performance from any supply voltage (3V-10V) with little variation with supply voltage for the most important specifications (e.g. BW, SR, I_{OUT}, etc.)
- Significant power saving (~40%) compared to competitive devices on the market with similar performance.

Application Hints

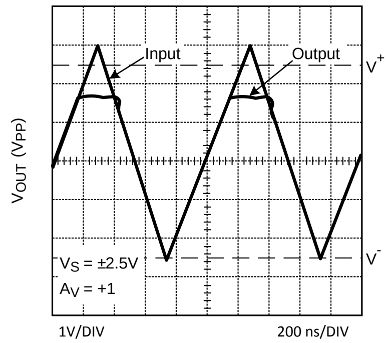
This Op Amp family is a drop-in replacement for the AD805X family of high speed Op Amps in most applications. In addition, the LMH664XEP will typically save about 40% on power dissipation, due to lower supply current, when compared to competition. All AD805X family's guaranteed parameters are included in the list of LMH664XEP guaranteed specifications in order to ensure equal or better level of performance. However, as in most high performance parts, due to subtleties of applications, it is strongly recommended that the performance of the part to be evaluated is tested under actual operating conditions to ensure full compliance to all specifications.

With 3V supplies and a common mode input voltage range that extends 0.5V below V^-, the LMH664XEP find applications in low voltage/low power applications. Even with 3V supplies, the −3dB BW (@ A_V = +1) is typically 115MHz with a tested limit of 80MHz. Production testing guarantees that process variations with not compromise speed. High frequency response is exceptionally stable confining the typical -3dB BW over the industrial temperature range to ±2.5%.

As can be seen from the typical performance plots, the LMH664XEP output current capability (~75mA) is enhanced compared to AD805X. This enhancement, increases the output load range, adding to the LMH664XEP's versatility.

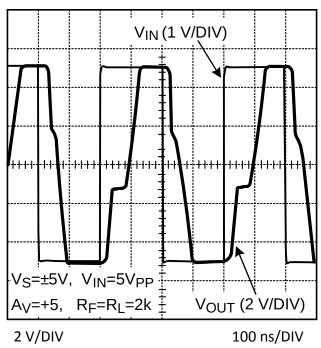
Because of the LMH664XEP's high output current capability attention should be given to device junction temperature in order not to exceed the Absolute Maximum Rating.

This device family was designed to avoid output phase reversal. With input overdrive, the output is kept near supply rail (or as closed to it as mandated by the closed loop gain setting and the input voltage). See:



However, if the input voltage range of −0.5V to 1V from V^+ is exceeded by more than a diode drop, the internal ESD protection diodes will start to conduct. The current in the diodes should be kept at or below 10mA.

Output overdrive recovery time is less than 100ns as can be seen from the following plot:



SINGLE SUPPLY, LOW POWER PHOTODIODE AMPLIFIER

The circuit shown is used to amplify the current from a photo-diode into a voltage output. In this circuit, the emphasis is on achieving high bandwidth and the transimpedance gain setting is kept relatively low. Because of its high slew rate limit and high speed, the LMH664XEP family lends itself well to such an application.

This circuit achieves approximately 1V/mA of transimpedance gain and capable of handling up to $1mA_{pp}$ from the photodiode. Q1, in a common base configuration, isolates the high capacitance of the photodiode (C_d) from the Op Amp input in order to maximize speed. Input is AC coupled through C1 to ease biasing and allow single supply operation. With 5V single supply, the device input/output is shifted to near half supply using a voltage divider from V_{CC}. Note that Q1 collector does not have any voltage swing and the Miller effect is minimized. D1, tied to Q1 base, is for temperature compensation of Q1's bias point. Q1 collector current was set to be large enough to handle the peak-to-peak photodiode excitation and not too large to shift the U1 output too far from mid-supply.

No matter how low an R_f is selected, there is a need for C_f in order to stabilize the circuit. The reason for this is that the Op Amp input capacitance and Q1 equivalent collector capacitance together (C_{IN}) will cause additional phase shift to the signal fed back to the inverting node. C_f will function as a zero in the feedback path counter-acting the effect of the C_{IN} and acting to stabilized the circuit. By proper selection of C_f such that the Op Amp open loop gain is equal to the inverse of the feedback factor at that frequency, the response is optimized with a theoretical 45° phase margin.

$$C_F = \sim \text{SQRT}\left[(C_{IN})/(2\pi \cdot GBWP \cdot R_F)\right] \quad (1)$$

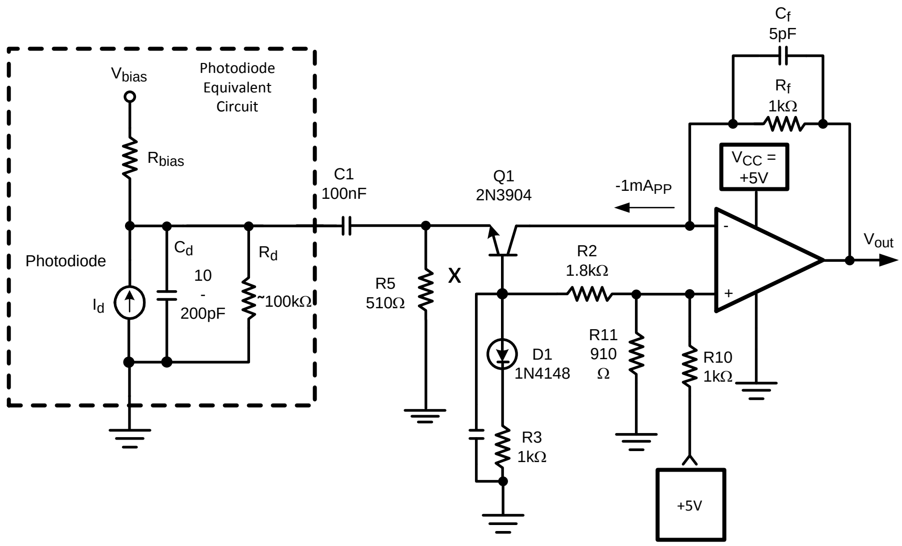
where GBWP is the Gain Bandwidth Product of the Op Amp

Optimized as such, the I-V converter will have a theoretical pole, f_p, at:

$$f_P = \text{SQRT}\left[GBWP/(2\pi R_F \cdot C_{IN})\right] \quad (2)$$

With Op Amp input capacitance of 3pF and an estimate for Q1 output capacitance of about 3pF as well, C_{IN} = 6pF. From the typical performance plots, LMH6642EP/6643EP family GBWP is approximately 57MHz. Therefore, with R_f = 1k, from Equation 1 and 2 above.

C_f = ~4.1pF, and f_p = 39MHz



For this example, optimum C_f was empirically determined to be around 5pF. This time domain response is shown in Figure 5 below showing about 9ns rise/fall times, corresponding to about 39MHz for f_p. The overall supply current from the +5V supply is around 5mA with no load.

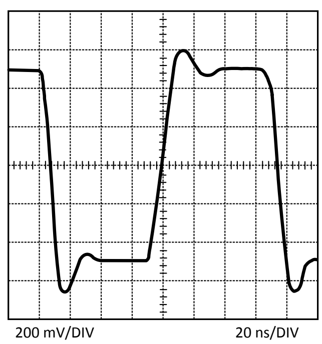


Figure 5.

PRINTED CIRCUIT BOARD LAYOUT AND COMPONENT VALUES SECTIONS

Generally, a good high frequency layout will keep power supply and ground traces away from the inverting input and output pins. Parasitic capacitances on these nodes to ground will cause frequency response peaking and possible circuit oscillations (see Application Note OA-15 for more information). National Semiconductor suggests the following evaluation boards as a guide for high frequency layout and as an aid in device testing and characterization:

Device	Package	Evaluation Board PN
LMH6642MF	SOT23-5	CLC730068
LMH6642MF	8-Pin SOIC	CLC730027
LMH6643MA	8-Pin SOIC	CLC730036
LMH6643MA	8-Pin MSOP	CLC730123
LMH6644MA	14-Pin SOIC	CLC730031
LMH6644MA	14-Pin TSSOP	CLC730131

These free evaluation boards are shipped when a device sample request is placed with National Semiconductor.

Another important parameter in working with high speed/high performance amplifiers, is the component values selection. Choosing external resistors that are large in value will effect the closed loop behavior of the stage because of the interaction of these resistors with parasitic capacitances. These capacitors could be inherent to the device or a by-product of the board layout and component placement. Either way, keeping the resistor values lower, will diminish this interaction to a large extent. On the other hand, choosing very low value resistors could load down nodes and will contribute to higher overall power dissipation.

IMPORTANT NOTICE

Products		**Applications**	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
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Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
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