

LMH6881 DC to 2.4GHz, High Linearity, Programmable Differential Amplifier

Check for Samples: [LMH6881](#)

FEATURES

- **Small Signal Bandwidth: 2400MHz**
- **OIP3 @ 100 MHz: 44dBm**
- **HD3 @ 100 MHz: -100dBc**
- **Noise Figure: 9.7dB**
- **Voltage Gain Range: 26dB to 6dB**
- **Voltage Gain Step Size 0.25dB**
- **Input Impedance 100Ω**
- **Parallel and Serial Gain Control**
- **Power Down Capability**

APPLICATIONS

- **Oscilloscope Front End**
- **Spectrum Analyzer Gain Block**
- **Differential ADC Driver**
- **Differential Cable Driver**
- **IF / RF and Baseband Gain Blocks**
- **Medical Imaging**

DESCRIPTION

The LMH6881 is a high-speed, high-performance, programmable differential amplifier. With a bandwidth of 2.4GHz and high linearity of 44dBm OIP3, the LMH6881 is suitable for a wide variety of signal conditioning applications.

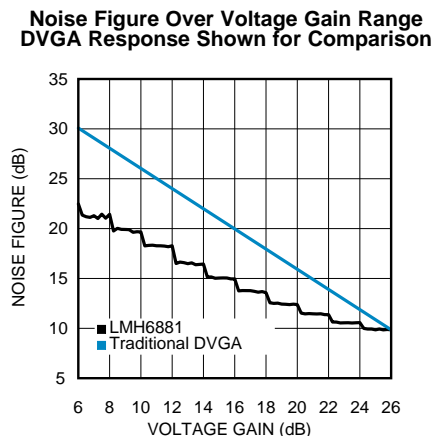
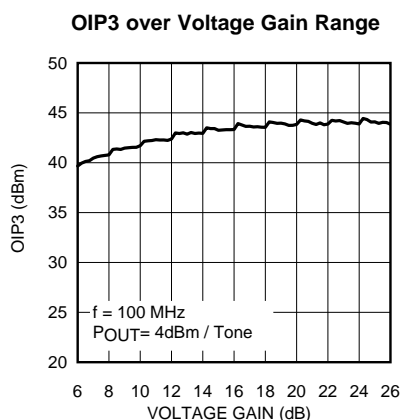
The LMH6881 programmable differential amplifier family combines the best of both fully differential amplifiers and variable gain amplifiers. It offers superior noise and distortion performance over the entire gain range without external resistors, enabling the use of just one device and one design for multiple applications requiring different gain settings.

The LMH6881 is an easy-to-use amplifier that can replace both fully differential, fixed gain amplifiers as well as variable gain amplifiers. The LMH6881 requires no external gain-setting components and supports gain settings from 6dB to 26dB with small, accurate 0.25dB gain steps. With an input impedance of 100 Ohms the LMH6881 is easy to drive from a variety of sources such as mixers or filters. The LMH6881 also supports 50 Ohm single ended signal sources and supports both DC- and AC-coupled applications.

Parallel gain control allows the LMH6881 to be soldered down in a fixed gain so that no control circuit is required. If dynamic gain control is desired, the LMH6881 can be changed with SPI compatible serial commands or with the parallel pins.

The LMH6881 is fabricated in TI's CBiCMOS8 proprietary complementary silicon germanium process and is available in a space saving, thermally enhanced 24-pin Lead Quad WQFN package. The same amplifier is offered in a dual package as the LMH6882.

Performance Curves



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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings⁽¹⁾⁽²⁾

ESD Tolerance ⁽³⁾	Human Body Model	1 kV
	Charged Device Model	250V
Positive Supply Voltage (VCC)		–0.6V to 5.5V
Differential Voltage between Any Two Grounds		<200 mV
Analog Input Voltage Range		–0.6V to 5.5V
Digital Input Voltage Range		–0.6V to 5.5V
Output Short Circuit Duration (one pin to ground)		Infinite
Junction Temperature		+150°C
Storage Temperature Range		–65°C to +150°C
Soldering Information	Infrared or Convection (30 sec)	260°C

- (1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications, see the Electrical Characteristics table.
- (2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
- (3) Human Body Model, applicable std. MIL-STD-883, Method 3015.7. Machine Model, applicable std. JESD22-A115-A (ESD MM std. of JEDEC) Field-Induced Charge-Device Model, applicable std. JESD22-C101-C (ESD FICDM std. of JEDEC).

Operating Ratings⁽¹⁾

Supply Voltage (VCC)			4.75V to 5.25V
Differential Voltage Between Any Two Grounds			<10 mV
Analog Input Voltage Range, AC Coupled			0V to VCC
Temperature Range ⁽²⁾			–40°C to +85°C
Package Thermal Resistance ⁽³⁾	24–pin WQFN	(θ_{JA})	53°C/W
		(θ_{JC})	6°C/W

- (1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications, see the Electrical Characteristics table.
- (2) The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA} and the ambient temperature T_A . The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A) / \theta_{JA}$. All numbers apply for packages soldered directly onto a PC Board.
- (3) Junction to ambient (θ_{JA}) thermal resistance measured on JEDEC 4 layer board. Junction to case (θ_{JC}) thermal resistance measured at exposed thermal pad; package is not mounted to any PCB.

5V Electrical Characteristics⁽¹⁾⁽²⁾⁽³⁾

The following specifications apply for single supply with VCC = 5V, Maximum Gain (26dB), R_L = 200Ω, f_{in} = 100 MHz.

Boldface limits apply at temperature extremes.

Symbol	Parameter	Conditions	Min ⁽⁴⁾	Typ ⁽⁵⁾	Max ⁽⁴⁾	Units
Dynamic Performance						
3dBBW	–3dB Bandwidth	V _{OUT} = 2 V _{PPD}		2.4		GHz
NF	Noise Figure	Source Resistance (R _s) = 100Ω		9.7		dB
OIP3	Output Third Order Intercept Point ⁽⁶⁾	f = 100 MHz, P _{OUT} = 4 dBm per tone, tone spacing = 1 MHz		44		dBm
		f = 200 MHz, P _{OUT} = 4 dBm per tone, tone spacing = 2 MHz		42		
OIP2	Output Second Order Intercept Point	P _{OUT} = 4 dBm per Tone, f ₁ = 112.5 MHz, f ₂ = 187.5 MHz		76		dBm
IMD3	Third Order Intermodulation Products	f = 100 MHz, P _{OUT} = 4 dBm per tone, tone spacing = 1 MHz		–80		dBc
		f = 200 MHz, P _{OUT} = 4 dBm per tone, tone spacing = 2 MHz		–76		
P1dB	1dB Compression Point	Output Power		17		dBm
HD2	Second Order Harmonic Distortion	f = 200 MHz, P _{OUT} = 4dBm		–65		dBc
HD3	Third Order Harmonic Distortion	f = 200 MHz, P _{OUT} = 4dBm		–74		dBc
CMRR	Common Mode Rejection Ratio ⁽⁷⁾	Pin = –15 dBm, f = 100 MHz		–40		dBc
Analog I/O						
R _{IN}	Input Resistance	Differential, INPD to INMD		100		Ω
R _{IN}	Input Resistance	Single Ended, INPS or INPD, 50Ω termination on unused input		50		Ω
V _{ICM}	Input Common Mode Voltage	Self Biased		2.5		V
	Maximum Input Voltage Swing	Volts peak to peak, differential		2.85		V _{PPD}
	Maximum Differential Output Voltage Swing	Differential, f < 10MHz		6		V _{PPD}
R _{OUT}	Output Resistance	Differential, f = 100MHz		0.4		Ω
Gain Parameters						
	Maximum Voltage Gain	Parallel Inputs (INPD and INMD), R _s = 100Ω		26		dB
		Single ended input (INMS or INPS), 50Ω R _s and 50Ω termination on unused input.		26.6		
	Minimum Gain	Parallel Inputs, R _s = 100Ω		6		dB
	Gain Steps	Available using SPI interface		80		
		Available using parallel interface		10		
	Gain Step Size	Available using SPI interface		0.25		dB
		Available using parallel interface		2		
	Gain Step Error	Any two adjacent steps over entire range		±0.125		dB
	Gain Step Phase Shift	Any two adjacent steps over entire range		±3		Degrees

- (1) Electrical Table values apply only for factory testing conditions at the temperature indicated. No guarantee of parametric performance is indicated in the electrical tables under conditions different than those tested
- (2) Negative input current implies current flowing out of the device.
- (3) Drift determined by dividing the change in parameter at temperature extremes by the total temperature change.
- (4) Limits are 100% production tested at 25°C. Limits over the operating temperature range are guaranteed through correlation using Statistical Quality Control (SQC) methods.
- (5) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not guaranteed on shipped production material.
- (6) OIP3 is the third order intermodulation intercept point. In this datasheet OIP3 numbers are single power measurements where OIP3 = IMD3 / 2 + P_{OUT} (per tone). OIP2 is the second order intercept point where OIP2 = IMD2 + P_{OUT} (per tone). HD2 is the second order harmonic distortion and is a single tone measurement. HD3 is the third order harmonic distortion and is a single tone measurement. Power measurements are made at the amplifier output pins.
- (7) CMRR is defined as the differential response at the output in response to a common mode signal at the input.

5V Electrical Characteristics⁽¹⁾⁽²⁾⁽³⁾ (continued)

The following specifications apply for single supply with VCC = 5V, Maximum Gain (26dB), R_L = 200Ω, f_{in} = 100 MHz.

Boldface limits apply at temperature extremes.

Symbol	Parameter	Conditions	Min ⁽⁴⁾	Typ ⁽⁵⁾	Max ⁽⁴⁾	Units
	Gain Step Switching Time			20		ns
	Enable/ Disable Time	Settled to 90% level		15		ns
Power Requirements						
ICC	Supply Current			100	135	mA
P	Power			0.5		W
ICCD	Disabled Supply Current			15		mA
All Digital Inputs						
	Logic Compatibility	TTL, 2.5V CMOS, 3.3V CMOS, 5V CMOS				
VIL	Logic Input Low Voltage			0.4		V
VIH	Logic Input High Voltage			2.0-5.0		V
IIH	Logic Input High Input Current			–9		μA
IIL	Logic Input Low Input Current			–47		μA
Parallel Mode Timing						
t _{GS}	Setup Time			3		ns
t _{GH}	Hold Time			3		ns
Serial Mode						
f _{CLK}	SPI Clock Frequency	50% duty cycle	10	50		MHz

CONNECTION DIAGRAM

24-Pin WQFN

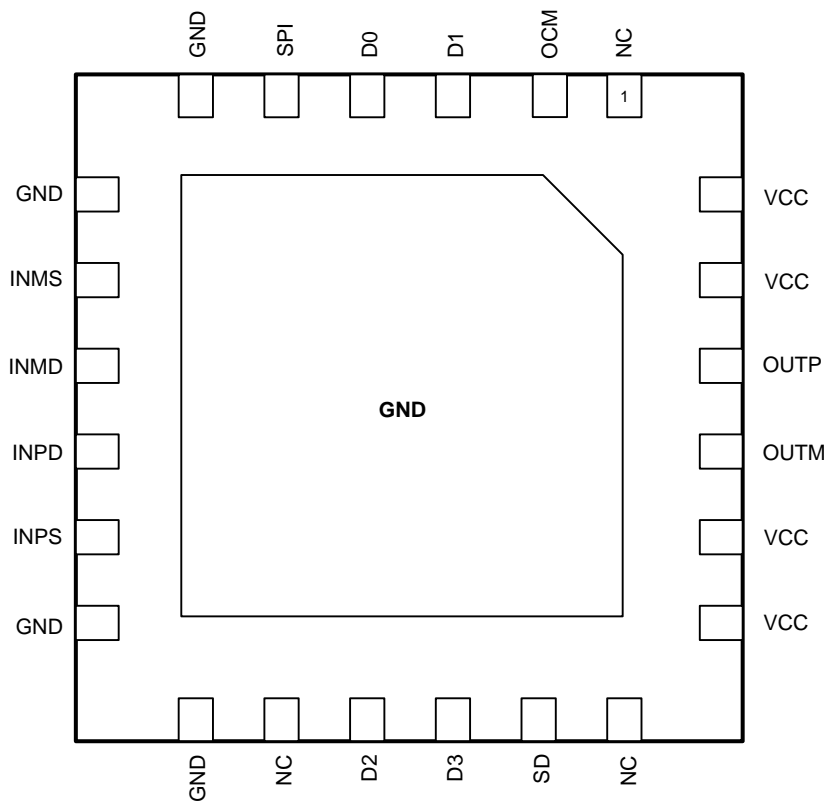


Figure 1. Top View

PIN DESCRIPTIONS

Pin Number	Symbol	Pin Category	Description
Analog I/O			
9, 10	INPD, INMD	Analog Input	Differential inputs 100Ω
8, 11	INPS, INMS	Analog Input	Single ended inputs 50Ω
21, 22	OUTP, OUTM	Analog Output	Differential outputs, low impedance
Power			
6, 7, 12, 13	GND	Ground	Ground pins. Connect to low impedance ground plane. All pin voltages are specified with respect to the voltage on these pins. The exposed thermal pad is internally bonded to the ground pins.
19, 20, 23, 24	VCC	Power	Power supply pins. Valid power supply range is 4.75V to 5.25V.
Exposed Center Pad		Thermal/ Ground	Thermal management/ Ground
Digital Inputs			
5	SPI	Digital Input	0 = Parallel Mode, 1 = Serial Mode
Parallel Mode Digital Pins, SPI= Logic Low			
3, 4, 15, 16	D0, D1, D2, D3	Digital Input	Attenuator control
17	SD	Digital Input	Shutdown 0 = amp on, 1 = amp off
Serial Mode Digital Pins, SPI= Logic High SPI™ Compatible			
4	SDO	Digital Output- Open Emitter	Serial Data Output (Requires external bias.)
3	SDI	Digital Input	Serial Data In
16	CS	Digital Input	Chip Select (active low)
15	CLK	Digital Input	Clock

Pin List

Pin	Description	Pin
1	NC	
2	OCM	Output Common Mode, gain of 2
3	D1, SDI	Parallel mode = Logic control signal, position 1 or weight 2 ¹ SPI mode = serial data in (SDI)
4	D0, SDO	Parallel mode = Logic control signal, position 0 or weight 2 ⁰ SPI mode = serial data out (SDO)
5	SPI	Serial mode control
6	GND	Ground
7	GND	Ground
8	INMS	Amplifier single ended input minus swing (negative)
9	INMD	Amplifier differential input minus swing (negative)
10	INPD	Amplifier differential input plus swing (positive)
11	INPS	Amplifier single ended input plus swing (positive)
12	GND	Ground
13	GND	Ground
14	NC	
15	D2	Parallel mode = Logic control signal, position 2 or weight 2 ² SPI mode = serial clock (CLK)
16	D3	Parallel mode = Logic control signal, position 3 or weight 2 ³ SPI mode = chip select (CS)
17	SD	Device Shutdown
18	NC	
19	VCC	Power supply nominal value of 5V
20	VCC	Power supply nominal value of 5V

Pin List (continued)

Pin	Description	Pin
21	OUTM	Amplifier output minus (negative)
22	OUTP	Amplifier output plus (positive)
23	VCC	Power supply nominal value of 5V
24	VCC	Power supply nominal value of 5V

Typical Performance Characteristics

(Unless otherwise specified, the following conditions apply: $T_A = 25^\circ\text{C}$, $V_{CC} = 5\text{V}$, $R_L = 200\Omega$, Maximum Gain, Differential Input). LMH6882 devices have been used for some typical performance plots.

**Frequency Response over Gain Range,
4dB Steps**

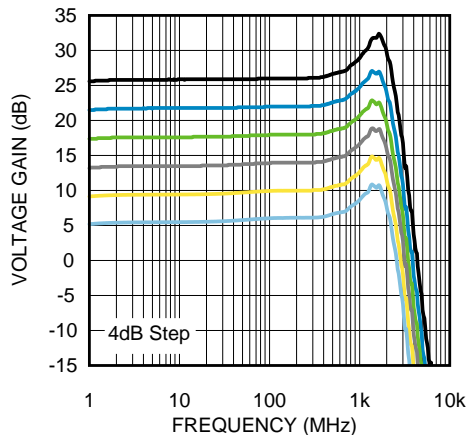


Figure 2.

OIP3 vs Voltage Gain

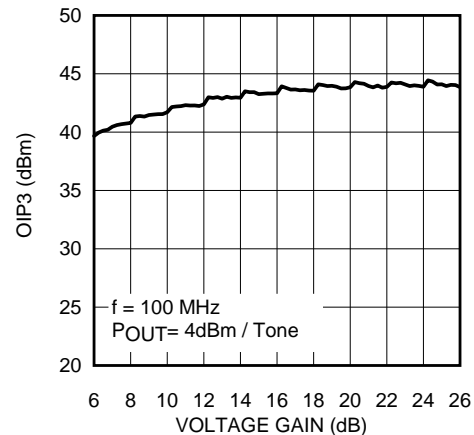


Figure 3.

OIP3 vs Output Power

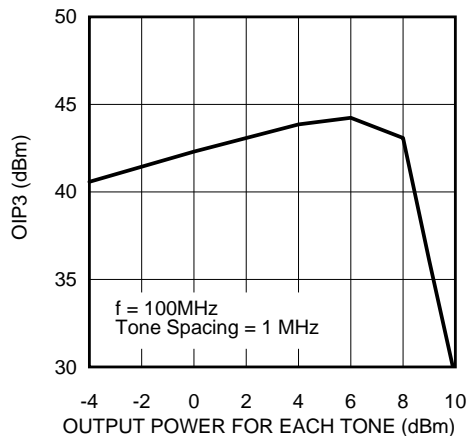


Figure 4.

Dynamic Range Figure vs Voltage Gain

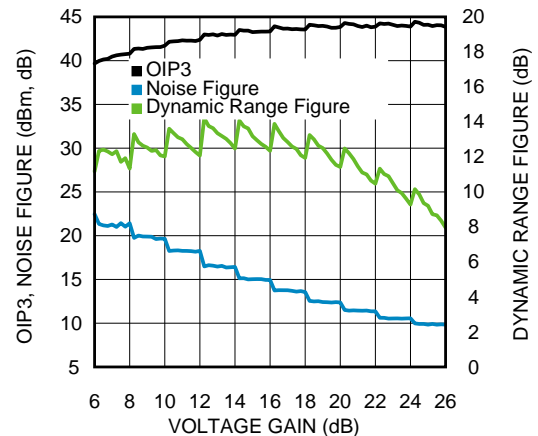


Figure 5.

OIP3 vs Frequency

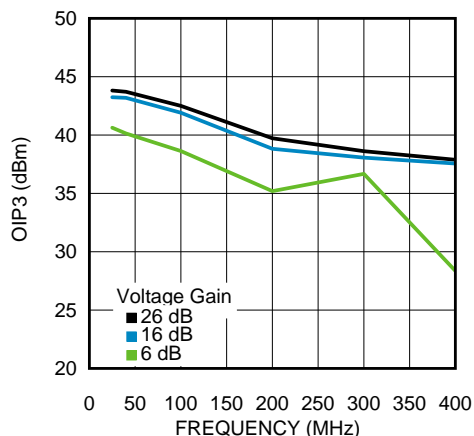


Figure 6.

OIP3 vs Supply Voltage

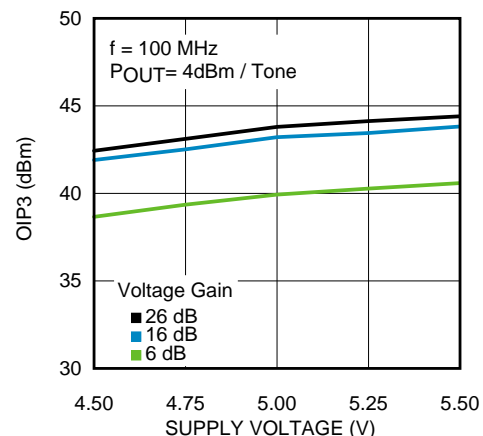


Figure 7.

Typical Performance Characteristics (continued)

(Unless otherwise specified, the following conditions apply: $T_A = 25^\circ\text{C}$, $V_{CC} = 5\text{V}$, $R_L = 200\Omega$, Maximum Gain, Differential Input). LMH6882 devices have been used for some typical performance plots.

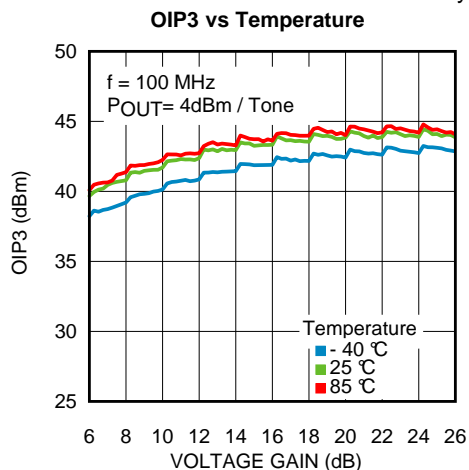


Figure 8.

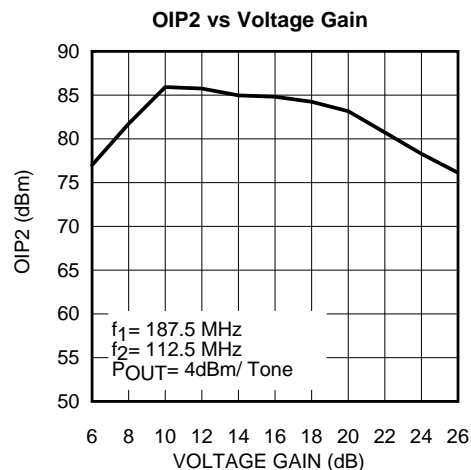


Figure 9.

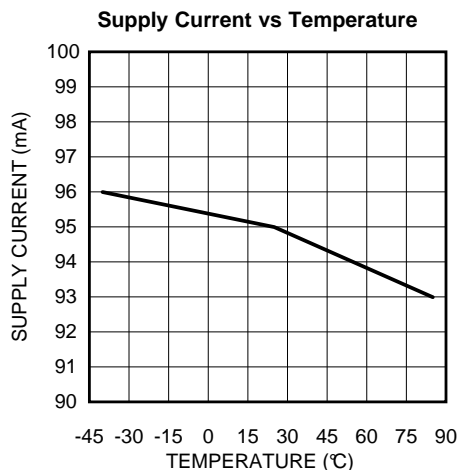


Figure 10.

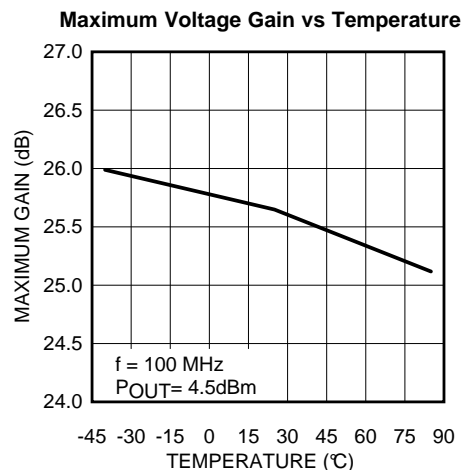


Figure 11.

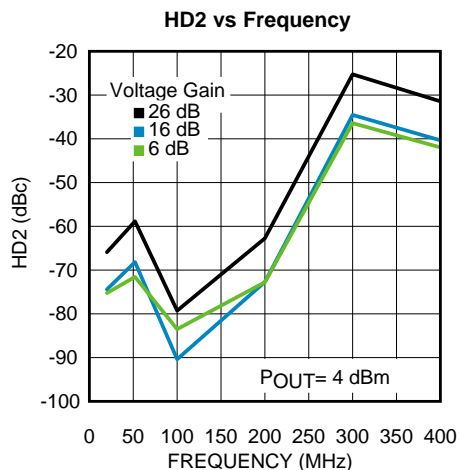


Figure 12.

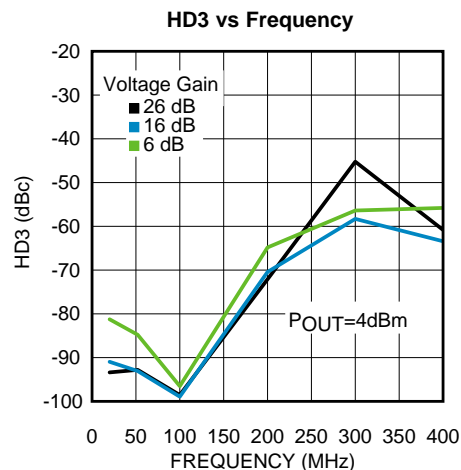


Figure 13.

Typical Performance Characteristics (continued)

(Unless otherwise specified, the following conditions apply: $T_A = 25^\circ\text{C}$, $V_{CC} = 5\text{V}$, $R_L = 200\Omega$, Maximum Gain, Differential Input). LMH6882 devices have been used for some typical performance plots.

HD2 & HD3 vs Voltage Gain

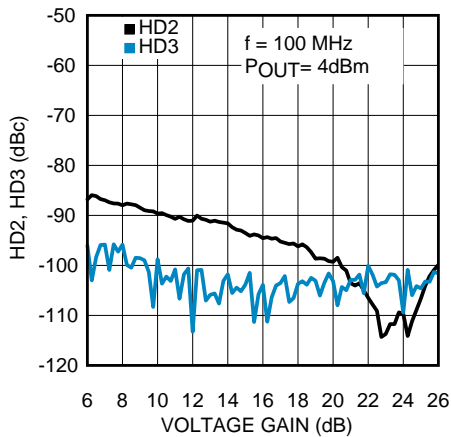


Figure 14.

HD2 vs Output Power

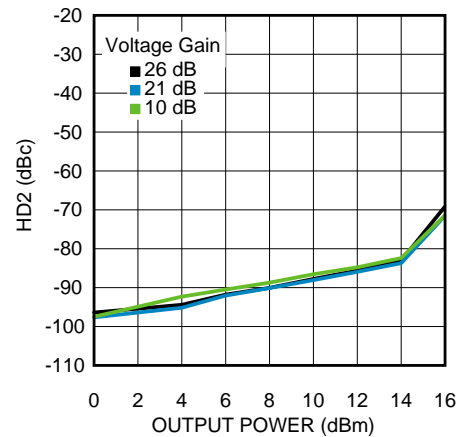


Figure 15.

HD3 vs Output Power

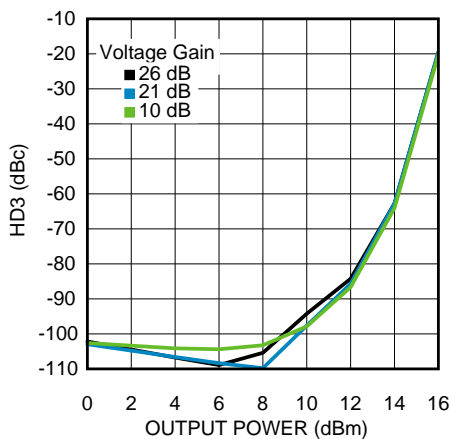


Figure 16.

Output Power vs Input Power

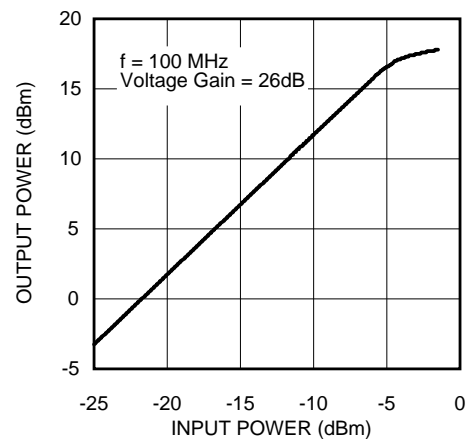


Figure 17.

Gain Step Amplitude Error

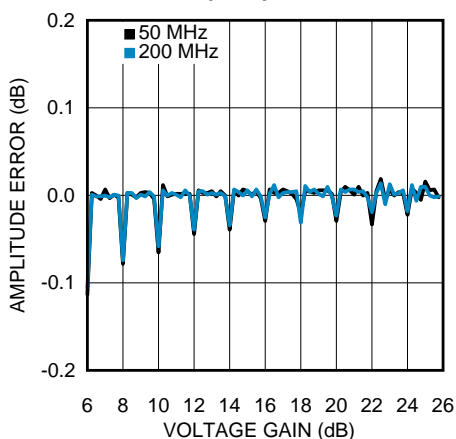


Figure 18.

Gain Step Phase Error

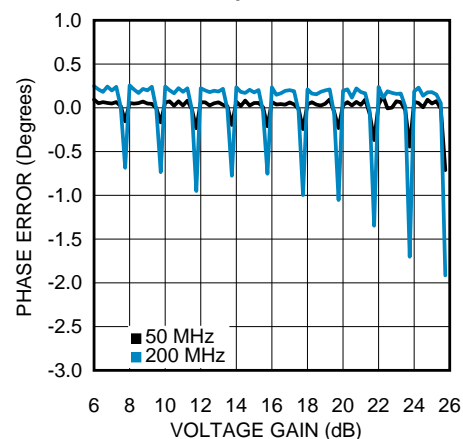


Figure 19.

Typical Performance Characteristics (continued)

(Unless otherwise specified, the following conditions apply: $T_A = 25^\circ\text{C}$, $V_{CC} = 5\text{V}$, $R_L = 200\Omega$, Maximum Gain, Differential Input). LMH6882 devices have been used for some typical performance plots.

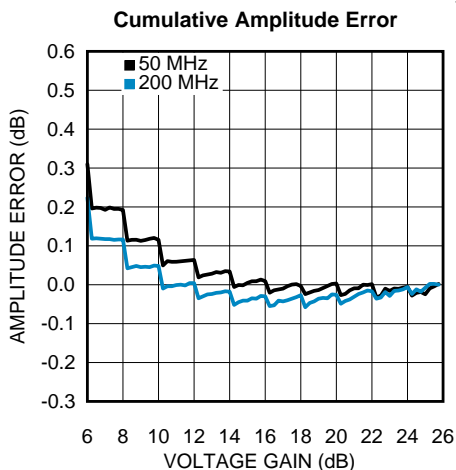


Figure 20.

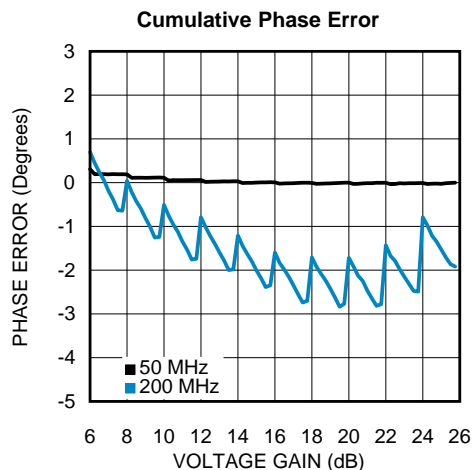


Figure 21.

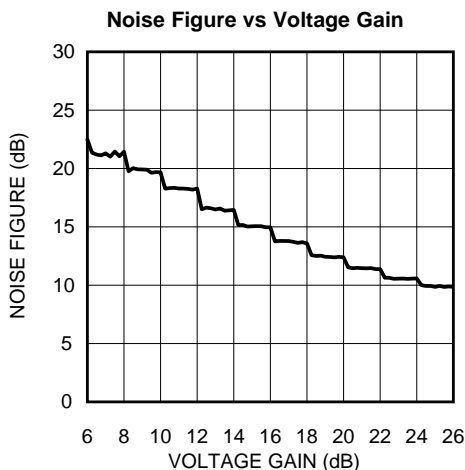


Figure 22.

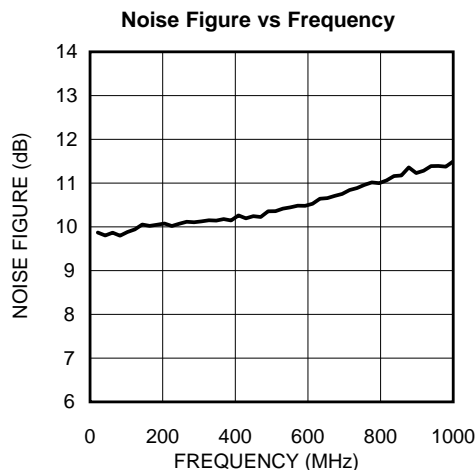


Figure 23.

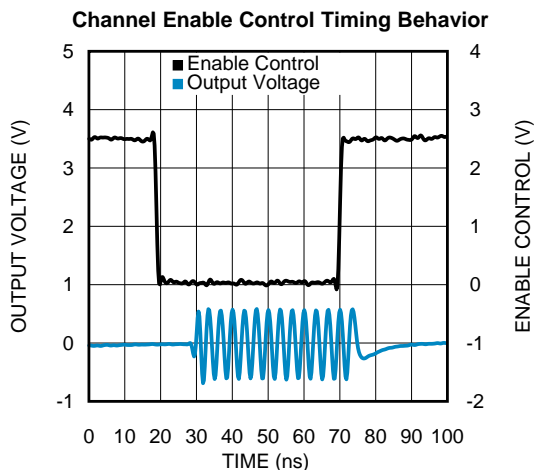


Figure 24.

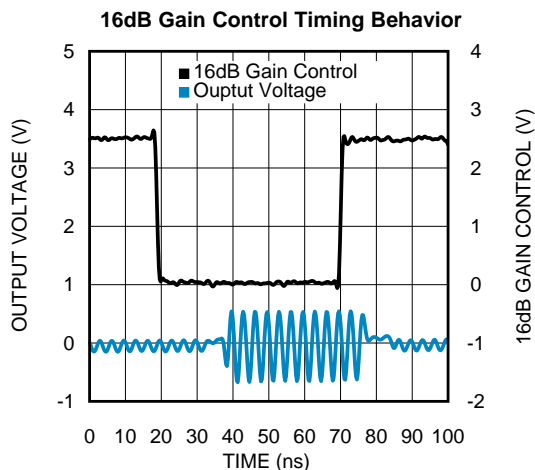


Figure 25.

Typical Performance Characteristics (continued)

(Unless otherwise specified, the following conditions apply: $T_A = 25^\circ\text{C}$, $V_{CC} = 5\text{V}$, $R_L = 200\Omega$, Maximum Gain, Differential Input). LMH6882 devices have been used for some typical performance plots.

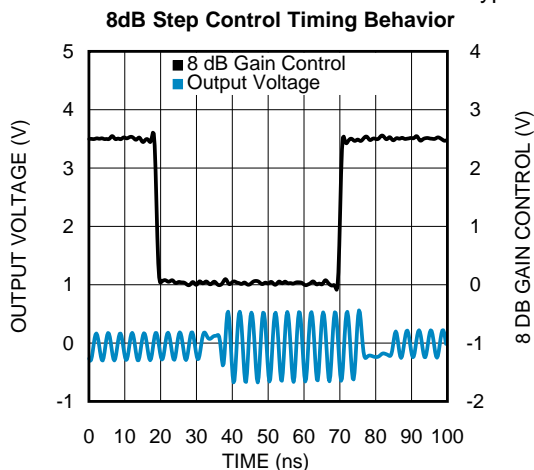


Figure 26.

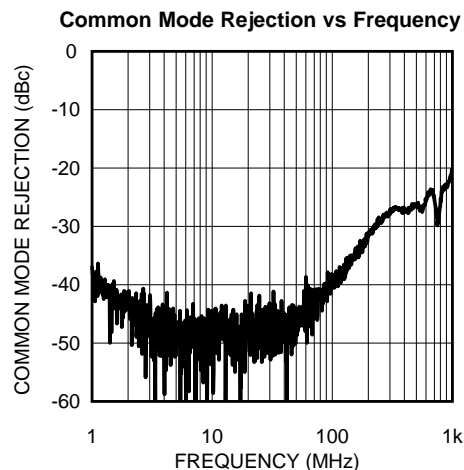


Figure 27.

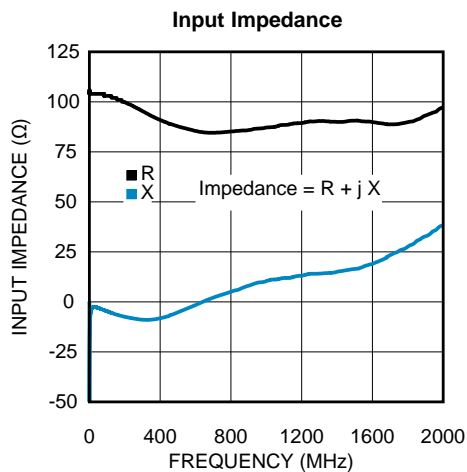


Figure 28.

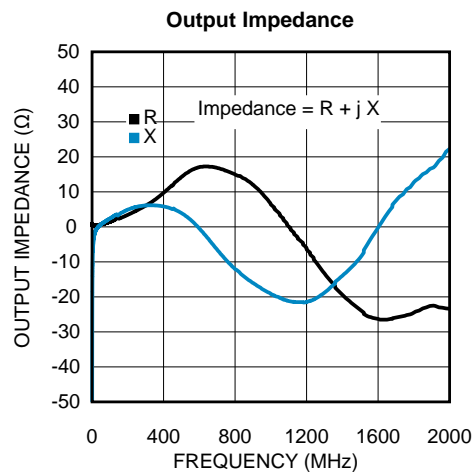


Figure 29.

Typical Performance Characteristics, Single Ended Input

(Unless otherwise specified, the following conditions apply: $T_A = 25^\circ\text{C}$, $V_{CC} = 5\text{V}$, $R_L = 200\Omega$, Maximum Gain.)

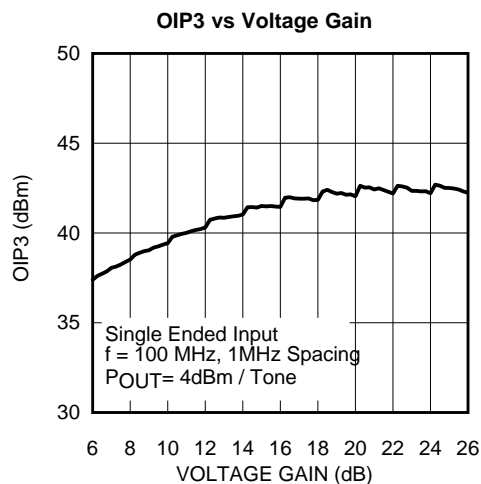


Figure 30.

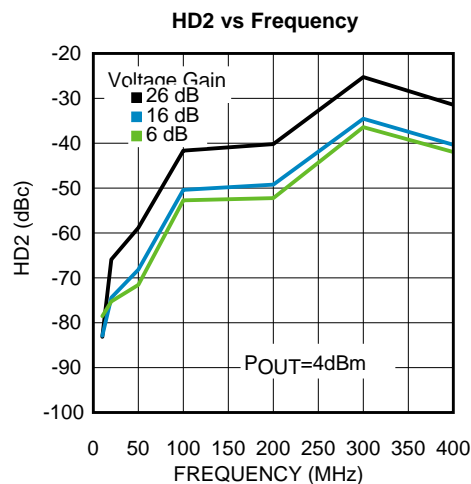


Figure 31.

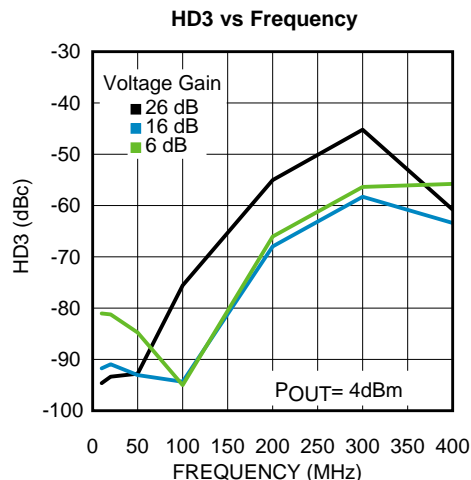


Figure 32.

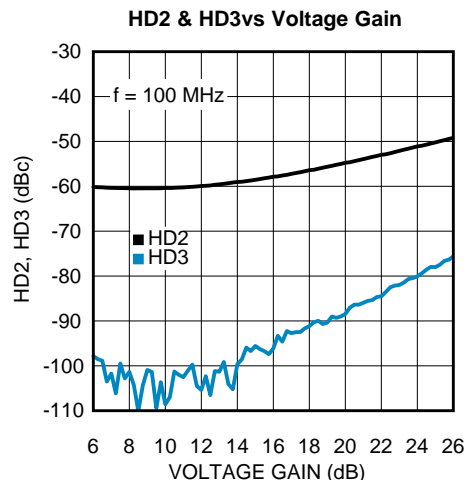


Figure 33.

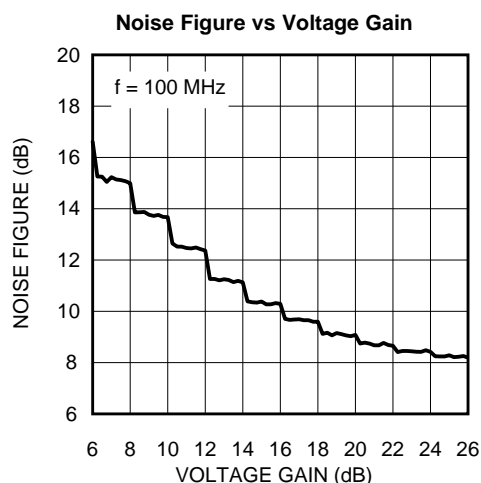


Figure 34.

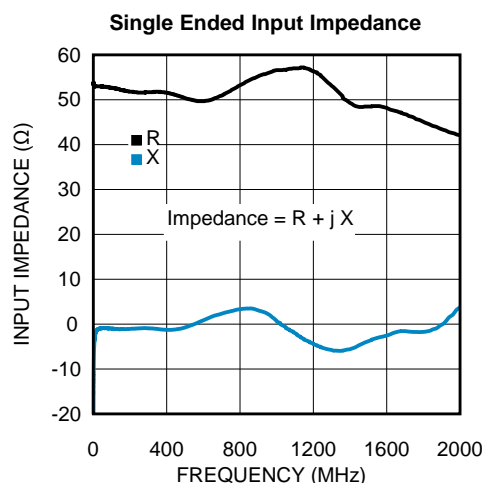


Figure 35.

APPLICATION INFORMATION

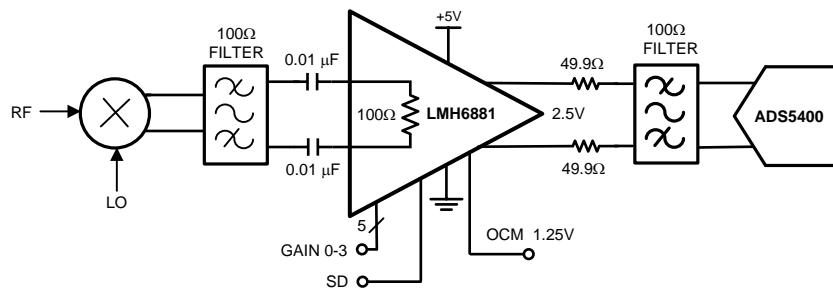


Figure 36. LMH6881 Typical Application

INTRODUCTION

The LMH6881 is a fully differential amplifier optimized for signal path applications up to 1000 MHz. The LMH6881 has a 100Ω input and a low impedance output. The gain is digitally controlled over a 20 dB range from 26dB to 6dB. The LMH6881 is designed to replace fixed gain differential amplifiers with a single, flexible gain device. It has been designed to provide good noise figure and OIP3 over the entire gain range. This design feature is highlighted by the Dynamic Range Figure (DRF). The DRF is defined as the input third order intercept point (IIP3) minus the noise figure (NF). Traditional variable gain amplifiers generally have the best OIP3 and NF performance at maximum gain only.

BASIC CONNECTIONS

A voltage between 4.75 V and 5.25 V should be applied to pins 19, 20, 23 and 24.. Each supply pin should be decoupled with a low inductance, surface-mount ceramic capacitor of 0.01μF as close to the device as possible. When vias are used to connect the bypass capacitors to a ground plane the vias should be used in pairs to help minimize parasitic inductance. Using pairs of bypass capacitors will also help reduce parasitic inductance between the amplifier power pins and ground.

The LMH6881 has internally terminated inputs. The INMD and INPD pins are intended to be the differential input pins and are terminated with a 100 Ohm differential resistor. The INMS and INPS pins are intended to be used for single ended inputs and have been designed to support single ended termination of 50 Ohms (active termination). If the single ended input pins are used for a differential signal the internal termination will appear to be a 36 Ohm differential load.

When using the LMH6881 differential input pins the unused single ended input pins should be left disconnected. Likewise when the single ended input pins are used the differential input pins should be left disconnected. Unused input pins should not be terminated or connected to ground.

The outputs of the LMH6881 need to be biased close to 2.5V for best performance. The common mode voltage of the output pins is set by the OCM pin. The OCM pin needs to be driven from an external, low noise source. There is a gain of 2 between the OCM pin and the output pins so that the OCM voltage should be close to 1.25V. The input pins are self biased to 2.5V. When using the LMH6881 for DC coupled applications make sure to keep the input and output common mode voltages close to the 2.5V requirement.

When using the LMH6881 in parallel mode the gain can be set in 2dB increments. If fixed gain is desired the pins can be strapped to ground or VCC as required. For finer gain control the LMH6881 supports SPI compliant digital control which allows the gain to be set in 0.25dB increments between 26dB and 6dB. The gain is defined as voltage gain. If power gain is required the source and load resistances need to be factored into the gain calculation.

The LMH6881 has a shutdown pin to enable power savings when the amplifier is not being used. For example, in a time division duplex (TDD) system the receiver may be shutdown during transmit to save power and to protect the receive analog to digital converter (ADC) from overload signals.

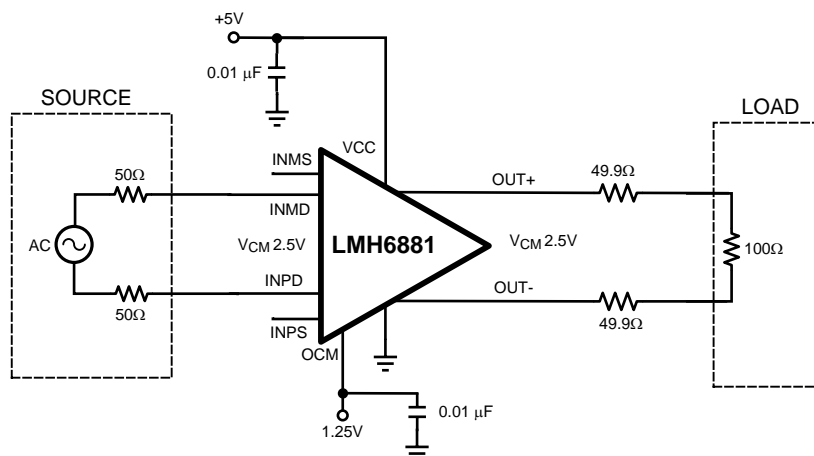


Figure 37. Basic Connections Schematic, Differential Input

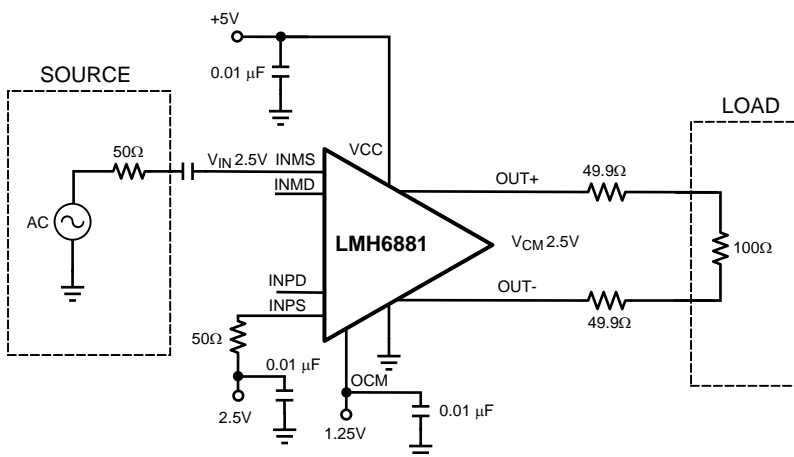


Figure 38. Basic Connections Schematic, Single Ended Input

INPUT CHARACTERISTICS

The LMH6881 input impedance is set by internal resistors to a nominal 100Ω. Process variations will result in a range of values. At higher frequencies parasitic reactances will start to impact the impedance. This characteristic will also depend on board layout and should be verified on the customer's system board.

At the maximum gain of 26dB the input signal will be much smaller than the output and the output may saturate or clip well before the input reaches the maximum signal amplitude. If the input is over driven, the input signal cannot swing more than 0.5V below the negative supply voltage (normally 0V) nor should it exceed the positive supply voltage. The input signal will clip and cause severe distortion if it is too large. Because the input stage self biases to approximately mid rail the supply voltage will impose the limit for input voltage swing.

At higher frequencies the LMH6881 input impedance is not purely resistive. The LMH6881 input may also be a different value than desired. This would be the case when connecting the LMH6881 directly to a mixer. It is possible to make narrow band LC impedance transform circuits to match the LMH6881 to other impedances. As an example [Figure 39](#) shows a circuit that converts 200 Ohms to 100 Ohms at 200MHz. For an easy way to calculate the L and C circuit values there are several options for online tools or down-loadable programs. The following tool might be helpful.

www.circuitsage.com/matching/matcher2.html

Excel can also be used for simple circuits; however, the "Analysis ToolPak" add-in must be installed to calculate complex numbers.

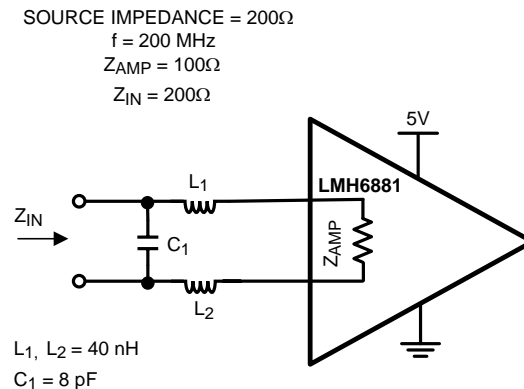


Figure 39. Differential LC Conversion Circuit

OUTPUT CHARACTERISTICS

The LMH6881 has a low impedance output very similar to a traditional Op-amp output. This means that a wide range of loads can be driven with good performance. Matching load impedance for proper termination of filters is as easy as inserting the proper value of resistor between the filter and the amplifier. This flexibility makes system design and gain calculations very easy.

By using a differential output stage the LMH6881 can achieve very large voltage swings on a single 5V supply. This is illustrated in Figure 40. This figure shows how a voltage swing of $5V_{PPD}$ is realized while only swinging $2.5V_{PP}$ on each output. The LMH6881 can swing up to $10V_{PPD}$ which is sufficient to drive most ADCs to full scale while using a matched impedance anti alias filter between the amplifier and the ADC. The LMH6881 has been designed for AC coupled applications and has been optimized for operation above 5 MHz.

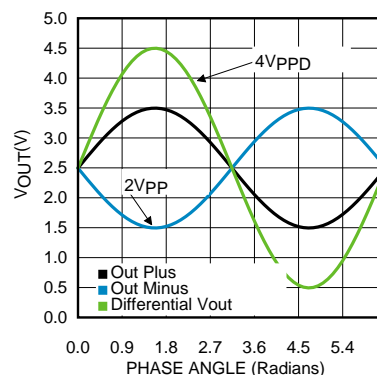


Figure 40. Differential Output Voltage

Like most closed loop amplifiers the LMH6881 output stage can be sensitive to capacitive loading. Best practise is to place the external termination resistors as close to the amplifier output pins as possible. Due to reactive components between the output and the filter input it may be desirable to use even smaller value resistors than a simple calculation would indicate. For instance, at 200 MHz resistors of 30 Ohms provide slightly better OIP3 performance on the LMH6881EVAL evaluation board and may also provide a better match to the filter input.

The ability of the LMH6881 to drive low impedance loads while maintaining excellent OIP3 performance creates an opportunity to greatly increase power gain and drive low impedance filters. This gives the system designer much needed flexibility in filter design. In many cases using a lower impedance filter will provide better component values for the filter. Another benefit of low impedance filters is that they are less likely to be influenced by circuit board parasitic reactances such as pad capacitance or trace inductance.

The LMH6881 is a voltage amplifier. Power gain is dependent on load conditions. See Figure 41 for details on power gain with respect to different load conditions. The graph was prepared for the 26dB voltage gain. Other gain settings will behave with the same.

All measurements in this data sheet, unless specified otherwise, refer to voltage or power at the device output pins. For instance, in an OPI3 measurement the power out will be equal to the output voltage at the device pins squared, divided by the total load voltage. In this case the power to the load would be three decibels less if the amplifier were to be used in a back terminated application such as driving a matched filter or transmission line.

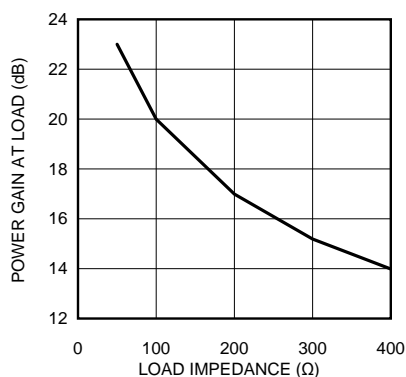


Figure 41. Power Gain vs Filter Impedance
Matching Resistor Loss = 6dB

Printed circuit board (PCB) design is critical to high frequency performance. In order to ensure output stability the load matching resistors should be placed as close to the amplifier output pins as possible. This allows the matching resistors to mask the board parasitics from the amplifier output circuit. An example of this is shown in Figure 42. Also note that the low pass filter uses center tapped capacitors. Having capacitors to ground provides a path for high frequency, common mode energy to dissipate. This is equally valuable for the ADC, so there are also capacitors to ground on the ADC side of the filter. The LMH6881EVAL evaluation board is available to serve as a guide for system board layout. See also application note AN-2235 for more details.

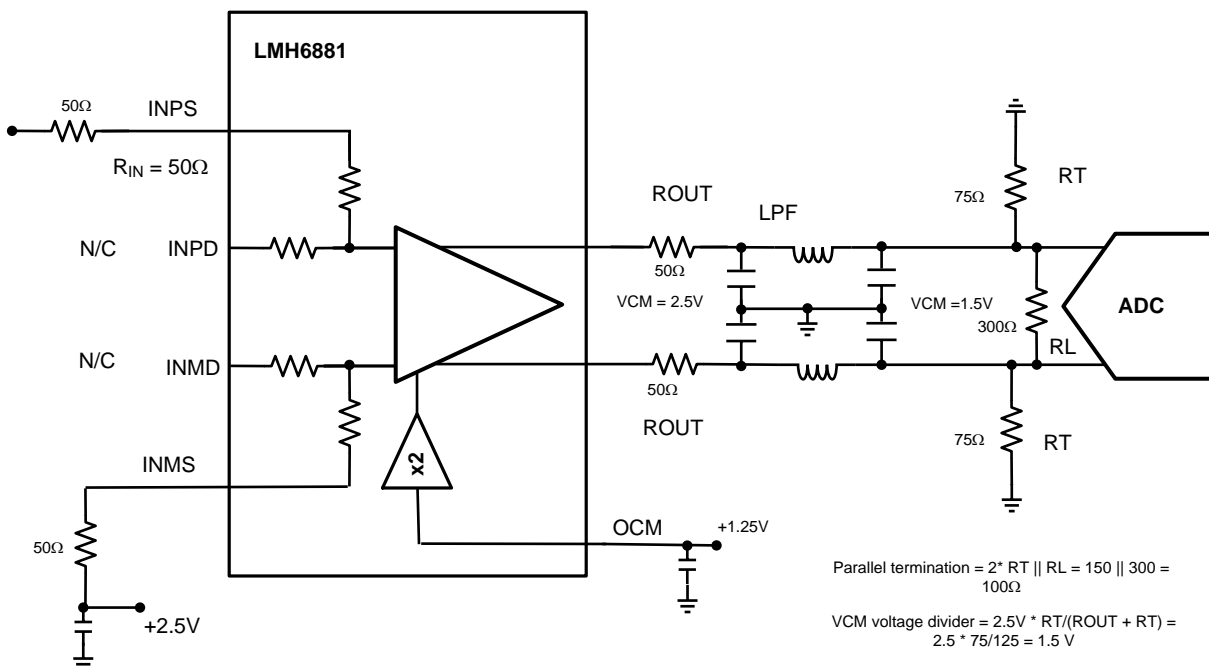


Figure 42. Single Ended Input, DC Coupled
Common Mode Voltage Divider on Output

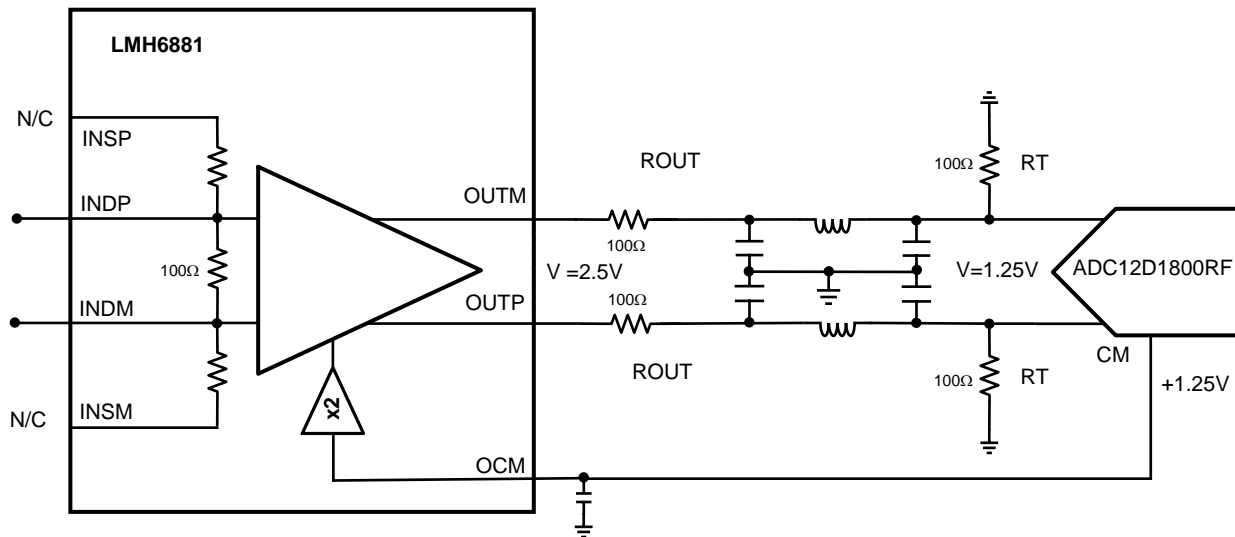


Figure 43. Differential Input, DC Coupled Common Mode Voltage Divider on Output

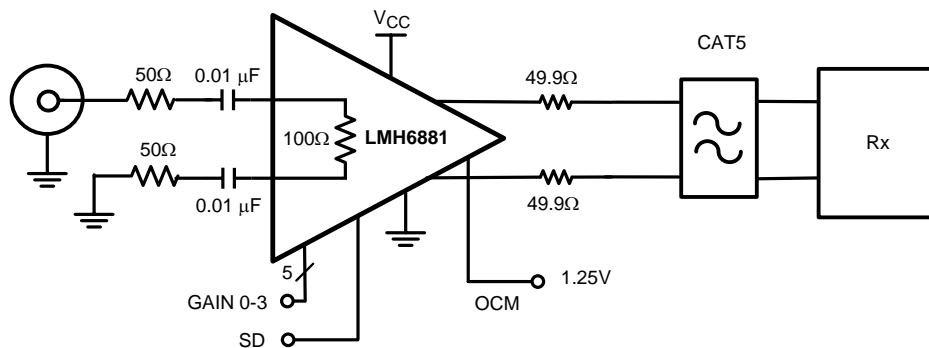


Figure 44. Single Ended Input, Differential Output Cable Driver

DIGITAL CONTROL

The LMH6881 will support two modes of control, parallel mode and serial mode (SPI compatible). Parallel mode is fastest and requires the most board space for logic line routing. Serial mode is compatible with existing SPI compatible systems.

The LMH6881 has gain settings covering a range of 20 dB. While the full gain range is available in parallel mode only 2dB steps are available. To avoid undesirable signal transients the LMH6881 should not be powered on with large inputs signals present. Careful planning of system power on sequencing is especially important to avoid damage to ADC inputs.

The LMH6881 was designed to interface with 2.5V to 5V CMOS logic circuits. If operation with 5V logic is required care should be taken to avoid signal transients exceeding the PDA supply voltage. Long, unterminated digital signal traces are particularly susceptible to these transients. Signal voltages on the logic pins that exceed the device power supply voltage may trigger ESD protection circuits and cause unreliable operation.

Some pins on the LMH6881 have different functions depending on the digital control mode. These functions will be described in the sections to follow.

Pins with Dual Functions

Pin	SPI = 0	SPI = 1
3	D1	SDI
4	D0	SDO ⁽¹⁾
15	D2	CLK
16	D3	CS (active low)

(1) Pin 4 requires external bias. See [Serial Mode](#) Section for Details.

PARALLEL INTERFACE

Parallel mode offers the fastest gain update capability with the drawback of requiring the most board space dedicated to control lines. To place the LMH6881 into parallel mode the SPI pin (pin 5) is set to the logical zero state. Alternately the SPI pin can be connected directly to ground.

The attenuator control pins are internally biased to logic high state with weak pull up resistors. The SPI pin has a weak internal resistor to ground. The enable pins bias to a mid logic state which is the Low Power Mode.

The LMH6881 has a 5-bit gain control bus. Data from the gain control pins is immediately sent to the gain circuit (i.e. gain is changed immediately). To minimize gain change glitches all gain pins should change at the same time. Gain glitches could result from timing skew between the gain set bits. This is especially the case when a small gain change requires a change in state of three or more gain control pins. If necessary the PDA could be put into a disabled state while the gain pins are reconfigured and then brought active when they have settled.

An SD (shutdown) pin is provided to reduce power consumption by disabling the highest power portions of the LMH6881. The gain register will preserve the last active gain setting during the disabled state. See the [Typical Performance](#) section for disable and enable timing information. The SD pin is inactive in SPI mode, see the [Serial Interface](#) section for SPI control options.

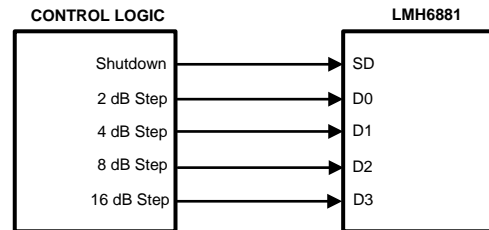


Figure 45. Parallel Mode Connection

SPI COMPATIBLE SERIAL INTERFACE

The serial interface allows a great deal of flexibility in gain programming and reduced board complexity. The LMH6881 serial interface is a generic 4-wire synchronous interface that is compatible with SPI type interfaces that are used on many microcontrollers and DSP controllers. Using only 4 wires for both channels allows for significant board space savings. The trade off for this reduced board complexity is slower response time in gain state changes. For systems where gain is changed only infrequently or where only slow gain changes are required serial mode is the best choice. To place the LMH6881 into serial mode the SPI pin (Pin 5) should be put into the logic high state. Alternatively the SPI pin can be connected directly to the 5V supply bus.

The serial mode is active when the SPI pin is set to a logic 1 state. In this configuration the pins function as shown in the [pin description](#) table. The SPI interface uses the following signals: clock input (CLK), serial data in (SDI), serial data out (SDO), and serial chip select (CS). The chip select pin is active low.

The enable pins are inactive in the serial mode. These pins can be left disconnected for serial mode.

The CLK pin is the serial clock pin. It is used to register the input data that is presented on the SDI pin on the rising edge; and to source the output data on the SDO pin on the falling edge. The user may disable clock and hold it in the low state, as long as the clock pulse-width minimum specification is not violated when the clock is enabled or disabled.

The CS pin is the chip select pin. This pin is active low, the chip is selected in the logic low state. Each assertion starts a new register access - i.e., the SDATA field protocol is required. The user is required to de-assert this signal after the 16th clock. If the CSb pin is de-asserted before the 16th clock, no address or data write will occur. The rising edge captures the address just shifted-in and, in the case of a write operation, writes the addressed register. There is a minimum pulse-width requirement for the de-asserted pulse - which is specified in the [Electrical Specifications](#) section.

The SDI pin is the input pin for the serial data. It must observe setup / hold requirements with respect to the SCLK. Each cycle is 16-bits long.

The SDO pin is the data output pin. This output is normally at a high impedance state, and is driven only when CSb is asserted. Upon CSb assertion, contents of the register addressed during the first byte are shifted out with the second 8 SCLK falling edges. Upon power-up, the default register address is 00h. The SDO pin requires external bias for clock speeds over 1MHz. See [Figure 47](#) for details on sizing the external bias resistor. Because the SDO pin is a high impedance pin, the board capacitance present at the pin will restrict data out speed that can be achieved. For a RC limited circuit the frequency is $\sim 1 / (2 * \pi * RC)$. As shown in the figure resistor values of 300 to 2000 Ohms are recommended.

Each serial interface access cycle is exactly 16 bits long as shown in [Figure 46](#). Each signal's function is described below. the read timing is shown in [Figure 48](#), while the write timing is shown in [Figure 49](#).

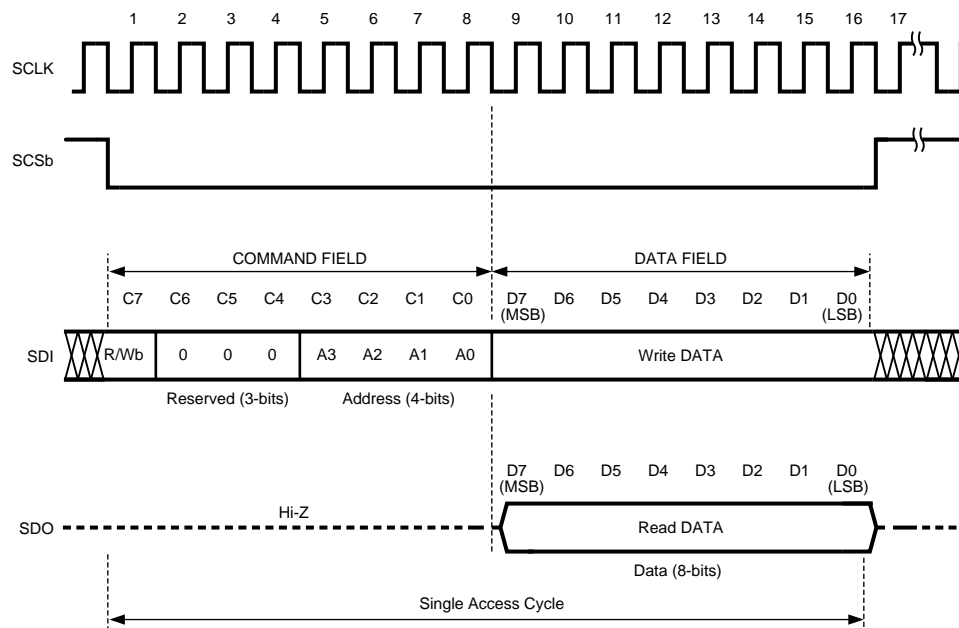


Figure 46. Serial Interface Protocol (SPI compatible)

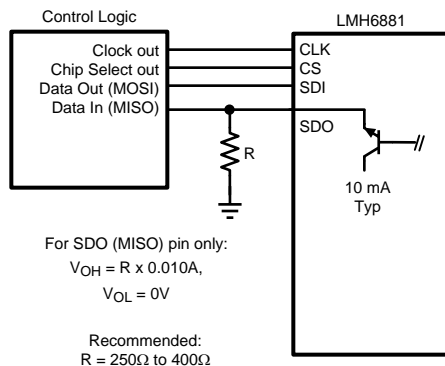


Figure 47. Internal Operation of the SDO pin

R/Wb	Read / Write bit. A value of 1 indicates a read operation, while a value of 0 indicates a write operation.
Reserved	Not used. Must be set to 0.
ADDR:	Address of register to be read or written.
DATA	In a write operation the value of this field will be written to the addressed register when the chip select pin is deasserted. In a read operation this field is ignored.

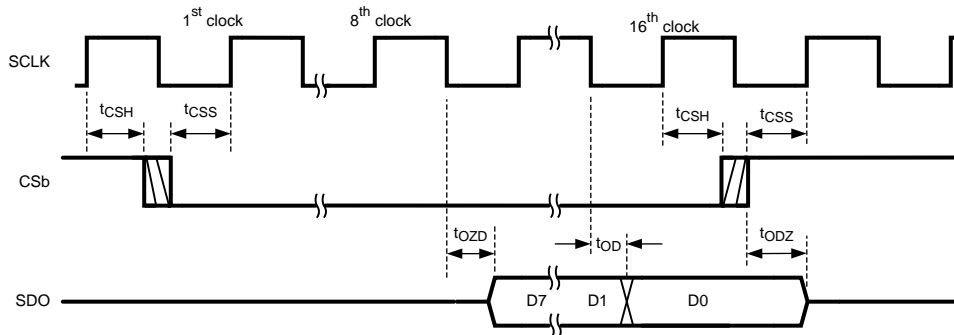


Figure 48. Read Timing

**Read Timing
Data Output on SDO Pin**

Parameter	Description
t_{CSH}	Chip select hold time
t_{CSS}	Chip select setup time
t_{OZD}	Initial output data delay
t_{ODZ}	High impedance delay
t_{OD}	Output data delay

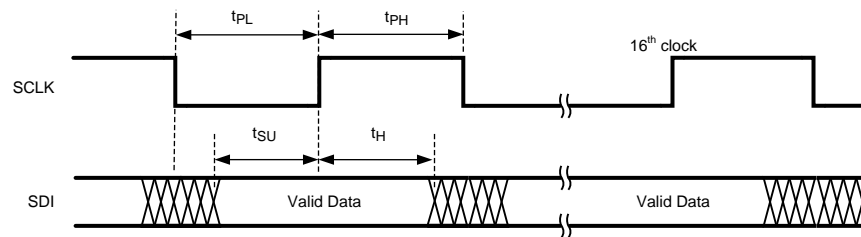


Figure 49. Write Timing Data Written to SDI Pin

Write Timing Data Input on SDI Pin

Parameter	Description
t_{PL}	Minimum clock low time (clock duty cycle)
t_{PH}	Minimum clock high time (clock duty cycle)
t_{SU}	Input data setup time
t_H	Input data hold time

Address	R/W	Name	Default Value Hex (Dec)
0	R	Revision ID	1 (1)
1	R	Product ID	20 (32)
2	R/W	Power Control	0 (0)
3	R/W	Attenuation	50 (80)

Serial Word Format for Register 2

7	6	5	4	3	2	1	0
RES	RES	RES	RES	RES	Shutdown 0= amp on		RES

Serial Word Format for Register 3

7	6	5	4	3	2	1	0
RES	Gain = 26 - (register value * 0.25) valid range is 0 to 80						

SPISU2 SPI CONTROL BOARD AND TINYI2CSPI SOFTWARE

Also available separately from the LMH6881EVAL evaluation board is a USB to SPI control board and supporting software. The SPISU2 board will connect directly to the LMH6881 evaluation board and provides a simple way to test and evaluate the SPI interface. For more details refer to the LMH6881EVAL user's guide. The evaluation board user's guide provides instructions on connecting the SPISU2 board and for configuring the TinyI2CSPI software.

THERMAL MANAGEMENT

The LMH6881 is packaged in a thermally enhanced package. The exposed pad is connected to the GND pins. It is recommended, but not necessary, that the exposed pad be connected to the supply ground plane. In any case, the thermal dissipation of the device is largely dependent on the attachment of this pad to the system printed circuit board (PCB). The exposed pad should be attached to as much copper on the PCB as possible, preferably external copper. However, it is also very important to maintain good high speed layout practices when designing a system board. Please refer to the LMH6881 evaluation board for suggested layout techniques.

The LMH6881EVAL evaluation board was designed for both signal integrity and thermal dissipation. The LMH6881EVAL has eight layers of copper. The inner copper layers are one ounce copper and are as solid as design constraints allow. The exterior copper layers are one ounce copper in order to allow fine geometry etching. The benefit of this board design is significant.

Applying a heat sink to the package will also help to remove heat from the device. The ATS-54150K-C2-R0 heat sink, manufactured by Advanced Thermal Solutions, provided good results in lab testing. Using both a heat sink and a good board thermal design will provide the best cooling results. If a heat sink will not fit in the system design, the external case can be used as a heat sink.

INTERFACING TO AN ADC

The LMH6881 was designed to be used with high speed ADCs such as the ADC12D1800RF, ADC12D1600RF or the ADS5400. As shown in the [Figure 36](#) Typical Application, DC coupling provides the best flexibility especially for first Nyquist applications.

The inputs of the LMH6881 will self bias to the optimum voltage for normal operation. The internal bias voltage for the inputs is approximately mid rail which is 2.5V with the typical 5V power supply condition. If DC coupling is not required it is usually easier to AC couple the amplifier to other stages.

ADC Noise Filter

Below are schematics and a table of values for second order Butterworth response filters for some common IF frequencies. These filters, shown in [Figure 50](#), offer a good compromise between bandwidth, noise rejection and cost. This filter topology is the same as is used on the ADC14V155KDRB High IF Receiver reference design board. This filter topology works best with the 12, 14 and 16 bit analog to digital converters shown in the table.

Filter Component Values⁽¹⁾

Center Frequency	75 MHz	150 MHz	180 MHz	250 MHz
Bandwidth	40 MHz	60 MHz	75 MHz	100 MHz
R1, R2	90Ω	90Ω	90Ω	90Ω
L1, L2	390 nH	370 nH	300 nH	225 nH
C1, C2	10 pF	3 pF	2.7 pF	1.9 pF
C3	22 pF	19 pF	15 pF	11 pF
L5	220 nH	62 nH	54 nH	36 nH
R3, R4	100Ω	100Ω	100Ω	100Ω

(1) Resistor values are approximate, but have been reduced due to the internal 10 Ohms of output resistance per pin.

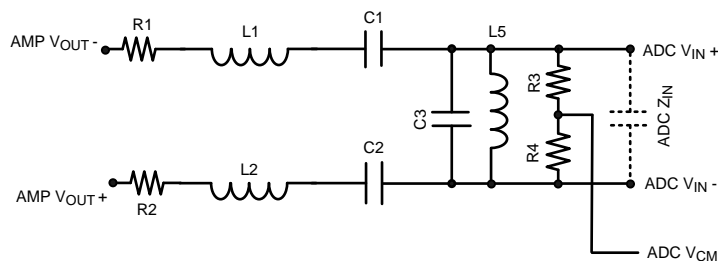


Figure 50. Sample Filter

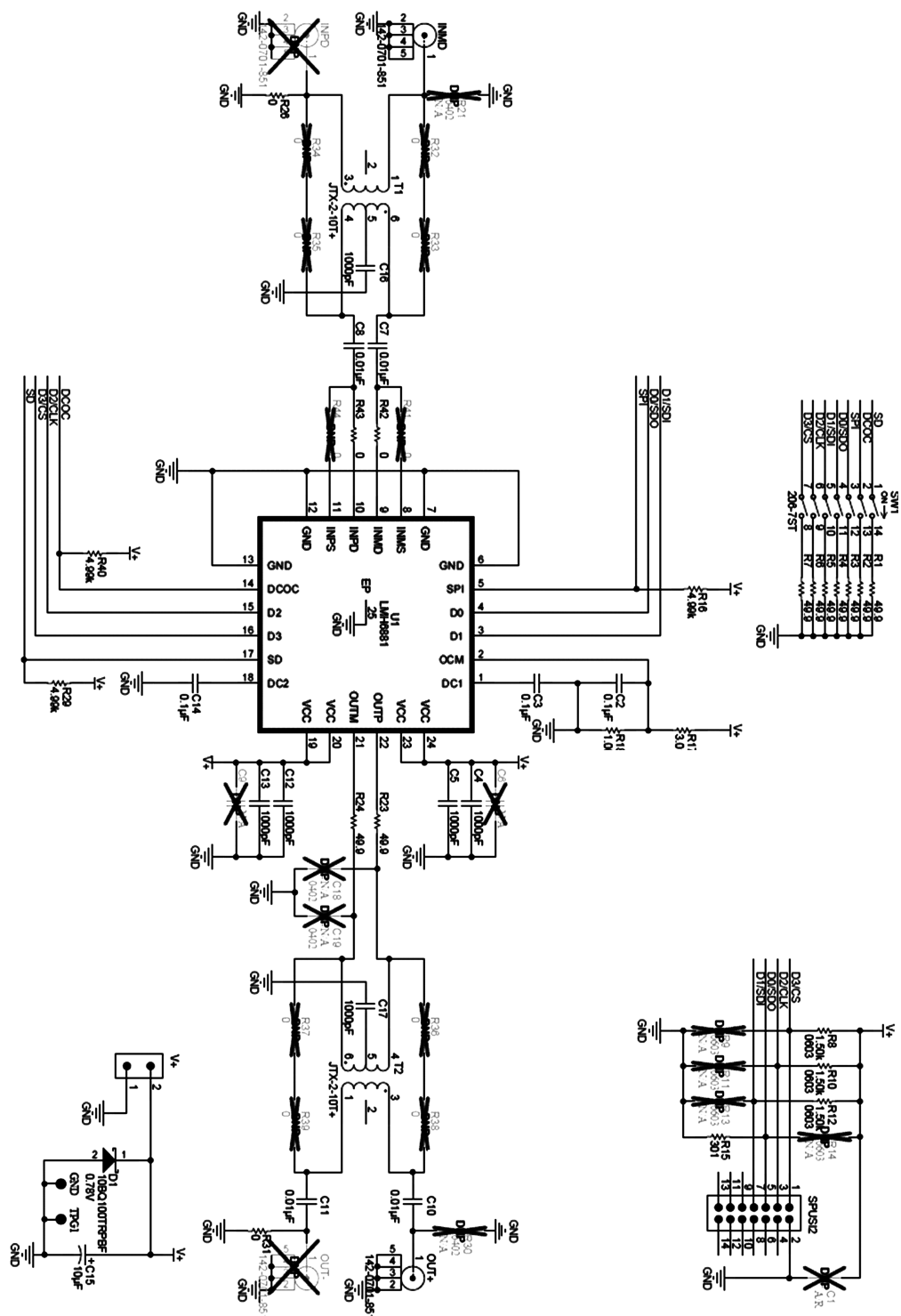
POWER SUPPLIES

The LMH6881 was designed primarily to be operated on 5V power supplies. The voltage range for VCC is 4.75V to 5.25V. Power supply accuracy of 2.5% or better is advised. When operated on a board with high speed digital signals it is important to provide isolation between digital signal noise and the LMH6881 inputs. The SP16160CH1RB reference board provides an example of good board layout.

COMPATIBLE HIGH SPEED ANALOG TO DIGITAL CONVERTERS

Product Number	Max Sampling Rate (MSPS)	Resolution	Channels
ADC12D1800RF	1800	12	DUAL
ADC12D1600RF	1600	12	DUAL
12D1000 RF	1000	12	DUAL
ADC12D800RF	800	12	DUAL
ADS5400	1000	12	SINGLE
ADC12C105	105	12	SINGLE
ADC10D1500	1500	10	DUAL
ADC12C170	170	12	SINGLE
ADC12V170	170	12	SINGLE
ADC14C105	105	14	SINGLE
ADC14DS105	105	14	DUAL
ADC14155	155	14	SINGLE
ADC14V155	155	14	SINGLE
ADC16V130	130	16	SINGLE
ADC16DV160	160	16	DUAL
ADC08D500	500	8	DUAL
ADC08500	500	8	SINGLE
ADC08D1000	1000	8	DUAL
ADC081000	1000	8	SINGLE
ADC08D1500	1500	8	DUAL
ADC081500	1500	8	SINGLE
ADC08(B)3000	3000	8	SINGLE
ADC08100	100	8	SINGLE
ADCS9888	170	8	SINGLE
ADC08(B)200	200	8	SINGLE
ADC11C125	125	11	SINGLE
ADC11C170	170	11	SINGLE

Evaluation Board



PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
LMH6881SQ/NOPB	ACTIVE	WQFN	RTW	24	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	L6881SQ	Samples
LMH6881SQE/NOPB	ACTIVE	WQFN	RTW	24	250	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	L6881SQ	Samples
LMH6881SQX/NOPB	ACTIVE	WQFN	RTW	24	4500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	L6881SQ	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

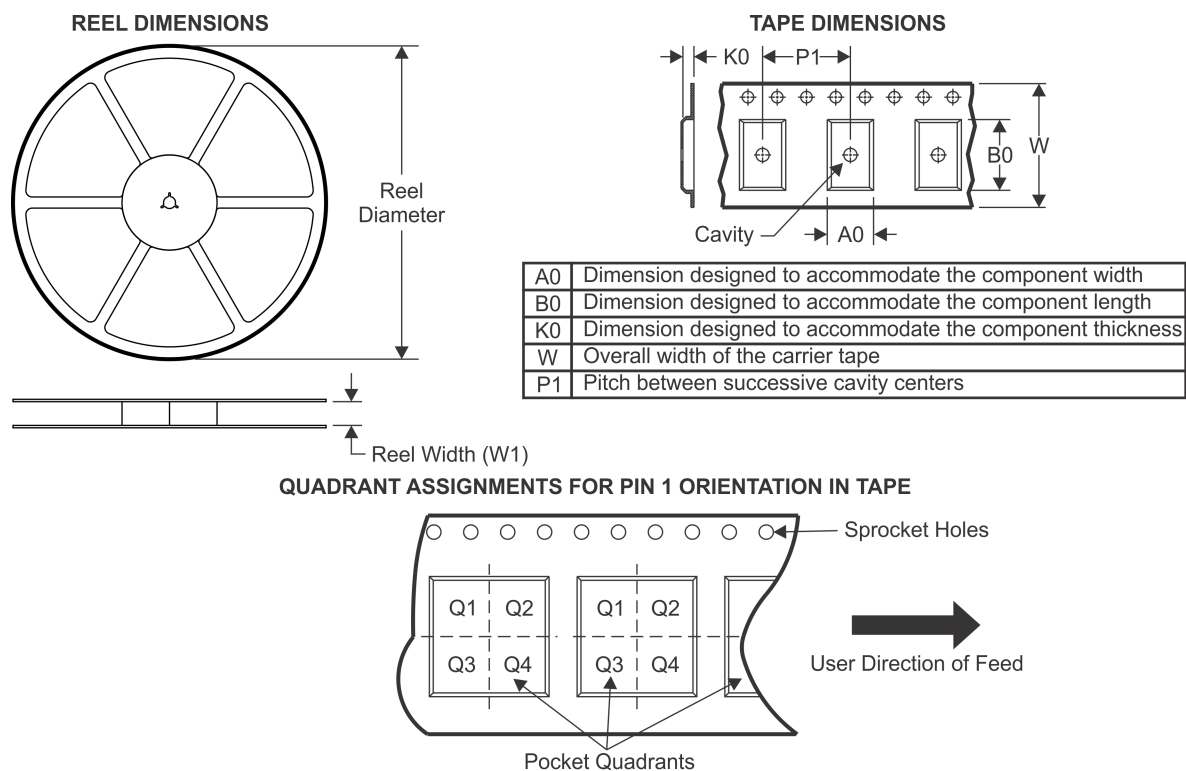
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Only one of markings shown within the brackets will appear on the physical device.

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*All dimensions are nominal

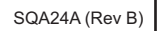
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMH6881SQ/NOPB	WQFN	RTW	24	1000	178.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LMH6881SQE/NOPB	WQFN	RTW	24	250	178.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LMH6881SQX/NOPB	WQFN	RTW	24	4500	330.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMH6881SQ/NOPB	WQFN	RTW	24	1000	203.0	190.0	41.0
LMH6881SQE/NOPB	WQFN	RTW	24	250	203.0	190.0	41.0
LMH6881SQX/NOPB	WQFN	RTW	24	4500	349.0	337.0	45.0



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No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have **not** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

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