

LMP2011 Single/LMP2012 Dual High Precision, Rail-to-Rail Output Operational Amplifier

Check for Samples: [LMP2011](#), [LMP2012](#)

FEATURES

(For $V_S = 5V$, Typical Unless Otherwise Noted)

- Low Guaranteed V_{OS} Over Temperature 60 μV
- Low Noise With No $1/f$ 35nV/ \sqrt{Hz}
- High CMRR 130 dB
- High PSRR 120 dB
- High A_{VOL} 130 dB
- Wide Gain-Bandwidth Product 3MHz
- High Slew Rate 4V/ μs
- Low Supply Current 930 μA

- Rail-to-Rail Output 30mV
- No External Capacitors Required

APPLICATIONS

- Precision Instrumentation Amplifiers
- Thermocouple Amplifiers
- Strain Gauge Bridge Amplifier

DESCRIPTION

The LMP201x series are the first members of National's new LMP™ precision amplifier family. The LMP201X series offers unprecedented accuracy and stability in space-saving miniature packaging while also being offered at an affordable price. This device utilizes patented techniques to measure and continually correct the input offset error voltage. The result is an amplifier which is ultra stable over time and temperature. It has excellent CMRR and PSRR ratings, and does not exhibit the familiar $1/f$ voltage and current noise increase that plagues traditional amplifiers. The combination of the LMP201X characteristics makes it a good choice for transducer amplifiers, high gain configurations, ADC buffer amplifiers, DAC I-V conversion, and any other 2.7V-5V application requiring precision and long term stability.

Other useful benefits of the LMP201X are rail-to-rail output, a low supply current of 930 μA , and wide gain-bandwidth product of 3 MHz. These extremely versatile features found in the LMP201X provide high performance and ease of use.

Connection Diagram

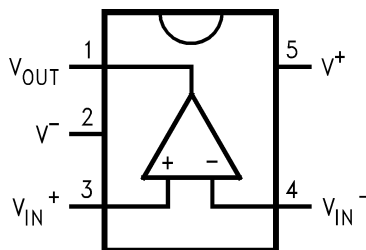


Figure 1. 5-Pin SOT-23 Single (LMP2011) Top View

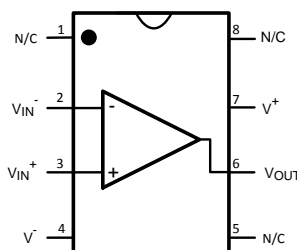


Figure 2. 8-Pin Single SOIC (LMP2011) Top View

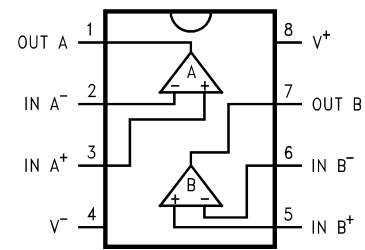


Figure 3. 8-Pin Dual SOIC/VSSOP (LMP2012) Top View



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.



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Absolute Maximum Ratings ⁽¹⁾⁽²⁾

ESD Tolerance	Human Body Model	2000V
	Machine Model	200V
Supply Voltage		5.8V
Common-Mode Input Voltage		$-0.3 \leq V_{CM} \leq V_{CC} + 0.3V$
Lead Temperature (soldering 10 sec.)		+300°C
Differential Input Voltage		±Supply Voltage
Current at Input Pin		30 mA
Current at Output Pin		30 mA
Current at Power Supply Pin		50 mA

- (1) Absolute Maximum Ratings indicate limits beyond which damage may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and test conditions, see the Electrical Characteristics.
- (2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.

Operating Ratings ⁽¹⁾

Supply Voltage	2.7V to 5.25V
Storage Temperature Range	–65°C to 150°C
Operating Temperature Range	–40°C to 125°C

- (1) Absolute Maximum Ratings indicate limits beyond which damage may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and test conditions, see the Electrical Characteristics.

2.7V DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_J = 25^\circ\text{C}$, $V^+ = 2.7V$, $V^- = 0V$, $V_{CM} = 1.35V$, $V_O = 1.35V$ and $R_L > 1\text{ M}\Omega$.

Boldface limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min ⁽¹⁾	Typ ⁽²⁾	Max ⁽¹⁾	Units
V_{OS}	Input Offset Voltage (LMP2011 only)			0.8	25 60	μV
	Input Offset Voltage (LMP2012 only)			0.8	36 60	
	Offset Calibration Time			0.5	10 12	ms
TCV_{OS}	Input Offset Voltage			0.015		$\mu\text{V}/^\circ\text{C}$
	Long-Term Offset Drift			0.006		$\mu\text{V}/\text{month}$
	Lifetime V_{OS} Drift			2.5		μV
I_{IN}	Input Current			–3		pA
I_{OS}	Input Offset Current			6		pA
R_{IND}	Input Differential Resistance			9		M Ω
CMRR	Common Mode Rejection Ratio	$-0.3 \leq V_{CM} \leq 0.9V$ $0 \leq V_{CM} \leq 0.9V$	95 90	130		dB
PSRR	Power Supply Rejection Ratio		95 90	120		dB
A_{VOL}	Open Loop Voltage Gain	$R_L = 10\text{ k}\Omega$	95 90	130		dB
		$R_L = 2\text{ k}\Omega$	90 85	124		

- (1) Limits are 100% production tested at 25°C. Limits over the operating temperature range are guaranteed through correlations using statistical quality control (SQC) method.
- (2) Typical values represent the most likely parametric norm.

2.7V DC Electrical Characteristics (continued)

Unless otherwise specified, all limits guaranteed for $T_J = 25^\circ\text{C}$, $V^+ = 2.7\text{V}$, $V^- = 0\text{V}$, $V_{CM} = 1.35\text{V}$, $V_O = 1.35\text{V}$ and $R_L > 1\text{ M}\Omega$.

Boldface limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min ⁽¹⁾	Typ ⁽²⁾	Max ⁽¹⁾	Units
V_O	Output Swing (LMP2011 only)	$R_L = 10\text{ k}\Omega$ to 1.35V $V_{IN}(\text{diff}) = \pm 0.5\text{V}$	2.665 2.655	2.68		V
				0.033	0.060 0.075	
		$R_L = 2\text{ k}\Omega$ to 1.35V $V_{IN}(\text{diff}) = \pm 0.5\text{V}$	2.630 2.615	2.65		V
				0.061	0.085 0.105	
	Output Swing (LMP2012 only)	$R_L = 10\text{ k}\Omega$ to 1.35V $V_{IN}(\text{diff}) = \pm 0.5\text{V}$	2.64 2.63	2.68		V
				0.033	0.060 0.075	
		$R_L = 2\text{ k}\Omega$ to 1.35V $V_{IN}(\text{diff}) = \pm 0.5\text{V}$	2.615 2.6	2.65		V
				0.061	0.085 0.105	
I_O	Output Current	Sourcing, $V_O = 0\text{V}$ $V_{IN}(\text{diff}) = \pm 0.5\text{V}$	5 3	12		mA
		Sinking, $V_O = 5\text{V}$ $V_{IN}(\text{diff}) = \pm 0.5\text{V}$	5 3	18		
I_S	Supply Current per Channel			0.919	1.20 1.50	mA

2.7V AC Electrical Characteristics

$T_J = 25^\circ\text{C}$, $V^+ = 2.7\text{V}$, $V^- = 0\text{V}$, $V_{CM} = 1.35\text{V}$, $V_O = 1.35\text{V}$, and $R_L > 1\text{ M}\Omega$. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min ⁽¹⁾	Typ ⁽²⁾	Max ⁽¹⁾	Units
GBW	Gain-Bandwidth Product			3		MHz
SR	Slew Rate			4		V/ μs
θ_m	Phase Margin			60		Deg
G_m	Gain Margin			-14		dB
e_n	Input-Referred Voltage Noise			35		$\text{nV}/\sqrt{\text{Hz}}$
i_n	Input-Referred Current Noise					$\text{pA}/\sqrt{\text{Hz}}$
$e_{n\text{p-p}}$	Input-Referred Voltage Noise	$R_S = 100\Omega$, DC to 10 Hz		850		nV_{pp}
t_{rec}	Input Overload Recovery Time			50		ms

(1) Limits are 100% production tested at 25°C . Limits over the operating temperature range are guaranteed through correlations using statistical quality control (SQC) method.

(2) Typical values represent the most likely parametric norm.

5V DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_J = 25^\circ\text{C}$, $V^+ = 5\text{V}$, $V^- = 0\text{V}$, $V_{CM} = 2.5\text{V}$, $V_O = 2.5\text{V}$ and $R_L > 1\text{ M}\Omega$.

Boldface limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min ⁽¹⁾	Typ ⁽²⁾	Max ⁽¹⁾	Units
V_{OS}	Input Offset Voltage (LMP2011 only)			0.12	25 60	μV
	Input Offset Voltage (LMP2012 only)			0.12	36 60	
	Offset Calibration Time			0.5	10 12	ms

(1) Limits are 100% production tested at 25°C . Limits over the operating temperature range are guaranteed through correlations using statistical quality control (SQC) method.

(2) Typical values represent the most likely parametric norm.

5V DC Electrical Characteristics (continued)

Unless otherwise specified, all limits guaranteed for $T_J = 25^\circ\text{C}$, $V^+ = 5\text{V}$, $V^- = 0\text{V}$, $V_{\text{CM}} = 2.5\text{V}$, $V_O = 2.5\text{V}$ and $R_L > 1\text{M}\Omega$.

Boldface limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min ⁽¹⁾	Typ ⁽²⁾	Max ⁽¹⁾	Units
TCV _{OS}	Input Offset Voltage			0.015		$\mu\text{V}/^\circ\text{C}$
	Long-Term Offset Drift			0.006		$\mu\text{V}/\text{month}$
	Lifetime V _{OS} Drift			2.5		μV
I _{IN}	Input Current			-3		pA
I _{OS}	Input Offset Current			6		pA
R _{IND}	Input Differential Resistance			9		M Ω
CMRR	Common Mode Rejection Ratio	$-0.3 \leq V_{\text{CM}} \leq 3.2$ $0 \leq V_{\text{CM}} \leq 3.2$	100 90	130		dB
PSRR	Power Supply Rejection Ratio		95 90	120		dB
A _{VOL}	Open Loop Voltage Gain	$R_L = 10\text{ k}\Omega$	105 100	130		dB
		$R_L = 2\text{ k}\Omega$	95 90	132		
V _O	Output Swing (LMP2011 only)	$R_L = 10\text{ k}\Omega$ to 2.5V $V_{\text{IN}}(\text{diff}) = \pm 0.5\text{V}$	4.96 4.95	4.978		V
				0.040	0.070 0.085	
		$R_L = 2\text{ k}\Omega$ to 2.5V $V_{\text{IN}}(\text{diff}) = \pm 0.5\text{V}$	4.895 4.875	4.919		V
				0.091	0.115 0.140	
	Output Swing (LMP2012 only)	$R_L = 10\text{ k}\Omega$ to 2.5V $V_{\text{IN}}(\text{diff}) = \pm 0.5\text{V}$	4.92 4.91	4.978		V
				0.040	0.080 0.095	
I _O	Output Current	Sourcing, $V_O = 0\text{V}$ $V_{\text{IN}}(\text{diff}) = \pm 0.5\text{V}$	8 6	15		mA
		Sinking, $V_O = 5\text{V}$ $V_{\text{IN}}(\text{diff}) = \pm 0.5\text{V}$	8 6	17		
I _S	Supply Current per Channel			0.930	1.20 1.50	mA

5V AC Electrical Characteristics

$T_J = 25^\circ\text{C}$, $V^+ = 5\text{V}$, $V^- = 0\text{V}$, $V_{\text{CM}} = 2.5\text{V}$, $V_O = 2.5\text{V}$, and $R_L > 1\text{M}\Omega$. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min ⁽¹⁾	Typ ⁽²⁾	Max ⁽¹⁾	Units
GBW	Gain-Bandwidth Product			3		MHz
SR	Slew Rate			4		V/ μs
θ_m	Phase Margin			60		deg
G _m	Gain Margin			-15		dB
e _n	Input-Referred Voltage Noise			35		nV/ $\sqrt{\text{Hz}}$
i _n	Input-Referred Current Noise					pA/ $\sqrt{\text{Hz}}$
e _n p-p	Input-Referred Voltage Noise	$R_S = 100\Omega$, DC to 10 Hz		850		nV _{pp}
t _{rec}	Input Overload Recovery Time			50		ms

(1) Limits are 100% production tested at 25°C . Limits over the operating temperature range are guaranteed through correlations using statistical quality control (SQC) method.

(2) Typical values represent the most likely parametric norm.

Typical Performance Characteristics

$T_A = 25^\circ\text{C}$, $V_S = 5\text{V}$ unless otherwise specified.

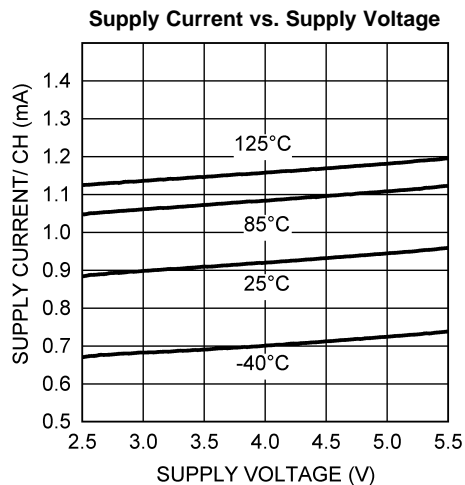


Figure 4.

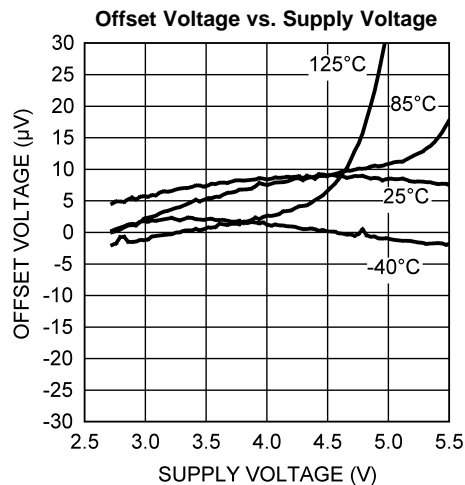


Figure 5.

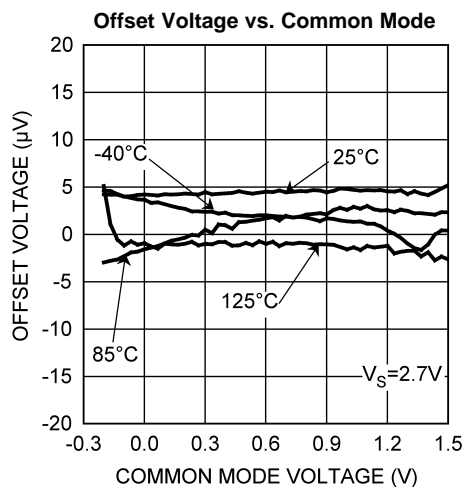


Figure 6.

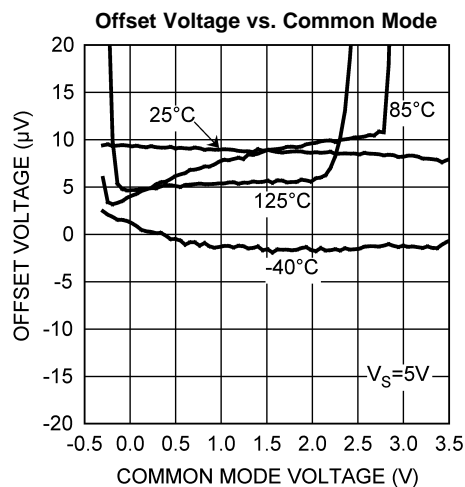


Figure 7.

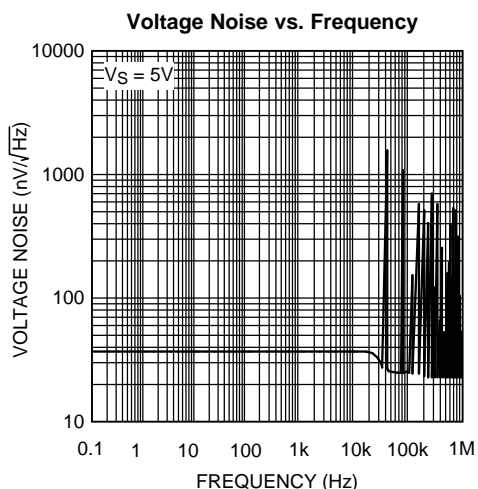


Figure 8.

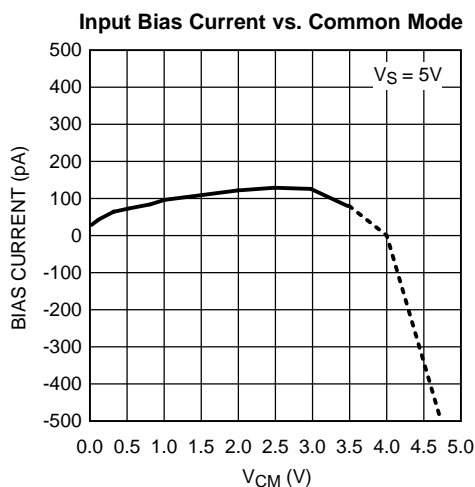


Figure 9.

Typical Performance Characteristics (continued)

$T_A = 25^\circ\text{C}$, $V_S = 5\text{V}$ unless otherwise specified.

PSRR vs. Frequency

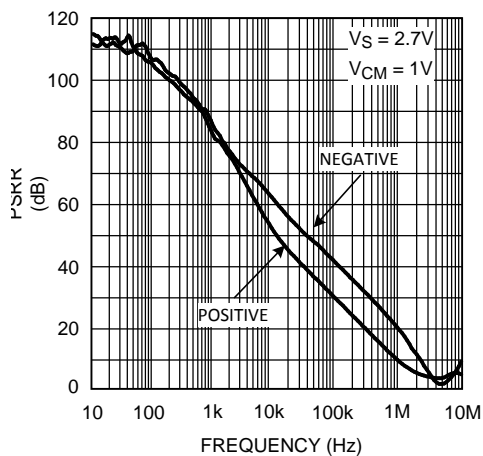


Figure 10.

PSRR vs. Frequency

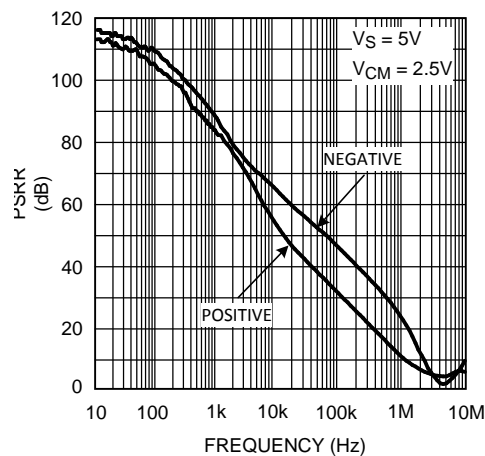


Figure 11.

Output Sourcing @ 2.7V

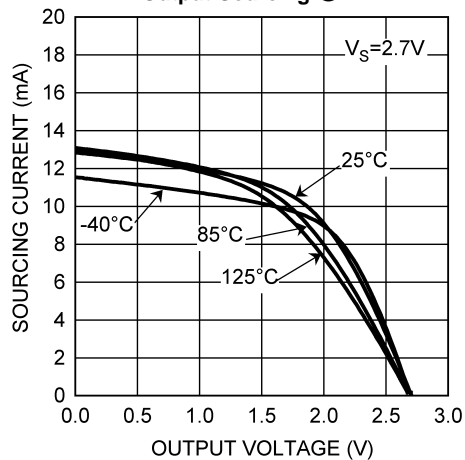


Figure 12.

Output Sourcing @ 5V

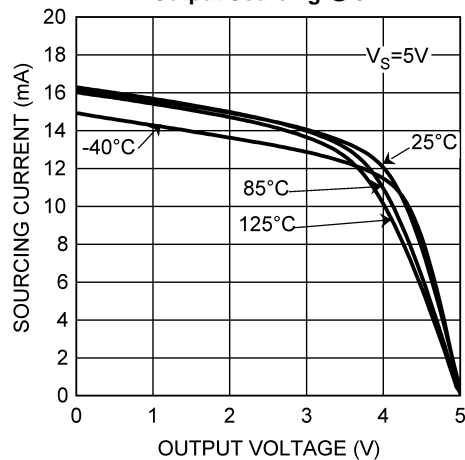


Figure 13.

Output Sinking @ 2.7V

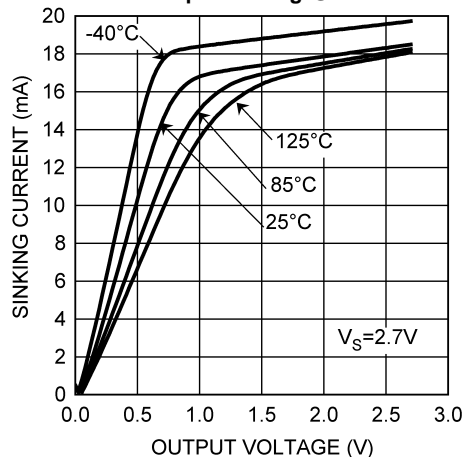


Figure 14.

Output Sinking @ 5V

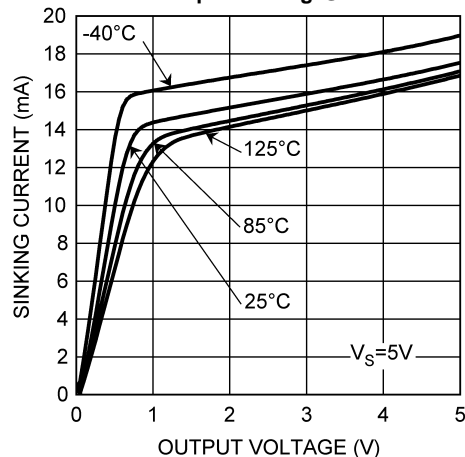


Figure 15.

Typical Performance Characteristics (continued)

$T_A=25^\circ\text{C}$, $V_S=5\text{V}$ unless otherwise specified.

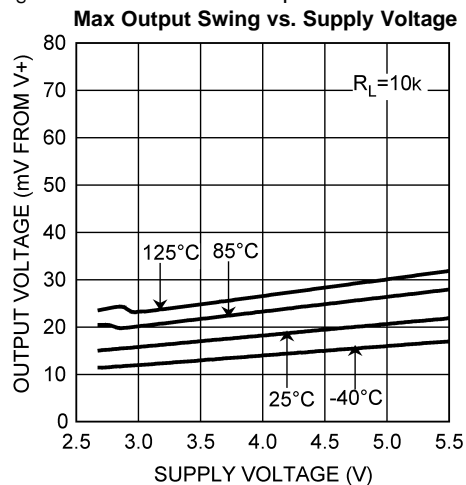


Figure 16.

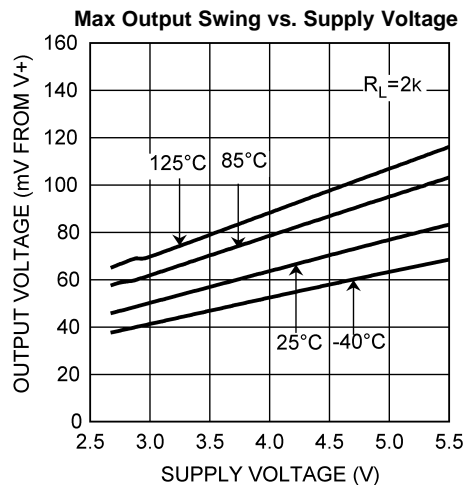


Figure 17.

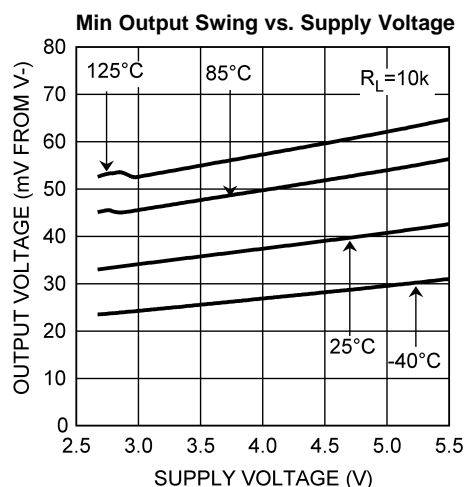


Figure 18.

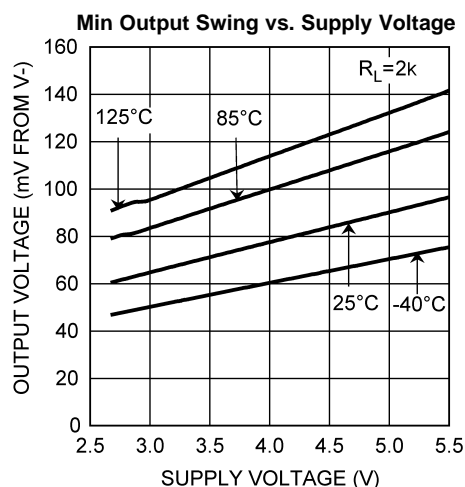


Figure 19.

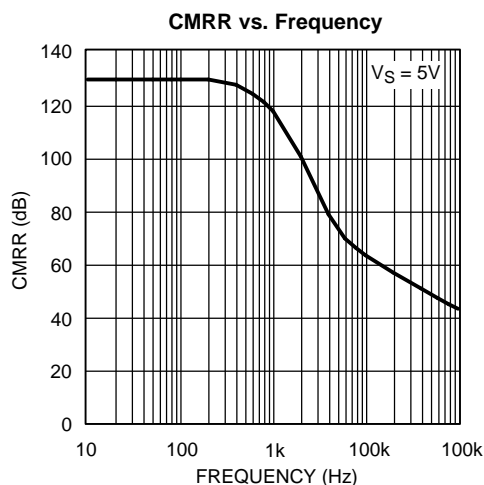


Figure 20.

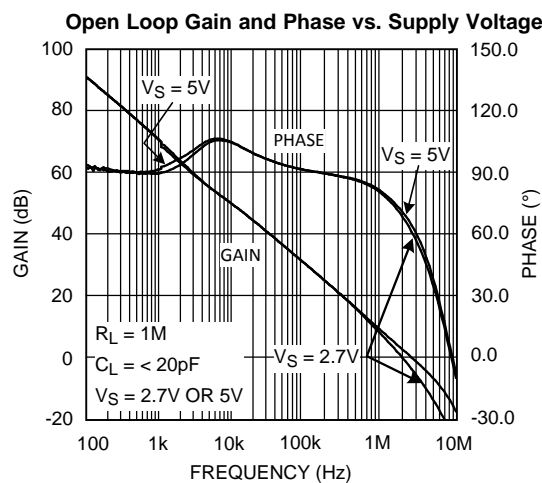


Figure 21.

Typical Performance Characteristics (continued)

$T_A = 25^\circ\text{C}$, $V_S = 5\text{V}$ unless otherwise specified.

Open Loop Gain and Phase vs. R_L @ 2.7V

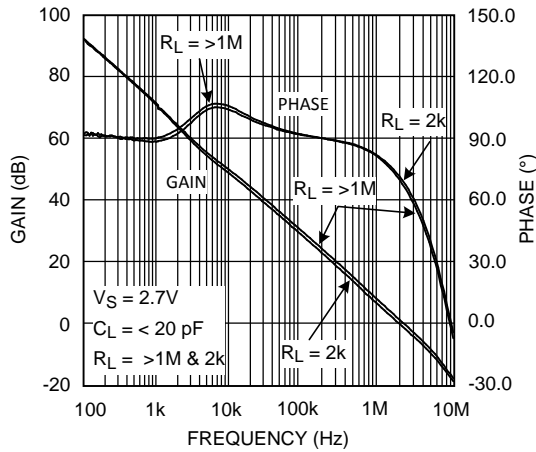


Figure 22.

Open Loop Gain and Phase vs. R_L @ 5V

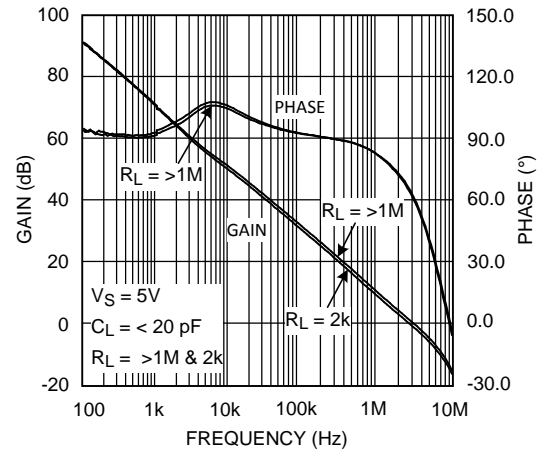


Figure 23.

Open Loop Gain and Phase vs. C_L @ 2.7V

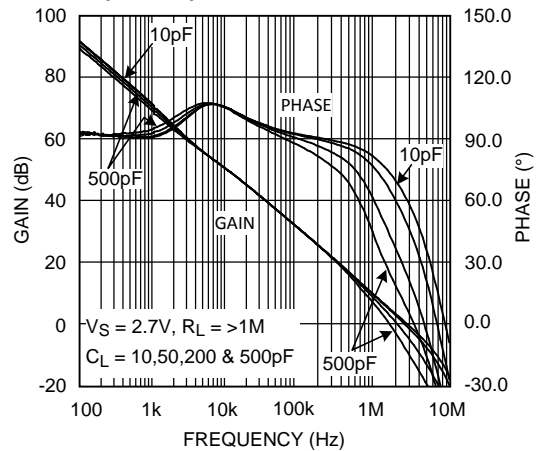


Figure 24.

Open Loop Gain and Phase vs. C_L @ 5V

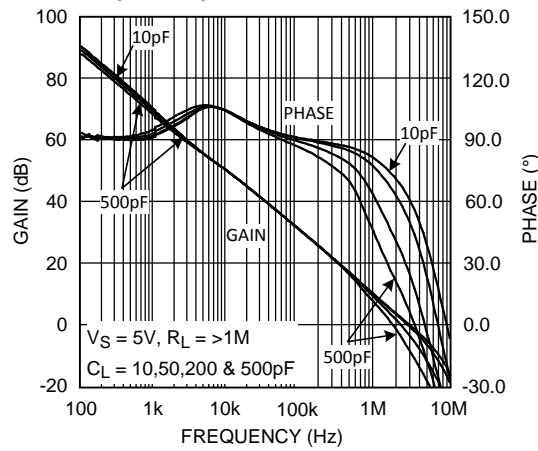


Figure 25.

Open Loop Gain and Phase vs. Temperature @ 2.7V

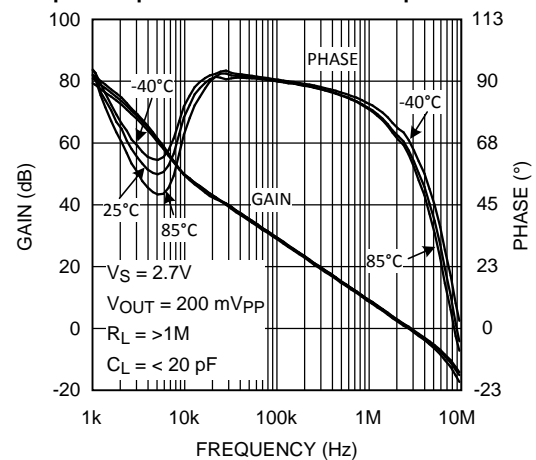


Figure 26.

Open Loop Gain and Phase vs. Temperature @ 5V

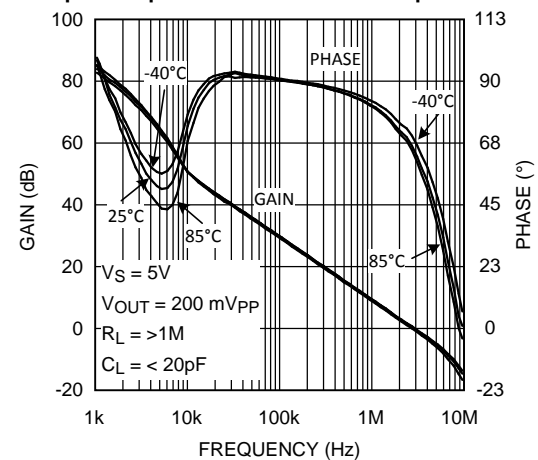


Figure 27.

Typical Performance Characteristics (continued)

$T_A = 25^\circ\text{C}$, $V_S = 5\text{V}$ unless otherwise specified.

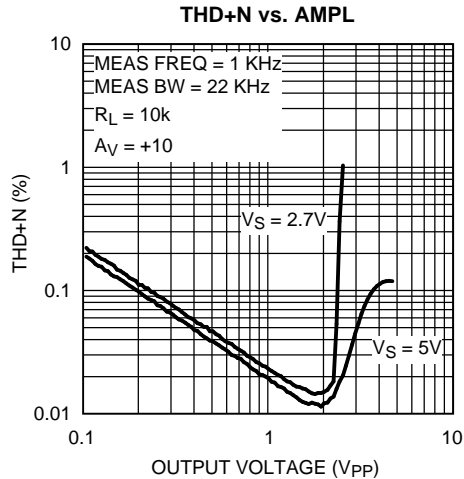


Figure 28.

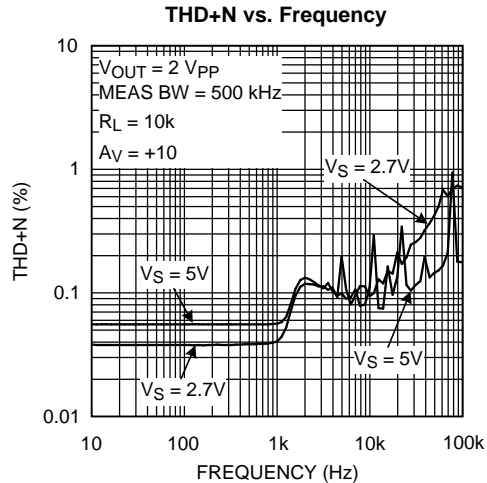


Figure 29.

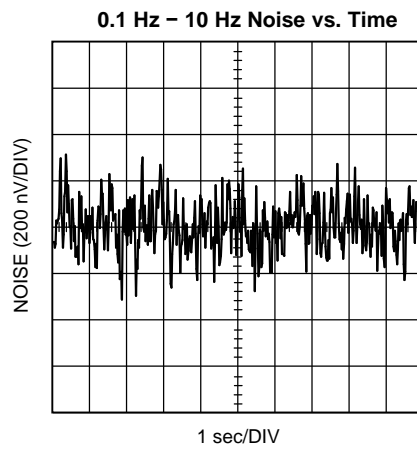


Figure 30.

APPLICATION INFORMATION

THE BENEFITS OF LMP201X NO 1/f NOISE

Using patented methods, the LMP201X eliminates the 1/f noise present in other amplifiers. That noise, which increases as frequency decreases, is a major source of measurement error in all DC-coupled measurements. Low-frequency noise appears as a constantly-changing signal in series with any measurement being made. As a result, even when the measurement is made rapidly, this constantly-changing noise signal will corrupt the result. The value of this noise signal can be surprisingly large. For example: If a conventional amplifier has a flat-band noise level of $10\text{ nV}/\sqrt{\text{Hz}}$ and a noise corner of 10 Hz, the RMS noise at 0.001 Hz is $1\mu\text{V}/\sqrt{\text{Hz}}$. This is equivalent to a $0.50\text{ }\mu\text{V}$ peak-to-peak error, in the frequency range 0.001 Hz to 1.0 Hz. In a circuit with a gain of 1000, this produces a 0.50 mV peak-to-peak output error. This number of 0.001 Hz might appear unreasonably low, but when a data acquisition system is operating for 17 minutes, it has been on long enough to include this error. In this same time, the LMP201X will only have a 0.21 mV output error. This is smaller by 2.4 x. Keep in mind that this 1/f error gets even larger at lower frequencies. At the extreme, many people try to reduce this error by integrating or taking several samples of the same signal. This is also doomed to failure because the 1/f nature of this noise means that taking longer samples just moves the measurement into lower frequencies where the noise level is even higher.

The LMP201X eliminates this source of error. The noise level is constant with frequency so that reducing the bandwidth reduces the errors caused by noise.

Another source of error that is rarely mentioned is the error voltage caused by the inadvertent thermocouples created when the common "Kovar type" IC package lead materials are soldered to a copper printed circuit board. These steel-based leadframe materials can produce over $35\text{ }\mu\text{V}/^\circ\text{C}$ when soldered onto a copper trace. This can result in thermocouple noise that is equal to the LMP201X noise when there is a temperature difference of only 0.0014°C between the lead and the board!

For this reason, the lead-frame of the LMP201X is made of copper. This results in equal and opposite junctions which cancel this effect. The extremely small size of the SOT-23 package results in the leads being very close together. This further reduces the probability of temperature differences and hence decreases thermal noise.

OVERLOAD RECOVERY

The LMP201X recovers from input overload much faster than most chopper-stabilized op amps. Recovery from driving the amplifier to 2X the full scale output, only requires about 40 ms. Many chopper-stabilized amplifiers will take from 250 ms to several seconds to recover from this same overload. This is because large capacitors are used to store the unadjusted offset voltage.

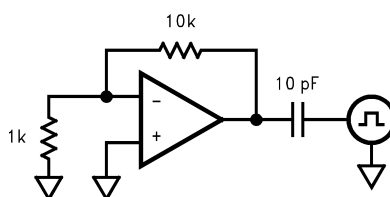


Figure 31. Overload Recovery Test

The wide bandwidth of the LMP201X enhances performance when it is used as an amplifier to drive loads that inject transients back into the output. ADCs (Analog-to-Digital Converters) and multiplexers are examples of this type of load. To simulate this type of load, a pulse generator producing a 1V peak square wave was connected to the output through a 10 pF capacitor. (Figure 31) The typical time for the output to recover to 1% of the applied pulse is 80 ns. To recover to 0.1% requires 860ns. This rapid recovery is due to the wide bandwidth of the output stage and large total GBW.

NO EXTERNAL CAPACITORS REQUIRED

The LMP201X does not need external capacitors. This eliminates the problems caused by capacitor leakage and dielectric absorption, which can cause delays of several seconds from turn-on until the amplifier's error has settled.

MORE BENEFITS

The LMP201X offers the benefits mentioned above and more. It has a rail-to-rail output and consumes only 950 μA of supply current while providing excellent DC and AC electrical performance. In DC performance, the LMP201X achieves 130 dB of CMRR, 120 dB of PSRR and 130 dB of open loop gain. In AC performance, the LMP201X provides 3 MHz of gain-bandwidth product and 4 V/ μs of slew rate.

HOW THE LMP201X WORKS

The LMP201X uses new, patented techniques to achieve the high DC accuracy traditionally associated with chopper-stabilized amplifiers without the major drawbacks produced by chopping. The LMP201X continuously monitors the input offset and corrects this error. The conventional chopping process produces many mixing products, both sums and differences, between the chopping frequency and the incoming signal frequency. This mixing causes large amounts of distortion, particularly when the signal frequency approaches the chopping frequency. Even without an incoming signal, the chopper harmonics mix with each other to produce even more trash. If this sounds unlikely or difficult to understand, look at the plot (Figure 32), of the output of a typical (MAX432) chopper-stabilized op amp. This is the output when there is no incoming signal, just the amplifier in a gain of -10 with the input grounded. The chopper is operating at about 150 Hz; the rest is mixing products. Add an input signal and the noise gets much worse. Compare this plot with Figure 33 of the LMP201X. This data was taken under the exact same conditions. The auto-zero action is visible at about 30 kHz but note the absence of mixing products at other frequencies. As a result, the LMP201X has very low distortion of 0.02% and very low mixing products.

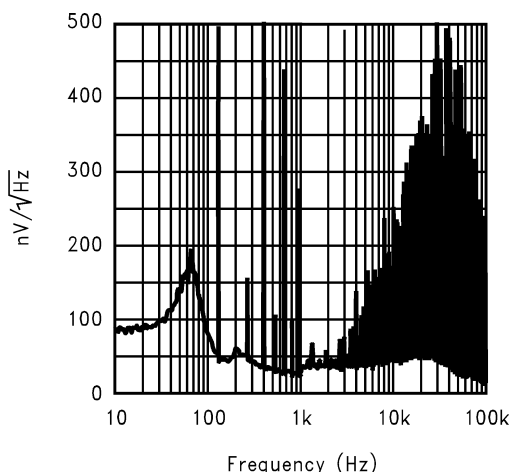


Figure 32. The Output of a Chopper Stabilized Op Amp (MAX432)

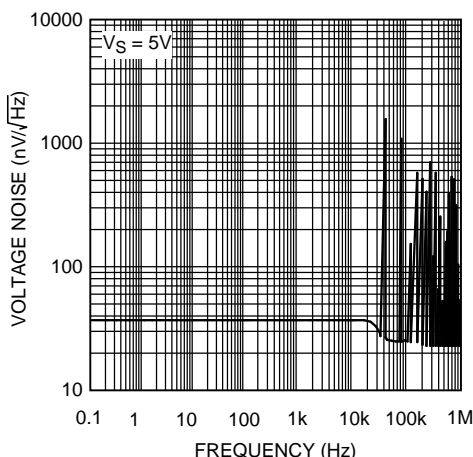


Figure 33. The Output of the LMP2011/LMP2012

INPUT CURRENTS

The LMP201X's input currents are different than standard bipolar or CMOS input currents in that it appears as a current flowing in one input and out the other. Under most operating conditions, these currents are in the picoamp level and will have little or no effect in most circuits. These currents tend to increase slightly when the common-mode voltage is near the minus supply. (See the [typical curves](#).) At high temperatures such as 85°C, the input currents become larger, 0.5 nA typical, and are both positive except when the V_{CM} is near V^- . If operation is expected at low common-mode voltages and high temperature, do not add resistance in series with the inputs to balance the impedances. Doing this can cause an increase in offset voltage. A small resistance such as 1 k Ω can provide some protection against very large transients or overloads, and will not increase the offset significantly.

PRECISION STRAIN-GAUGE AMPLIFIER

This Strain-Gauge amplifier ([Figure 34](#)) provides high gain (1006 or ~60 dB) with very low offset and drift. Using the resistors' tolerances as shown, the worst case CMRR will be greater than 108 dB. The CMRR is directly related to the resistor mismatch. The rejection of common-mode error, at the output, is independent of the differential gain, which is set by R3. The CMRR is further improved, if the resistor ratio matching is improved, by specifying tighter-tolerance resistors, or by trimming.

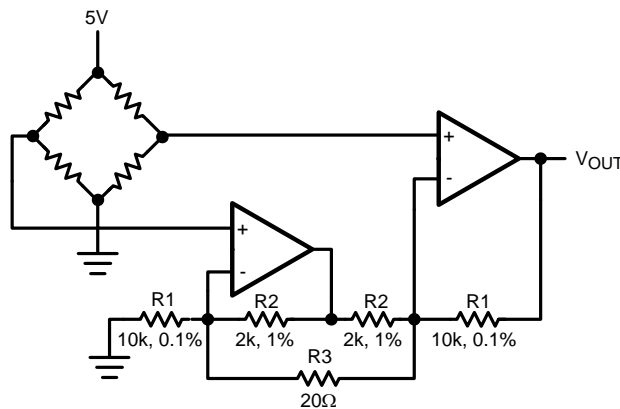


Figure 34. Precision Strain Gauge Amplifier

Extending Supply Voltages and Output Swing by Using a Composite Amplifier Configuration:

In cases where substantially higher output swing is required with higher supply voltages, arrangements like the ones shown in [Figure 35](#) and [Figure 36](#) could be used. These configurations utilize the excellent DC performance of the LMP201X while at the same time allow the superior voltage and frequency capabilities of the LM6171 to set the dynamic performance of the overall amplifier. For example, it is possible to achieve $\pm 12V$ output swing with 300 MHz of overall GBW ($A_V = 100$) while keeping the worst case output shift due to V_{OS} less than 4 mV. The LMP201X output voltage is kept at about mid-point of its overall supply voltage, and its input common mode voltage range allows the V- terminal to be grounded in one case ([Figure 35](#), inverting operation) and tied to a small non-critical negative bias in another ([Figure 36](#), non-inverting operation). Higher closed-loop gains are also possible with a corresponding reduction in realizable bandwidth. [Table 1](#) shows some other closed loop gain possibilities along with the measured performance in each case.

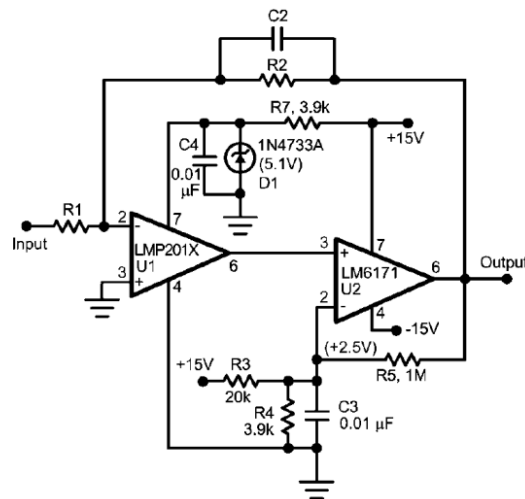


Figure 35. Composite Amplifier Configuration

Table 1. Composite Amplifier Measured Performance

A_V	R1 (Ω)	R2 (Ω)	C2 (pF)	BW (MHz)	SR (V/ μ s)	e_n p-p (mV _{PP})
50	200	10k	8	3.3	178	37
100	100	10k	10	2.5	174	70
100	1k	100k	0.67	3.1	170	70
500	200	100k	1.75	1.4	96	250
1000	100	100k	2.2	0.98	64	400

In terms of the measured output peak-to-peak noise, the following relationship holds between output noise voltage, e_n p-p, for different closed-loop gain, A_V , settings, where -3 dB Bandwidth is BW:

$$\frac{e_{npp1}}{e_{npp2}} = \sqrt{\frac{BW1}{BW2}} \cdot \frac{A_V1}{A_V2} \quad (1)$$

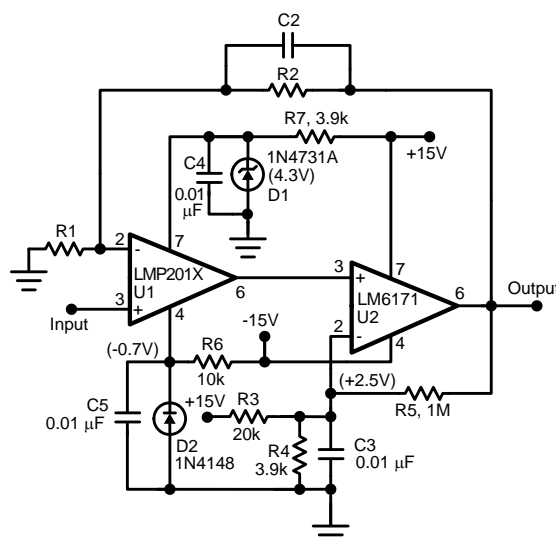


Figure 36. Composite Amplifier Configuration

It should be kept in mind that in order to minimize the output noise voltage for a given closed-loop gain setting, one could minimize the overall bandwidth. As can be seen from [Equation 1](#) above, the output noise has a square-root relationship to the Bandwidth.

In the case of the inverting configuration, it is also possible to increase the input impedance of the overall amplifier, by raising the value of R1, without having to increase the feed-back resistor, R2, to impractical values, by utilizing a "Tee" network as feedback. See the LMC6442 data sheet (Application Notes section) for more details on this.

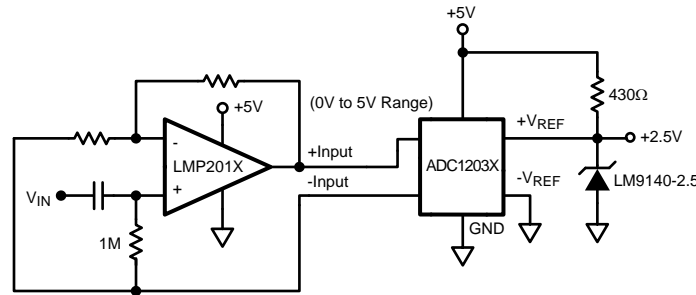


Figure 37. AC Coupled ADC Driver

LMP201X AS ADC INPUT AMPLIFIER

The LMP201X is a great choice for an amplifier stage immediately before the input of an ADC (Analog-to-Digital Converter), whether AC or DC coupled. See [Figure 37](#) and [Figure 38](#). This is because of the following important characteristics:

- A)** Very low offset voltage and offset voltage drift over time and temperature allow a high closed-loop gain setting without introducing any short-term or long-term errors. For example, when set to a closed-loop gain of 100 as the analog input amplifier for a 12-bit A/D converter, the overall conversion error over full operation temperature and 30 years life of the part (operating at 50°C) would be less than 5 LSBs.
- B)** Fast large-signal settling time to 0.01% of final value (1.4 μ s) allows 12 bit accuracy at 100 KHz or more sampling rate
- C)** No flicker (1/f) noise means unsurpassed data accuracy over any measurement period of time, no matter how long. Consider the following op amp performance, based on a typical low-noise, high-performance commercially-available device, for comparison:
 Op amp flatband noise = 8nV/ $\sqrt{\text{Hz}}$
 1/f corner frequency = 100 Hz
 A_V = 2000
 Measurement time = 100 sec
 Bandwidth = 2 Hz
 This example will result in about 2.2 mV_{PP} (1.9 LSB) of output noise contribution due to the op amp alone, compared to about 594 μ V_{PP} (less than 0.5 LSB) when that op amp is replaced with the LMP201X which has no 1/f contribution. If the measurement time is increased from 100 seconds to 1 hour, the improvement realized by using the LMP201X would be a factor of about 4.8 times (2.86 mV_{PP} compared to 596 μ V when LMP201X is used) mainly because the LMP201X accuracy is not compromised by increasing the observation time.
- D)** Copper leadframe construction minimizes any thermocouple effects which would degrade low level/high gain data conversion application accuracy (see discussion under [The Benefits of the LMP201X](#) section above).
- E)** Rail-to-Rail output swing maximizes the ADC dynamic range in 5-Volt single-supply converter applications. Below are some typical block diagrams showing the LMP201X used as an ADC amplifier ([Figure 37](#) and [Figure 38](#)).

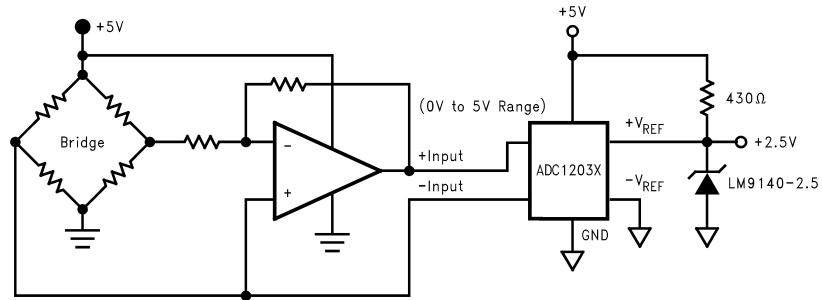


Figure 38. DC Coupled ADC Driver

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
LMP2011MA	ACTIVE	SOIC	D	8	95	TBD	CU SNPB	Level-1-235C-UNLIM	-40 to 125	LMP20 11MA	Samples
LMP2011MA/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LMP20 11MA	Samples
LMP2011MAX	ACTIVE	SOIC	D	8	2500	TBD	CU SNPB	Level-1-235C-UNLIM	-40 to 125	LMP20 11MA	Samples
LMP2011MAX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LMP20 11MA	Samples
LMP2011MF	ACTIVE	SOT-23	DBV	5	1000	TBD	CU SNPB	Level-1-260C-UNLIM	-40 to 125	AN1A	Samples
LMP2011MF/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	AN1A	Samples
LMP2011MFX	ACTIVE	SOT-23	DBV	5	3000	TBD	CU SNPB	Level-1-260C-UNLIM	-40 to 125	AN1A	Samples
LMP2011MFX/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	AN1A	Samples
LMP2012MA	ACTIVE	SOIC	D	8	95	TBD	CU SNPB	Level-1-235C-UNLIM	-40 to 125	LMP20 12MA	Samples
LMP2012MA/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LMP20 12MA	Samples
LMP2012MAX	ACTIVE	SOIC	D	8	2500	TBD	CU SNPB	Level-1-235C-UNLIM	-40 to 125	LMP20 12MA	Samples
LMP2012MAX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LMP20 12MA	Samples
LMP2012MM	ACTIVE	VSSOP	DGK	8	1000	TBD	CU SNPB	Level-1-260C-UNLIM	-40 to 125	AP1A	Samples
LMP2012MM/NOPB	ACTIVE	VSSOP	DGK	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	AP1A	Samples
LMP2012MMX	ACTIVE	VSSOP	DGK	8	3500	TBD	CU SNPB	Level-1-260C-UNLIM	-40 to 125	AP1A	Samples
LMP2012MMX/NOPB	ACTIVE	VSSOP	DGK	8	3500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	AP1A	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

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Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ Only one of markings shown within the brackets will appear on the physical device.

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*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMP2011MAX	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LMP2011MAX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LMP2011MF	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMP2011MF/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMP2011MFX	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMP2011MFX/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMP2012MAX	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LMP2012MAX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LMP2012MM	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMP2012MM/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMP2012MMX	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMP2012MMX/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

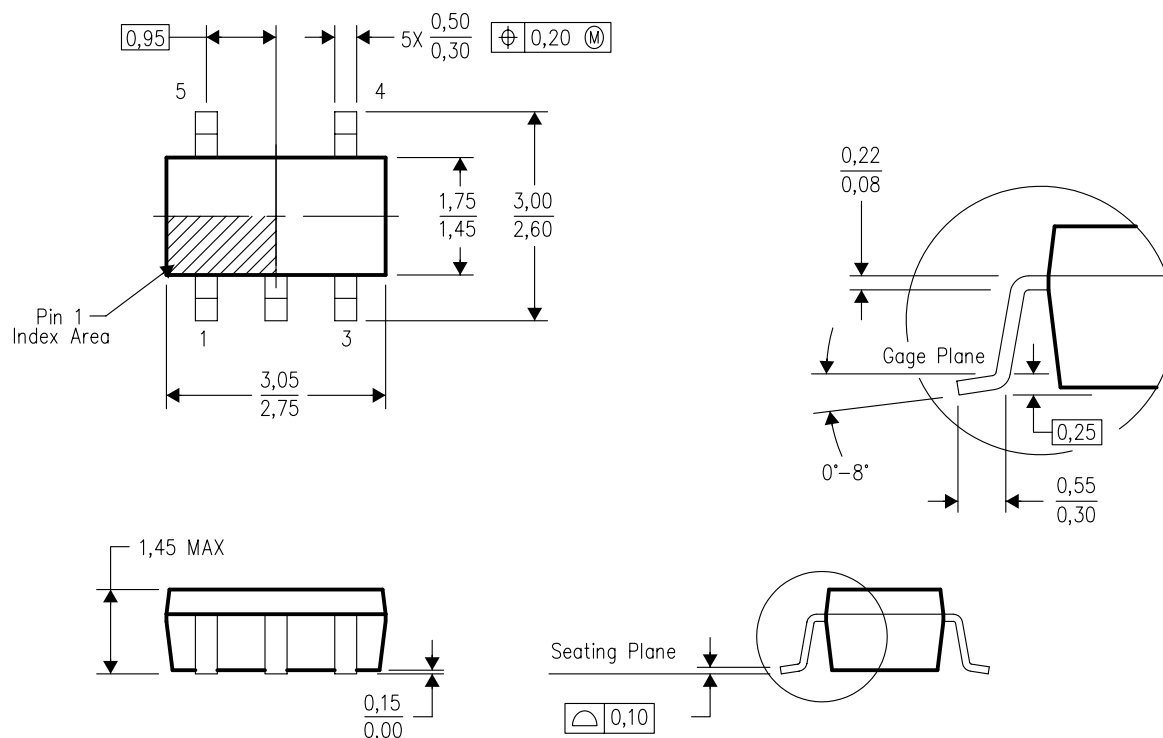


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMP2011MAX	SOIC	D	8	2500	349.0	337.0	45.0
LMP2011MAX/NOPB	SOIC	D	8	2500	349.0	337.0	45.0
LMP2011MF	SOT-23	DBV	5	1000	203.0	190.0	41.0
LMP2011MF/NOPB	SOT-23	DBV	5	1000	203.0	190.0	41.0
LMP2011MFX	SOT-23	DBV	5	3000	206.0	191.0	90.0
LMP2011MFX/NOPB	SOT-23	DBV	5	3000	206.0	191.0	90.0
LMP2012MAX	SOIC	D	8	2500	349.0	337.0	45.0
LMP2012MAX/NOPB	SOIC	D	8	2500	349.0	337.0	45.0
LMP2012MM	VSSOP	DGK	8	1000	203.0	190.0	41.0
LMP2012MM/NOPB	VSSOP	DGK	8	1000	203.0	190.0	41.0
LMP2012MMX	VSSOP	DGK	8	3500	349.0	337.0	45.0
LMP2012MMX/NOPB	VSSOP	DGK	8	3500	349.0	337.0	45.0

DBV (R-PDSO-G5)

PLASTIC SMALL-OUTLINE PACKAGE



4073253-4/K 03/2006

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 mm per side.
 - D. Falls within JEDEC MO-178 Variation AA.

DBV (R-PDSO-G5)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
 - D. Publication IPC-7351 is recommended for alternate designs.
 - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

DGK (S-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



4073329/E 05/06

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
 - E. Falls within JEDEC MO-187 variation AA, except interlead flash.

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - $\triangle C$ Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - $\triangle D$ Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AA.

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