

Micropower Precision Comparator and Precision Reference with Adjustable Hysteresis

Check for Samples: [LMP7300](#)

FEATURES

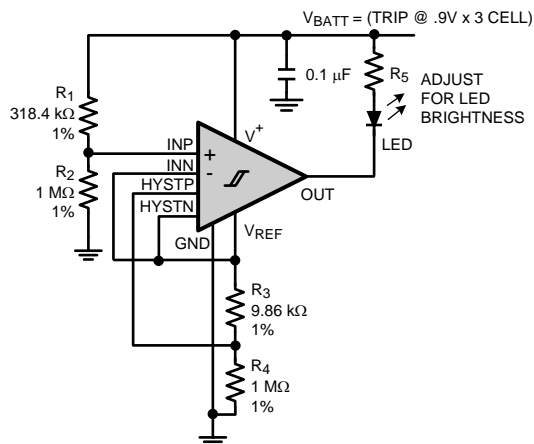
- (For $V_S = 5V$, typical unless otherwise noted)
- Supply Current 13 μA
- Propagation Delay 4 μs
- Input Offset Voltage 0.3 mV
- CMRR 100 dB
- PSRR 100 dB
- Positive and Negative Hysteresis Control
- Adjustable Hysteresis 1 mV/mV
- Reference Voltage 2.048V
- Reference Voltage Accuracy 0.25%
- Reference Voltage Source Current 1 mA
- Wide Supply Voltage Range 2.7V to 12V
- Operating Temperature Range Ambient $-40^{\circ}C$ to $125^{\circ}C$

APPLICATIONS

- Precision Threshold Detection
- Battery Monitoring
- Battery Management Systems
- Zero Crossing Detectors

Typical Application

Micropower Precision Battery Low Voltage Detector for 3 Cell Discharge Voltage



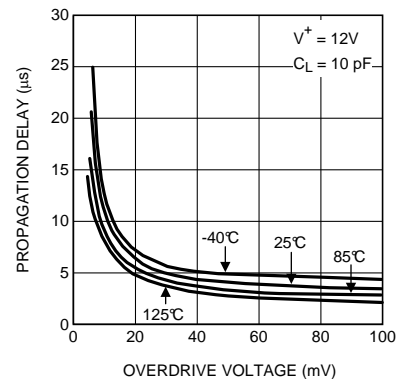
DESCRIPTION

The LMP7300 is a combination comparator and reference with ideal specifications for precision threshold detecting. The precision 2.048V reference comes with a 0.25% maximum error. The comparator features micropower (35 μW), low offset voltage (0.75 mV max), and independent adjustable positive and negative hysteresis.

Hysteresis control for the comparator is accomplished through two external pins. The HYSTP pin sets the positive hysteresis and the HYSTN pin sets the negative hysteresis. The comparator design isolates the V_{IN} source impedance and the programmable hysteresis components. This isolation prevents any undesirable interaction allowing the IC to maintain a precise threshold voltage during level detection.

The combination of low offset voltage, external hysteresis control, and precision voltage reference provides an easy to use micropower precision threshold detector.

The LMP7300 open collector output makes it ideal for mixed voltage system designs. The output voltage upper rail is unconstrained by V_{CC} and can be pulled above V_{CC} to a maximum of 12V. The LMP7300 is a member of the LMP precision amplifier family.



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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings⁽¹⁾⁽²⁾

| | | |
|--------------------------------------|------------------------------------|--------------------------|
| ESD Tolerance ⁽³⁾ | Human Body Model | 2000V |
| | Machine Model | 200V |
| V_{IN} Differential | | $\pm V_S$ |
| Supply Voltage ($V_S = V^+ - V^-$) | | 13.6V |
| Voltage at Input/Output Pins | | $V^+ + 0.3V, V^- - 0.3V$ |
| Storage Temperature Range | | -65°C to +150°C |
| Junction Temperature ⁽⁴⁾ | | +150°C |
| Soldering Information | Infrared or Convection (20 sec) | 235°C |
| | Wave Soldering Lead Temp. (10 sec) | 260°C |

- (1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics Tables.
- (2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
- (3) Human Body Model, applicable std. MIL-STD-883, Method 3015.7. Machine Model, applicable std. JESD22-A115-A (ESD MM std. of JEDEC) Field-Induced Charge-Device Model, applicable std. JESD22-C101-C (ESD FICDM std. of JEDEC).
- (4) The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA} . The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A) / \theta_{JA}$. All numbers apply for packages soldered directly onto a PC Board.

Operating Ratings⁽¹⁾

| | | |
|---|-------------|----------------|
| Temperature Range ⁽²⁾ | | -40°C to 125°C |
| Supply Voltage ($V_S = V^+ - V^-$) | | 2.7V to 12V |
| Package Thermal Resistance (θ_{JA}) ⁽²⁾ | 8-Pin SOIC | 166°C/W |
| | 8-Pin VSSOP | 235°C/W |

- (1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics Tables.
- (2) The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA} . The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A) / \theta_{JA}$. All numbers apply for packages soldered directly onto a PC Board.

2.7V Electrical Characteristics⁽¹⁾

Unless otherwise specified, all limits are guaranteed for $T_A = 25^\circ\text{C}$, $V^+ = 2.7\text{V}$, $V^- = 0\text{V}$, and $V_{CM} = V^+/2$, $R_{PULLUP} = 100\text{ k}\Omega$, $C_{LOAD} = 10\text{ pF}$. **Boldface** limits apply at the temperature extremes.

| Symbol | Parameter | Conditions | Min ⁽²⁾ | Typ ⁽³⁾ | Max ⁽²⁾ | Units |
|-----------------------|--------------------------------------|---|--------------------|--------------------|--------------------|-------------------|
| I _S | Supply Current | R _{PULLUP} = Open | | 9 | 12 17 | μA |
| Comparator | | | | | | |
| V _{OS} | Input Offset Voltage | V _{CM} = V ⁺ /2 SOIC | | ±0.07 | ±0.75 ±2 | mV |
| | | V _{CM} = V ⁺ /2 VSSOP | | ±0.07 | ±1.0 ±2.2 | mV |
| TCV _{OS} | Input Offset Average Drift | See ⁽⁴⁾ | | 1.8 | | μV/°C |
| I _B | Input Bias Current ⁽⁵⁾ | V _{ID} < 2.5V | | 1.2 | 3 4 | nA |
| I _{OS} | Input Offset Current | | | 0.15 | 0.5 | nA |
| CMRR | Common Mode Rejection Ratio | 1V < V _{CM} < 2.7V | 80 | 100 | | dB |
| PSRR | Power Supply Rejection Ratio | V ⁺ = 2.7V to 12V | 80 | 100 | | dB |
| V _{OL} | Output Low Voltage | I _{LOAD} = 10 mA | | 0.25 | 0.4 0.5 | V |
| I _{LEAK} | Output Leakage Current | Comparator Output in High State | | 1 | | pA |
| HC _{LIN} | Hysteresis Control Voltage Linearity | 0 < Ref-H _{YS} TP,N < 25 mV | | 1.000 | | mV/V |
| | | 25 mV < Ref-H _{YS} TP,N < 100 mV | | 0.950 | | |
| I _{HYS} | Hysteresis Leakage Current | | | 1.2 | 3 4 | nA |
| T _{PD} | Propagation Delay (High to Low) | Overdrive = 10 mV, C _L = 10 pF | | 12 | 17 | μs |
| | | Overdrive = 100 mV, C _L = 10 pF | | 4.5 | 7.6 | |
| Reference | | | | | | |
| V _O | Reference Voltage | SOIC | 2.043 | 2.048 | 2.053 | V |
| | | VSSOP | 2.043 | 2.048 | 2.056 | V |
| | Line Regulation | V _{CC} = 2.7V to 12V | | 14 | 80 | μV/V |
| | Load Regulation | I _{OUT} = 0 to 1 mA | | 0.2 | 0.5 | mV/mA |
| TCV _{REF/°C} | Temperature Coefficient | −40°C to 125°C | | | 55 | ppm/°C |
| V _N | Output Noise Voltage | 0.1 Hz to 10 Hz | | 80 | | μV _{PP} |
| | | 10 Hz to 10 kHz | | 100 | | μV _{RMS} |

- (1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that $T_J = T_A$. No guarantee of parametric performance is indicated in the electrical tables under conditions of internal self-heating where $T_J > T_A$.
- (2) Limits are 100% production tested at 25°C . Limits over the operating temperature range are guaranteed through correlations using statistical quality control (SQC) method.
- (3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not guaranteed on shipped production material.
- (4) Offset voltage average drift determined by dividing the change in V_{OS} at temperature extremes, by the total temperature change.
- (5) Positive current corresponds to current flowing into the device.

5V Electrical Characteristics⁽¹⁾

Unless otherwise specified, all limits are guaranteed for $T_A = 25^\circ\text{C}$, $V^+ = 5\text{V}$, $V^- = 0\text{V}$, and $V_{\text{CM}} = V^+/2$, $R_{\text{PULLUP}} = 100\text{ k}\Omega$, $C_{\text{LOAD}} = 10\text{ pF}$. **Boldface** limits apply at the temperature extremes.

| Symbol | Parameter | Conditions | Min ⁽²⁾ | Typ ⁽³⁾ | Max ⁽²⁾ | Units |
|-----------------------|--------------------------------------|--|--------------------|--------------------|--------------------|-------------------|
| I _S | Supply Current | R _{PULLUP} = Open | | 10 | 13 18 | μA |
| Comparator | | | | | | |
| V _{OS} | Input Offset Voltage | V _{CM} = V ⁺ /2 SOIC | | ±0.07 | ±0.75 ±2 | mV |
| | | V _{CM} = V ⁺ /2 VSSOP | | ±0.07 | ±1.0 ±2.2 | mV |
| TCV _{OS} | Input Offset Average Drift | See ⁽⁴⁾ | | 1.8 | | μV/°C |
| I _B | Input Bias Current ⁽⁵⁾ | V _{ID} < 2.5V | | 1.2 | 3 4 | nA |
| I _{OS} | Input Offset Current | | | 0.15 | 0.5 | nA |
| CMRR | Common Mode Rejection Ratio | 1 ≤ V _{CM} ≤ 5V | 80 | 100 | | dB |
| PSRR | Power Supply Rejection Ratio | V ⁺ = 2.7V to 12V | 80 | 100 | | dB |
| V _{OL} | Output Voltage Low | I _{LOAD} = 10 mA | | 0.25 | 0.4 | V |
| I _{LEAK} | Output Leakage Current | Comparator Output in High State | | 1 | | pA |
| HC _{LIN} | Hysteresis Control Voltage Linearity | 0 < Ref-V _{HYS} TP,N < 25 mV | | 1.000 | | mV/V |
| | | 25 mV < Ref-V _{HYS} TP,N < 100 mV | | 0.950 | | |
| I _{HYS} | Hysteresis Leakage Current | | | 1.2 | 3 4 | nA |
| TPD | Propagation Delay (High to Low) | Overdrive = 10 mV, C _L = 10 pF | | 12 | 15 | μs |
| | | Overdrive = 100 mV, C _L = 10 pF | | 4 | 7 | |
| Reference | | | | | | |
| V _O | Reference Voltage | SOIC | 2.043 | 2.048 | 2.053 | V |
| | | VSSOP | 2.043 | 2.048 | 2.056 | V |
| | Line Regulation | V _{CC} = 2.7V to 12V | | 14 | 80 | μV/V |
| | Load Regulation | I _{OUT} = 0 to 1 mA | | 0.2 | 0.5 | mV/mA |
| TCV _{REF/°C} | Temperature Coefficient | −40°C to 125°C | | | 55 | ppm/°C |
| V _N | Output Noise Voltage | 0.1 Hz to 10 Hz | | 80 | | μV _{PP} |
| | | 10 Hz to 10 kHz | | 100 | | μV _{RMS} |

- (1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that $T_J = T_A$. No guarantee of parametric performance is indicated in the electrical tables under conditions of internal self-heating where $T_J > T_A$.
- (2) Limits are 100% production tested at 25°C . Limits over the operating temperature range are guaranteed through correlations using statistical quality control (SQC) method.
- (3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not guaranteed on shipped production material.
- (4) Offset voltage average drift determined by dividing the change in V_{OS} at temperature extremes, by the total temperature change.
- (5) Positive current corresponds to current flowing into the device.

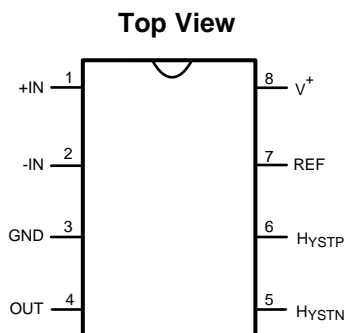
12V Electrical Characteristics⁽¹⁾

Unless otherwise specified, all limits are guaranteed for $T_A = 25^\circ\text{C}$, $V^+ = 12\text{V}$, $V^- = 0\text{V}$, and $V_{CM} = V^+/2$, $R_{PULLUP} = 100\text{ k}\Omega$, $C_{LOAD} = 10\text{ pF}$. **Boldface** limits apply at the temperature extremes.

| Symbol | Parameter | Conditions | Min ⁽²⁾ | Typ ⁽³⁾ | Max ⁽²⁾ | Units |
|-----------------------|--------------------------------------|--|--------------------|--------------------|--------------------|-------------------|
| I _S | Supply Current | R _{PULLUP} = Open | | 11 | 14 20 | μA |
| Comparator | | | | | | |
| V _{OS} | Input Offset Voltage | V _{CM} = V ⁺ /2 SOIC | | ±0.08 | ±0.75 ±2 | mV |
| | | V _{CM} = V ⁺ /2 VSSOP | | ±0.08 | ±1.0 ±2.2 | mV |
| TCV _{OS} | Input Offset Average Drift | See ⁽⁴⁾ | | 1.8 | | μV/°C |
| I _B | Input Bias Current ⁽⁵⁾ | V _{ID} > 2.5V | | 1.2 | 3 4 | nA |
| I _{OS} | Input Offset Current | | | 0.15 | 0.5 | nA |
| CMRR | Common Mode Rejection Ratio | 1V ≤ V _{CM} ≤ 12V | 80 | 100 | | dB |
| PSRR | Power Supply Rejection Ratio | V ⁺ = 2.7V to 12V | 80 | 100 | | dB |
| V _{OL} | Output Voltage Low | I _{LOAD} = 10 mA | | 0.25 | 0.4 | V |
| I _{LEAK} | Output Leakage Current | Comparator Output in High State | | 1 | | pA |
| H _{CLIN} | Hysteresis Control Voltage Linearity | 0 < Ref-V _{+HYS} TP, N < 25 mV | | 1.000 | | mV/V |
| | | 25 mV < Ref-V _{+HYS} TP, N < 100 mV | | 0.950 | | |
| I _{HYS} | Hysteresis Leakage Current | | | 1.2 | 3 4 | nA |
| TPD | Propagation Delay (High to Low) | Overdrive = 10 mV, C _L = 10 pF | | 11 | 15 | μs |
| | | Overdrive = 100 mV, C _L = 10 pF | | 3.5 | 6.8 | |
| Reference | | | | | | |
| V _O | Reference Voltage | T _J = 25°C SOIC | 2.043 | 2.048 | 2.053 | V |
| | | T _J = 25°C VSSOP | 2.043 | 2.048 | 2.056 | V |
| | Line Regulation | V _{CC} = 2.7V to 12V | | 14 | 80 | μV/V |
| | Load Regulation | I _{OUT} = 0 to 1 mA | | 0.2 | 0.5 | mV/mA |
| TCV _{REF/°C} | Temperature Coefficient | −40°C to +125°C | | | 55 | ppm/°C |
| V _N | Output Noise Voltage | 0.1 Hz to 10 Hz | | 80 | | μV _{PP} |
| | | 10 Hz to 10 kHz | | 100 | | μV _{RMS} |

- (1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that $T_J = T_A$. No guarantee of parametric performance is indicated in the electrical tables under conditions of internal self-heating where $T_J > T_A$.
- (2) Limits are 100% production tested at 25°C . Limits over the operating temperature range are guaranteed through correlations using statistical quality control (SQC) method.
- (3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not guaranteed on shipped production material.
- (4) Offset voltage average drift determined by dividing the change in V_{OS} at temperature extremes, by the total temperature change.
- (5) Positive current corresponds to current flowing into the device.

CONNECTION DIAGRAM



**Figure 1. 8-Pin VSSOP (See DGK Package)
8-Pin SOIC (See D Package)**

Pin Descriptions

| Symbol | Pin Name | Description |
|--------|--------------------------------|--|
| +IN | Non-Inverting Comparator Input | The +IN has a common-mode voltage range from 1V above the negative rail to, and including, the positive rail. Internal ESD diodes, connected from the +IN pin to the rails, protect the input stage from overvoltage. If the input voltage exceeds the rails, the diodes turn on and clamp the input to a safe level. |
| -IN | Inverting Comparator Input | The -IN has a common-mode voltage range from 1V above the negative rail to, and including, the positive rail. Internal ESD diodes, connected from the -IN pin to the rails, protects the input stage from overvoltage. If the input voltage exceeds the rails, the diodes turn on and clamp the input to a safe level. |
| GND | Ground | This pin may be connected to a negative DC voltage source for applications requiring a dual supply. If connected to a negative supply, decouple this pin with 0.1 μ F ceramic capacitor to ground. The internal reference output voltage is referenced to this pin. GND is the die substrate connection. |
| OUT | Comparator Output | The output is an open-collector. It can drive voltage loads by using a pullup resistor, or it can drive current loads by sinking a maximum output current. This pin may be taken to a maximum of +12V with respect to the ground pin, irrespective of supply voltage. |
| HYSTN | Negative Hysteresis Pin | This pin sets the lower trip voltage V_{IL} . The common mode range is from 1V above the negative rail to V_{CC} . The input signal must fall below V_{IL} for the comparator to switch from high to low state. |
| HYSTP | Positive Hysteresis pin | This pin sets the upper trip voltage V_{IH} . The common mode range is from 1V above the negative rail to V_{CC} . The input signal must rise above V_{IH} for the comparator to switch from low to high state. |
| REF | Reference Voltage Output Pin | This is the output pin of a 2.048V band gap precision reference. |
| V+ | Positive Supply Terminal | The supply voltage range is 2.7V to 12V. Decouple this pin with 0.1 μ F ceramic capacitor to ground. |

Typical Performance Characteristics

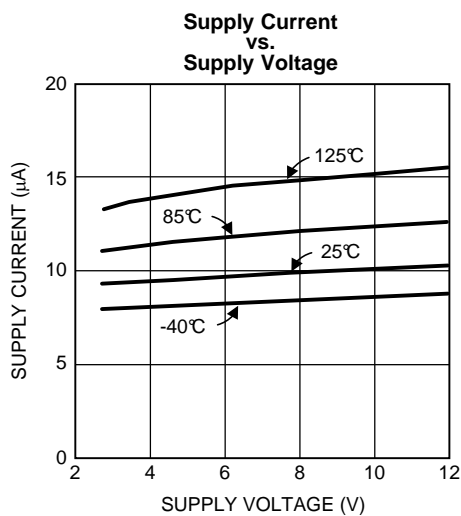


Figure 2.

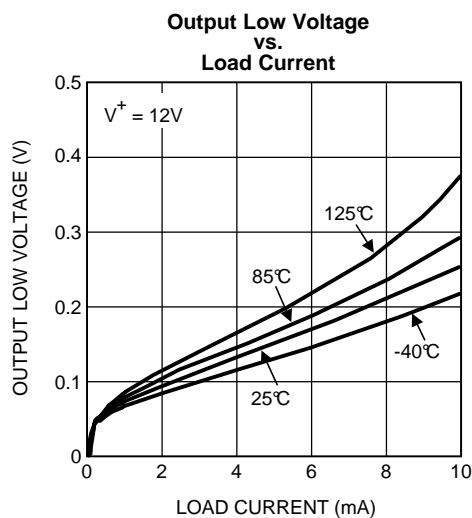


Figure 3.

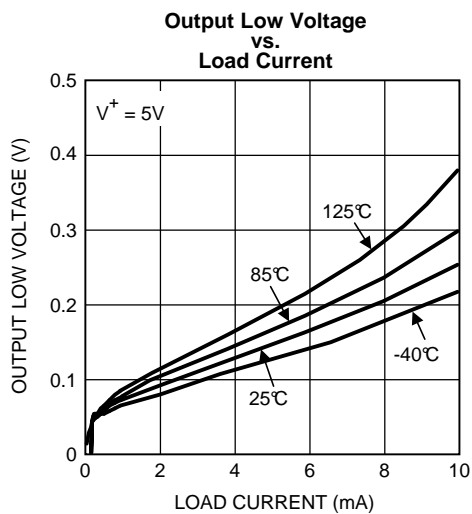


Figure 4.

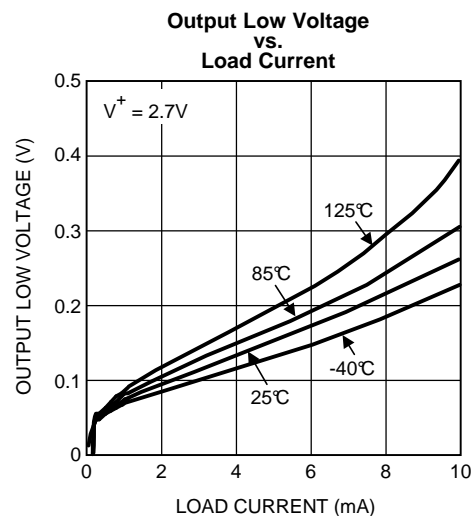


Figure 5.

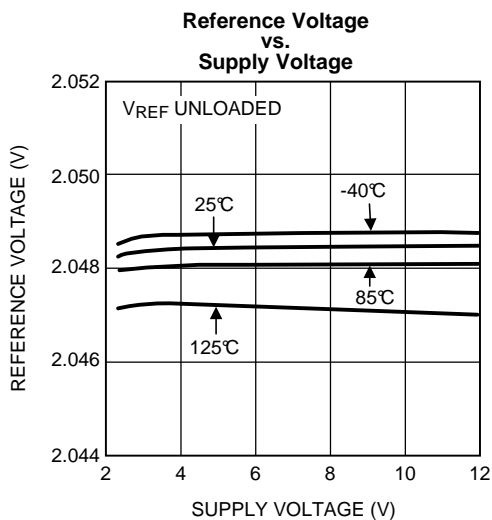


Figure 6.

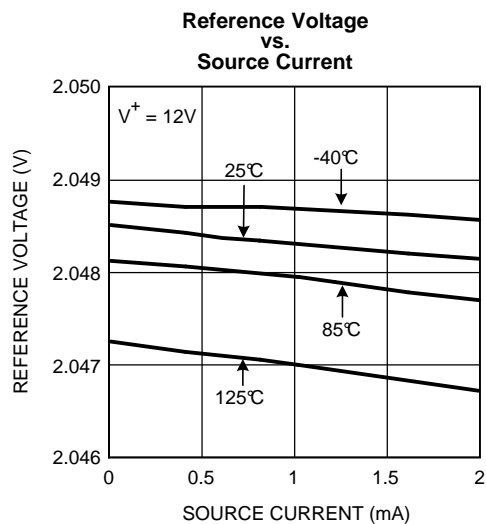
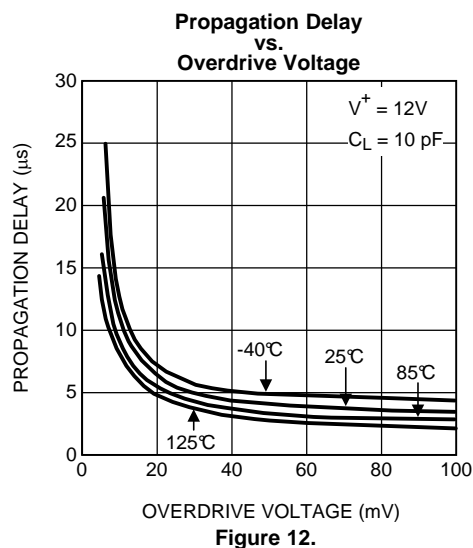
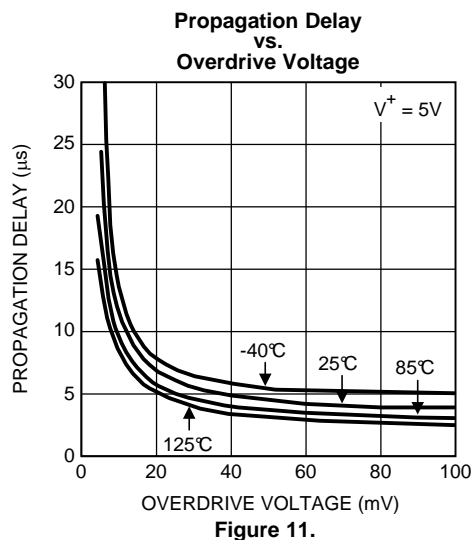
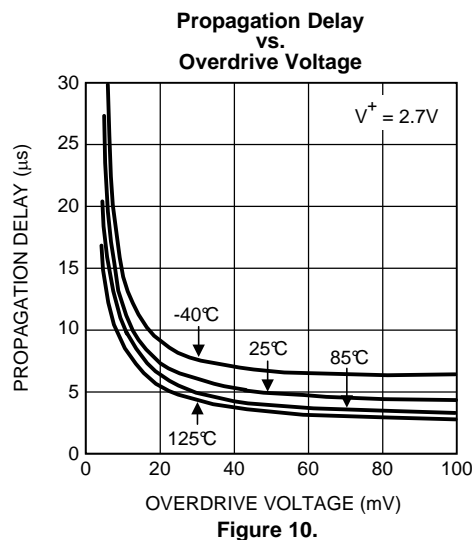
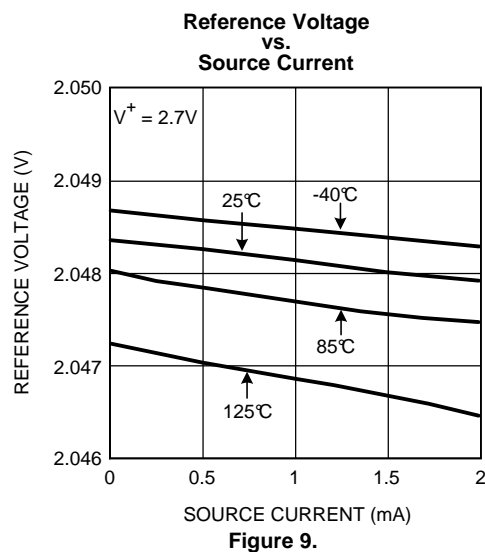
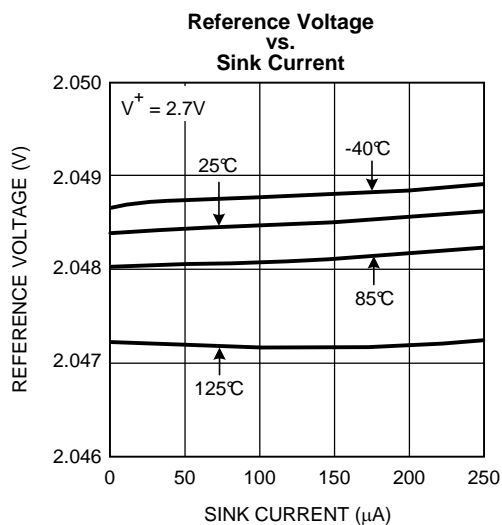


Figure 7.

Typical Performance Characteristics (continued)



APPLICATION INFORMATION

GENERAL DESCRIPTION

The LMP7300 is a unique combination of micropower and precision. The open collector comparator has low offset, high CMRR, high PSRR, programmable hysteresis and microamp supply current. The precision 2.048V reference provides a DAC or ADC with an accurate binary divisible voltage. The comparator and reference combination forms an ideal single IC solution for low power sensor or portable applications.

VOLTAGE REFERENCE

The reference output voltage is a band gap derived 2.048V that is trimmed to achieve typically 0.2% accuracy over the full operating temperature range of -40°C to 125°C . The trim procedure employs a curvature correction algorithm to compensate for the base emitter thermal nonlinearity inherent in band gap design topologies. The reference accuracy and the set resistor tolerance determine the magnitude and precision of the programmable hysteresis. In situations where reference noise filtering is required a 5 μF capacitor in series with a 190 Ω resistor to ground are recommended.

COMPARATOR

Output Stage

The comparator employs an open collector output stage that can switch microamp loads for micropower precision threshold detection to applications requiring activating a solenoid, a lamp, or an LED. The wired-OR type output easily interfaces to TTL, CMOS, or multiple outputs, as in a window comparator application, over a range of 0.5V to 12V. The output is capable of driving greater than 10 mA output current and yet maintaining a saturation voltage below 0.4V over temperature. The supply current increases linearly when driving heavy loads so a pullup resistor of 100 k Ω or greater is recommended for micropower applications.

Fault Detection Rate

The user's choice of a pullup resistor and capacitive load determines the minimum response time and the event detection rate. By optimizing overdrive, the pullup resistor and capacitive load fault update rates of 200 kHz to 250 kHz or greater can be achieved.

HYSTERESIS

False triggering on noise coupled into the signal path is a common problem for comparator based threshold detectors. One of the most effective solutions is to add hysteresis. Hysteresis is a circuit signal path characteristic where an amplitude delay is introduced to the normal input. Positive hysteresis forces the signal to pass the normal switch point before the output makes a low to high transition while negative hysteresis does the opposite. This is a memory effect. The comparator behaves differently based on which direction the signal is going.

The LM7300 has been designed with a unique way of introducing hysteresis. The set points are completely independent of each other, the power supply, and the input or output conditions. The HYSTP pin sets positive hysteresis and the HYSTN pin sets the negative hysteresis in a simple way using two resistors. The pins can be tied together for the same hysteresis or tied to separate voltage taps for asymmetric hysteresis, or tied to the reference for no hysteresis. When the precision reference is used to drive the voltage tap resistor divider precise, stable threshold levels can be obtained. The maximum recommended hysteresis is about 130 mV. This places the HYSTP and HYSTN pin voltages at $V_{\text{REF}} - 130\text{ mV}$ which is approximately the center of their input common mode range at 2.7V. For the typical example, a differential input signal voltage, V_{IN} , is applied between INP and INN, the non-inverting and inverting inputs of the comparator. A DC switch or threshold voltage, V_{TH} , is set on the negative input to keep the output off when the signal is above and on when it goes below this level. For a precision threshold tie the INN pin to V_{REF} . With the output, off the circuit is in the minimum power state. [Figure 14](#) through [Figure 22](#) demonstrate the different configurations for setting the upper threshold V_{IH} and the lower threshold V_{IL} and their relationship to the input trip point V_{REF} , by the following formulas.

$$V_{IL} = V_{REF} - V_{REF} \left(\frac{R_1}{R_1 + R_2} \right)$$

$$V_{IH} = V_{REF} + V_{REF} \left(\frac{R_1}{R_1 + R_2} \right)$$

(1)

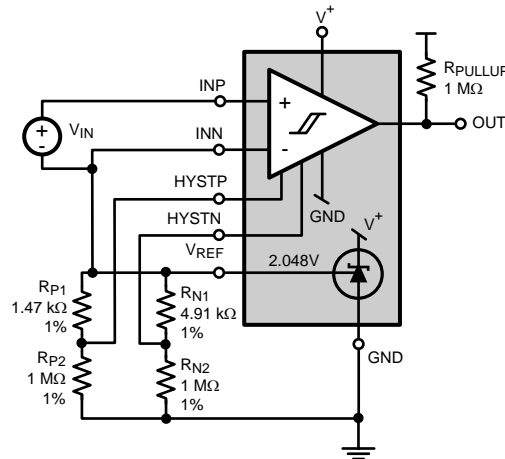


Figure 13. Typical Micropower Application to Set Asymmetric Positive and Negative Hysteresis of -10 mV, +3 mV

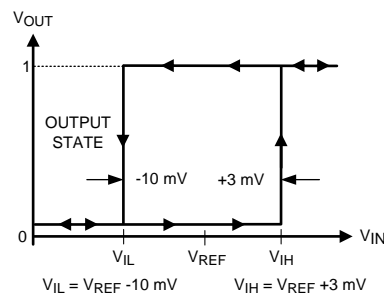


Figure 14. Typical Micropower Application to Set Asymmetric Positive and Negative Hysteresis of -10 mV, +3 mV

When $V_{ID} = 0$, $INN = INP = V_{TH}$

Figure 16 shows the configuration with no hysteresis when the HYSTP and HYSTN pins are connected together to V_{REF} . This configuration is not recommended because it has the highest level of false triggers due to the system noise.

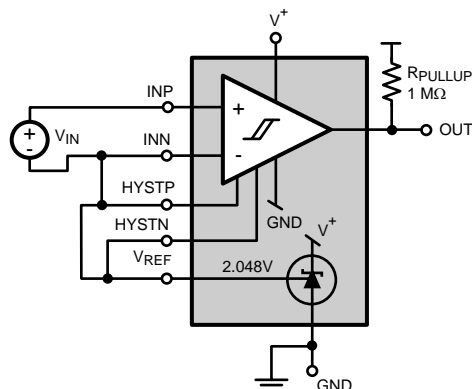


Figure 15. Typical Configuration for No Hysteresis

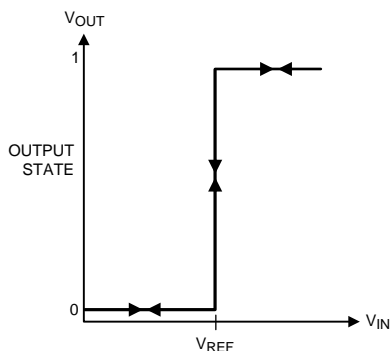


Figure 16. Typical Configuration for No Hysteresis

Figure 18 shows the configuration with symmetric hysteresis when the HYSTP and HYSTN pins are connected to the same voltage that is less than V_{REF} . The two trip points set a hysteresis band around the input threshold voltage V_{REF} , such that the positive band is equal to the negative band.

This configuration controls the false triggering mentioned in Figure 16. Symmetric hysteresis values less than 5 mV to 10 mV are recommended for precise level detection applications.

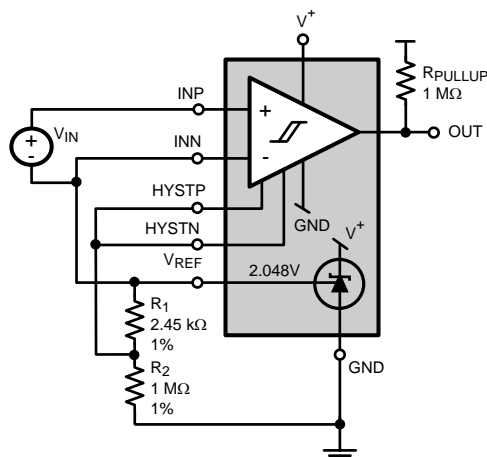


Figure 17. Symmetric Hysteresis ± 5 mV

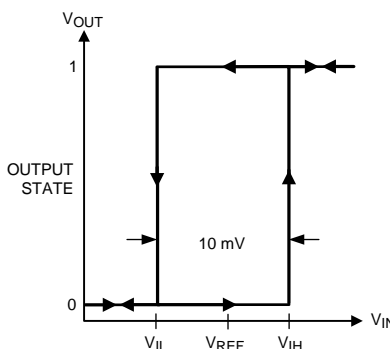


Figure 18. Symmetric Hysteresis ± 5 mV

Figure 20 shows the case for negative hysteresis by biasing only the HYSN pin to a voltage less than V_{REF} .

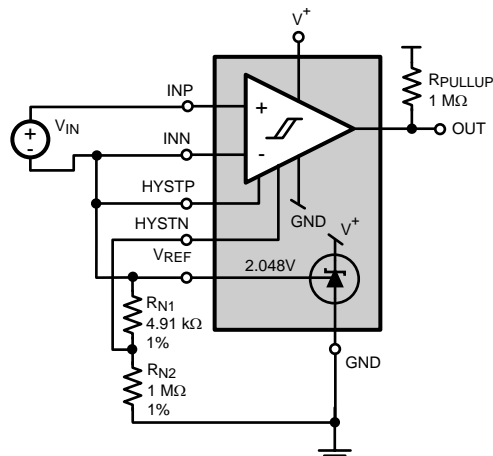


Figure 19. Typical Configuration for Negative Hysteresis = -10 mV

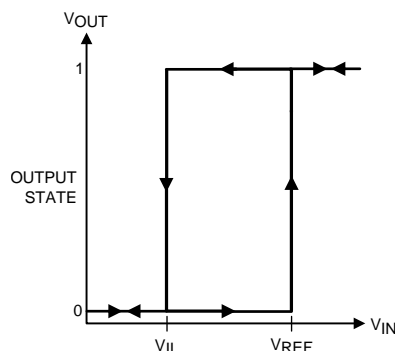


Figure 20. Typical Configuration for Negative Hysteresis = -10 mV

The case for setting only a positive hysteresis is demonstrated in [Figure 22](#).

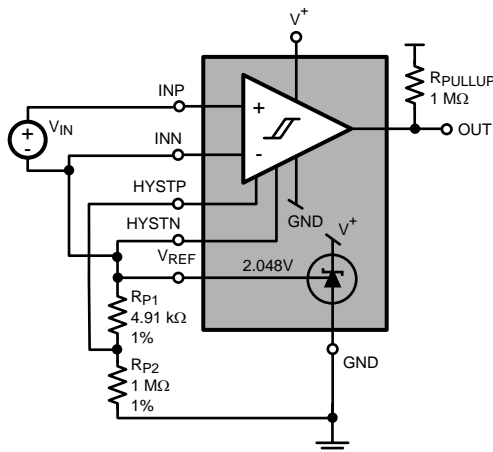


Figure 21. Connections for Positive Hysteresis = +10 mV

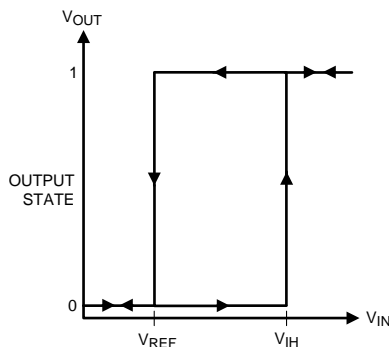


Figure 22. Connections for Positive Hysteresis = +10 mV

In the general case, as demonstrated with both positive and negative hysteresis bands in Figure 23, noise within these bands will have no effect on the state of the comparator output. In Example #1 the noise is well behaved and in band. The output is clean and well behaved. In Example #2, a significant amount of out of band noise is present but due to hysteresis no false triggers occur on the rising positive or falling negative edges. The hysteresis forces the signal level to move higher or lower before the output is set to the opposite state.

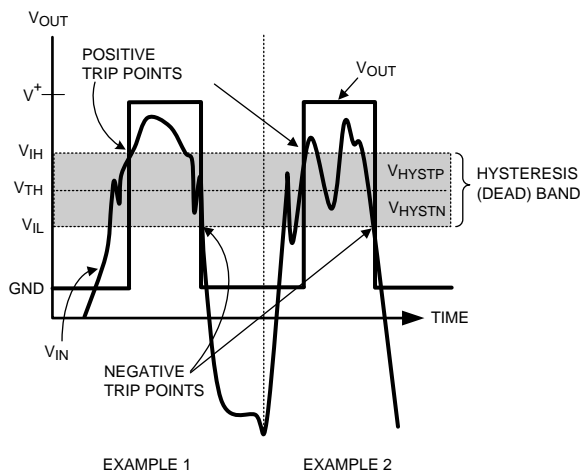


Figure 23. Output Response with Input Noise Less than Hysteresis Band

How Much Hysteresis Is Correct?

An effective way of determining the minimum hysteresis necessary for clean switching is to decrease the amount of hysteresis until false triggering is observed, and then use a multiple of say three times that amount of hysteresis in the final circuit. This is most easily accomplished in the breadboard phase by making R_1 and R_2 potentiometers. For applications near or above +100°C a minimum of 5 mV hysteresis is recommended due to peaking of the LMP7300 noise sensitivity at high temperatures.

LAYOUT RECOMMENDATIONS

A good PCB layout is always important to reduce output to input coupling. Positive feedback noise reduces performance. For the LMP7300 output coupling is minimized by the unique package pinout. The output is kept away from the non-inverting and inverting inputs, the reference and the hysteresis pins.

EVALUATION BOARDS

Texas Instruments provides the following PCB boards as an aid in evaluating the LMP7300 performance.

| Device | Package | Evaluation Board Ordering ID |
|-----------|------------|------------------------------|
| LMP7300MA | 8-Pin SOIC | LMP7300MA-EVAL |

WINDOW COMPARATOR

Figure 25 shows two LMP7300s configured as a micropower window detector in a temperature level detection application. The circuit shown monitors the ambient temperature change. If the temperature rises outside the 15°C to 35°C window, either comparator 1 for high temp, or comparator 2 for low temp, will set low, indicating a fault condition has occurred. The open collector outputs are pulled up separately but can be wire-OR'd for a single fault indication. If the temperature returns inside the window it must overcome the 22 mV asymmetric hysteresis band established on either comparator. For the high side the temperature must drop below 34°C and for the low side the temperature must rise above 16°C for the outputs to reset high and remove the fault indication. The temperature is sensed by a 30 kΩ @ 25°C Omega Precision NTC Thermistor #44008 (±0.2% tol).

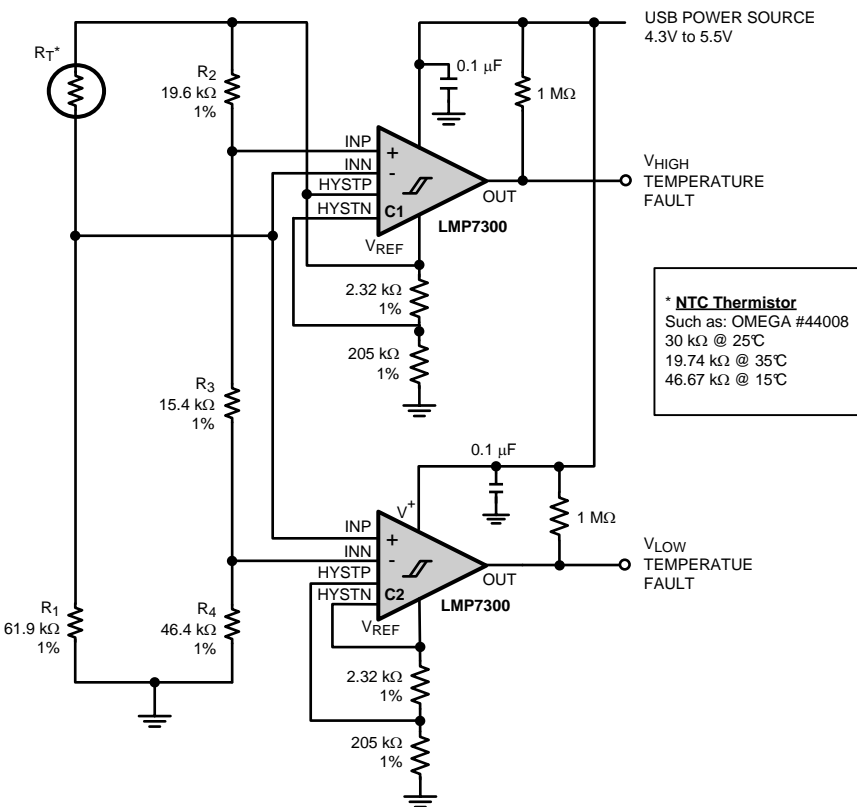


Figure 24. Temperature Controlled Window Detector to Monitor Ambient Temperature

PRECISION HIGH TEMPERATURE SWITCH

The LMP7300 brings accuracy and stability to simple sensor switch applications. Figure 26 shows the LMP7300 setup in a high temperature switch configuration. The input bridge establishes the trip point at 85°C and the reset temperature at 80°C. The comparator is set up with positive hysteresis of 14.3 mV and no negative hysteresis. When the temperature is rising it trips at 85°C. The 14.3 mV hysteresis allows the temperature to drop to 80°C before reset.

The temperature sensor used is an Omega 44008 Precision NTC Thermistor. The 44008 has an accuracy of $\pm 0.2^{\circ}\text{C}$. The resistance at 85°C is 3270.9Ω and at 80°C is 3840.2Ω . The trip voltage threshold is established by one half of the bridge, which is the ratio of R_{ADJ} and R_{SET} . The input signal bias is set by the second half, which is the ratio of the thermistor resistance R_{TH} and R_{SET} . The resistance values are chosen for $\sim 50\ \mu\text{A}$ bridge current to minimize the power in the thermistor. The thermistor specification states it has a $1^{\circ}\text{C}/\text{mW}$ dissipation error. The reference voltage establishes the supply voltage for the bridge to make the circuit independent of supply voltage variation. Capacitor C_1 establishes a low frequency pole at $F_{\text{CORNER}} = 1/(2\pi C_1 * 2(R_{\text{SET}}//R_{\text{ADJ}}))$. With the resistance values chosen C_1 should be selected for $F_c < 10\ \text{Hz}$. This will limit the thermal noise in the bridge.

The accuracy of the circuit can be calculated from the nearest resistance values chosen. For 1% resistors R_{ADJ} is $3.24\ \text{k}\Omega$, and R_{SET} is $78.7\ \text{k}\Omega$. The bridge gain becomes $2.488\ \text{mV}/^{\circ}\text{C}$ at 85°C . In general, the higher the bridge current is allowed to be, the higher the bridge gain will be. The actual trip point found during simulation is 85.3°C and the reset point is 80.04°C . With the values chosen the worst case trip temperature uncertainty is $\pm 1.451^{\circ}\text{C}$ and the reset uncertainty is $\pm 1.548^{\circ}\text{C}$. Accuracy could be maximized with resistors chosen to 0.1% values, 0.1% tolerance and by using the 0.1% model of the Omega 44008 thermistor.

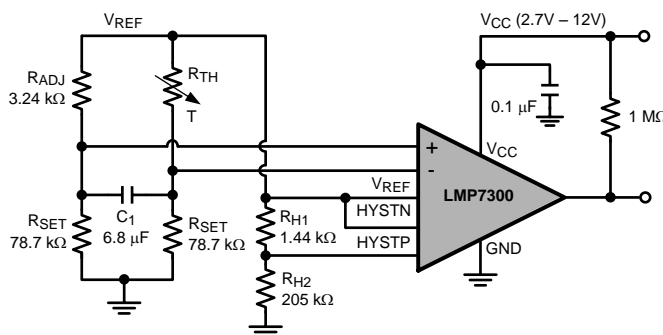


Figure 25. Precision High Temperature Switch

MICROPOWER PRECISION BATTERY LOW VOLTAGE DETECTOR

The ability of the LMP7300 to operate at very low supply voltages, makes it an ideal choice for low battery detection application in portable equipment. The circuit in Figure 26 performs the function of low voltage threshold detection in a 3 cell 0.9V discharge voltage, battery monitor application. R_1 and R_2 are chosen to set the inverting input voltage equal to the non-inverting input voltage when the battery voltage is equal to the minimum operating voltage of the system. Here, the very precise reference output voltage is directly connected to the non-inverting input on the comparator and sets an accurate threshold voltage. The hysteresis is set to 0 mV negative and 20 mV positive. The output is off for voltages higher than the minimum V_{BATT} , and turns on when the circuit detects a minimum battery voltage condition.

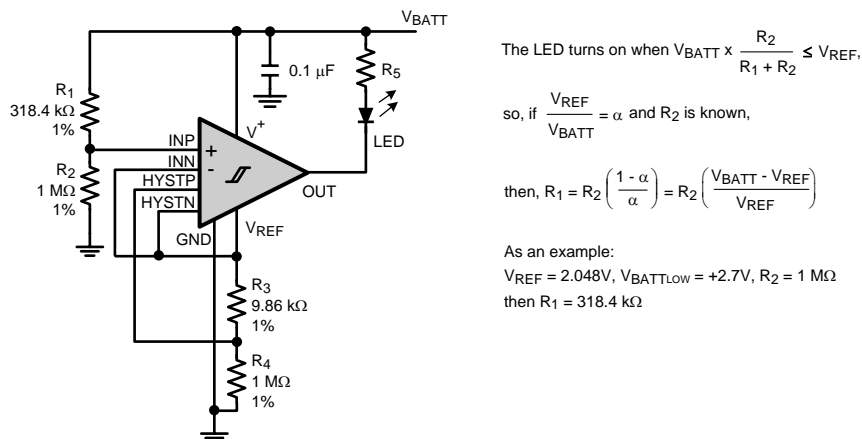


Figure 26. Battery Voltage Monitor for 3 Cell Discharge Voltage

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) | Op Temp (°C) | Top-Side Markings (4) | Samples |
|------------------|---------------|--------------|--------------------|------|-------------|----------------------------|------------------|----------------------|--------------|--------------------------|-------------------------|
| LMP7300MA/NOPB | ACTIVE | SOIC | D | 8 | 95 | Green (RoHS & no Sb/Br) | CU SN | Level-1-260C-UNLIM | -40 to 125 | LMP73 00MA | Samples |
| LMP7300MAX/NOPB | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU SN | Level-1-260C-UNLIM | -40 to 125 | LMP73 00MA | Samples |
| LMP7300MM/NOPB | ACTIVE | VSSOP | DGK | 8 | 1000 | Green (RoHS & no Sb/Br) | CU SN | Level-1-260C-UNLIM | -40 to 125 | C31A | Samples |
| LMP7300MME/NOPB | ACTIVE | VSSOP | DGK | 8 | 250 | Green (RoHS & no Sb/Br) | CU SN | Level-1-260C-UNLIM | -40 to 125 | C31A | Samples |
| LMP7300MMX/NOPB | ACTIVE | VSSOP | DGK | 8 | 3500 | Green (RoHS & no Sb/Br) | CU SN | Level-1-260C-UNLIM | -40 to 125 | C31A | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Only one of markings shown within the brackets will appear on the physical device.

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DGK (S-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
 - E. Falls within JEDEC MO-187 variation AA, except interlead flash.

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- $\triangle C$ Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- $\triangle D$ Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AA.

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