LMV761/LMV762/LMV762Q Low Voltage, Precision Comparator with Push-Pull Output

Check for Samples: LMV761, LMV762

FEATURES

- **(V_S = 5V, T_A = 25°C, typical values unless specified).**
- **Input Offset Boltage 0.2mV**
- **Input Offset Boltage (Max Over Temp) 1mV**
- **Input Bias Current 0.2pA**
- **Propagation Delay (OD = 50mV) 120 nsec**
- **Low Supply Current 300µA**
- **CMRR 100dB**
- **PSRR 110dB**
- **Extended Temperature Range −40°C to 125°C**
- **Push-Pull Output**
- **Ideal for 2.7V and 5V Single Supply Applications**
- **Available in Space-Saving Packages:**
  - **6-Pin SOT-23 (Single w/Shutdown)**
  - **8-Pin SOIC (single w/Shutdown)**
  - **8-Pin SOIC/VSSOP (Dual without Shutdown)**
- **LMV762Q is an Automotive Grade Product that is AEC-Q100 Grade 1 Qualified and is Manufactured on an Automotive Grade Flow**

APPLICATIONS

- **Portable and Battery-Powered Systems**
- **Scanners**
- **Set Top Boxes**
- **High Speed Differential Line Receiver**
- **Window Comparators**
- **Zero-Crossing Detectors**
- **High Speed Sampling Circuits**
- **Automotive**

DESCRIPTION

The LMV761/LMV762/LMV762Q are precision comparators intended for applications requiring low noise and low input offset voltage. The LMV761 single has a shutdown pin that can be used to disable the device and reduce the supply current. The LMV761 is available in a space saving 6-Pin SOT-23 or 8-Pin SOIC package. The LMV762 dual is available in 8-Pin SOIC or VSSOP package and LMV762Q in VSSOP and SOIC package.

They feature a CMOS input and Push-Pull output stage. The Push-Pull output stage eliminates the need for an external pull-up resistor.

The LMV761/LMV762/LMV762Q are designed to meet the demands of small size, low power and high performance required by portable and battery operated electronics.

The input offset voltage has a typical value of 200µV at room temp and a 1mV limit over temp.

Typical Circuit

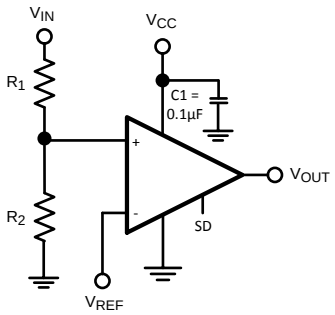


Figure 1. Threshold Detector

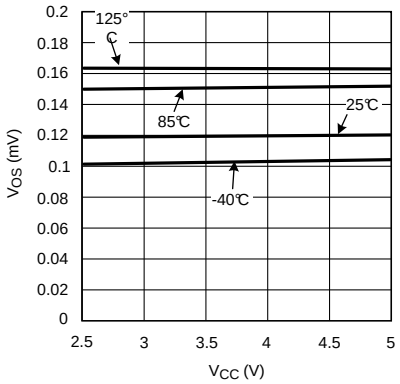


Figure 2. V_{OS} vs. V_{CC}

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings(1)(2)

ESD Tolerance(3)	Human Body Model	2000V
	Machine Model	200V
Supply Voltage ($V^+ - V^-$)		5.5V
Differential Input Voltage		Supply Voltage
Voltage between any two pins		Supply Voltage
Output Short Circuit Duration(4)	Current at Input Pin	±5 mA
Soldering Information	Infrared or Convection (20 sec.)	235°C
	Wave Soldering (10 sec.)	260°C (Lead Temp)
Junction Temperature		150°C
Storage Temperature Range		−65°C to 150°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test condition, see the Electrical Characteristics.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(3) Unless otherwise specified human body model is 1.5kΩ in series with 100pF. Machine model 200pF.
(4) Applies to both single supply and split supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C. Output current in excess of ±25 mA over long term may adversely affect reliability.

Operating Ratings

Supply Voltage ($V^+ - V^-$)		2.7V to 5.25V
Temperature Range		−40°C to +125°C
Package Thermal Resistance(1)	6-Pin SOT-23	265°C/W
	8-Pin SOIC	190°C/W
	8-Pin VSSOP	235°C/W

(1) The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)}-T_A)\theta_{JA}$. All numbers apply for packages soldered directly into a PC board.

2.7V Electrical Characteristics

Unless otherwise specified, all limited guaranteed for T_J = 25°C, V_{CM} = V^+/2, V^+ = 2.7V, V^- = 0V^-. **Boldface** limits apply at the temperature extremes. (1)

Symbol	Parameter	Condition	Min (2)	Typ (3)	Max (2)	Units
V_{OS}	Input Offset Voltage			0.2	**1.0**	mV
I_B	Input Bias Current (4)			0.2	50	pA
I_{OS}	Input Offset Current (4)			.001	5	pA
CMRR	Common Mode Rejection Ratio	0V < V_{CM} < V_{CC} - 1.3V	80	100		dB
PSRR	Power Supply Rejection Ratio	V^+ = 2.7V to 5V	80	110		dB
CMVR	Input Common Mode Voltage Range	CMRR > 50dB			**−0.3** **1.5**	V
V_O	Output Swing High	I_L = 2mA, V_{ID} = 200mV	V^+ – 0.35	V^+ – 0.1		V
	Output Swing Low	I_L = −2mA, V_{ID} = −200mV		90	250	mV
I_{SC}	Output Short Circuit Current (5)	Sourcing, V_O = 1.35V, V_{ID} = 200mV	6.0	20		mA
		Sinking, V_O = 1.35V, V_{ID} = −200mV	6.0	15		
I_S	Supply Current LMV761 (Single Comparator)			275	700	µA
	LMV762/LMV762Q (Both Comparators)			550	**1400**	µA
$I_{OUT\ LEAKAGE}$	Output Leakage I @ Shutdown	$\overline{SD}$ = GND, V_O = 2.7V		0.20		µA
$I_{S\ LEAKAGE}$	Supply Leakage I @ Shutdown	$\overline{SD}$ = GND, V_{CC} = 2.7V		0.20	2	µA
t_{PD}	Propagation Delay R_L = 5.1kΩ C_L = 50pF	Overdrive = 5mV		270		ns
		Overdrive = 10mV		205		
		Overdrive = 50mV		120		
t_{SKEW}	Propagation Delay Skew			5		ns
t_r	Output Rise Time	10% to 90%		1.7		ns
t_f	Output Fall Time	90% to 10%		1.8		ns
t_{on}	Turn On Time from Shutdown			6		µs

(1) Maximum temperature guarantee range is −40°C to 125°C.
(2) All limits are guaranteed by testing or statistical analysis.
(3) Typical values represent the most likely parametric norm.
(4) Guaranteed by design.
(5) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that T_J = T_A. No guarantee of parametric performance is indicated in the electrical tables under conditions of internal self-heating where T_J > T_A. See Application Information for information on temperature de-rating of this device. Absolute Maximum Rating indicate junction temperature limits beyond which the device may be permanently degraded, either mechanically or electrically.

5.0V Electrical Characteristics

Unless otherwise specified, all limited guaranteed for T_J = 25°C, V_{CM} = V^+/2, V^+ = 5.0V, V^- = 0V^-. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Condition	Min(1)	Typ(2)	Max(1)	Units
V_{OS}	Input Offset Voltage			0.2	**1.0**	mV
I_B	Input Bias Current(3)			0.2	50	pA
I_{OS}	Input Offset Current(3)			0.01	5	pA
CMRR	Common Mode Rejection Ratio	0V < V_{CM} < V_{CC} - 1.3V	80	100		dB
PSRR	Power Supply Rejection Ratio	V^+ = 2.7V to 5V	80	110		dB
CMVR	Input Common Mode Voltage Range	CMRR > 50dB			**−0.3** **3.8**	V
V_O	Output Swing High	I_L = 4mA, V_{ID} = 200mV	V^+ – 0.35	V^+ – 0.1		V
	Output Swing Low	I_L = −4mA, V_{ID} = −200mV		120	250	mV
I_{SC}	Output Short Circuit Current(4)	Sourcing, V_O = 2.5V, V_{ID} = 200mV	6.0	60		mA
		Sinking, V_O = 2.5V, V_{ID} = −200mV	6.0	40		
I_S	Supply Current LMV761 (Single Comparator)			225	700	µA
	LMV762/LMV762Q (Both Comparators)			450	**1400**	µA
I_{OUT} LEAKAGE	Output Leakage I @ Shutdown	$\overline{SD}$ = GND, V_O = 5.0V		0.20		µA
I_{S} LEAKAGE	Supply Leakage I @ Shutdown	$\overline{SD}$ = GND, V_{CC} = 5.0V		0.20	2	µA
t_{PD}	Propagation Delay R_L = 5.1kΩ C_L = 50pF	Overdrive = 5mV		225		ns
		Overdrive = 10mV		190		
		Overdrive = 50mV		120		
t_{SKEW}	Propagation Delay Skew			5		ns
t_r	Output Rise Time	10% to 90%		1.7		ns
t_f	Output Fall Time	90% to 10%		1.5		ns
t_{on}	Turn On Time from Shutdown			4		µs

(1) All limits are guaranteed by testing or statistical analysis.
(2) Typical values represent the most likely parametric norm.
(3) Guaranteed by design.
(4) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that T_J = T_A. No guarantee of parametric performance is indicated in the electrical tables under conditions of internal self-heating where T_J > T_A. See Application Information for information on temperature de-rating of this device. Absolute Maximum Rating indicate junction temperature limits beyond which the device may be permanently degraded, either mechanically or electrically.

Connection Diagrams

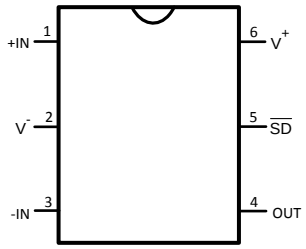


Figure 3. LMV761 (Single) 6-Pin SOT-23 Top View

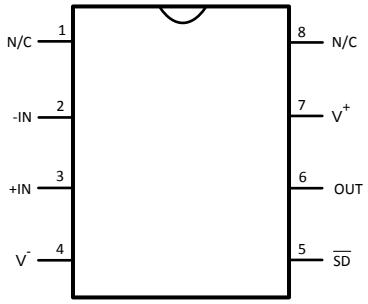


Figure 4. LMV761 (Single) 8-Pin SOIC Top View

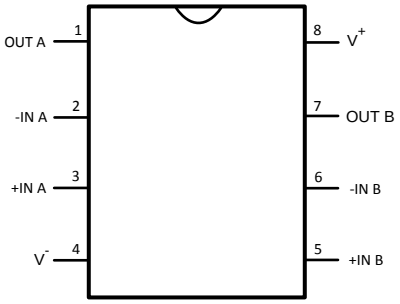


Figure 5. LMV762/LMV762Q (Dual) 8-Pin SOIC and VSSOP Top View

Typical Performance Characteristics

PSI vs. V_{CC} (V_O = High)

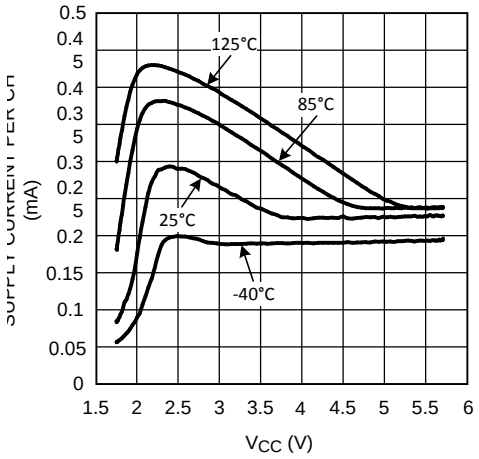


Figure 6.

PSI vs. V_{CC} (V_O = Low)

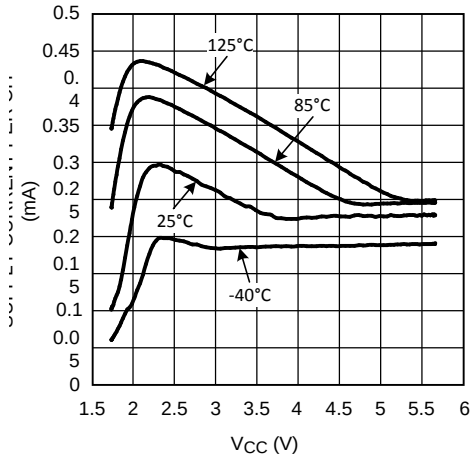


Figure 7.

V_{OS} vs. V_{CC}

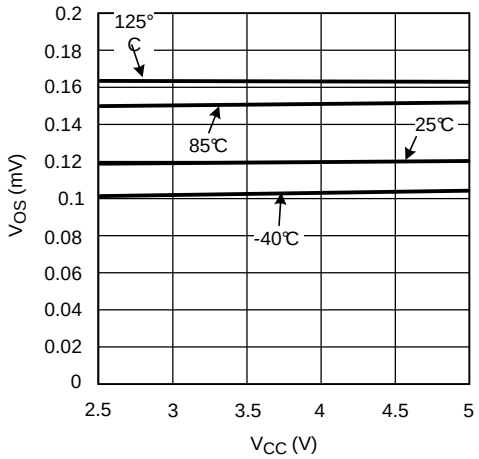


Figure 8.

Input Bias vs. Common Mode @ 25°C

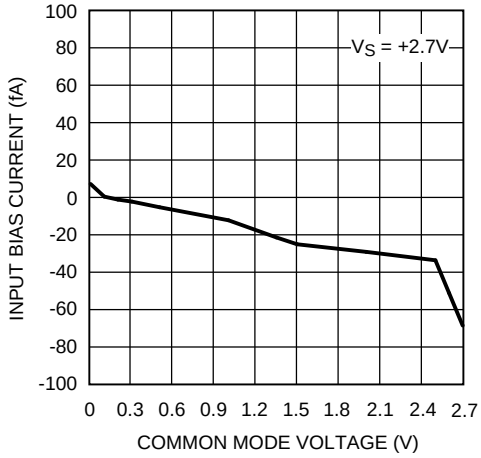


Figure 9.

Input Bias vs. Common Mode @ 25°C

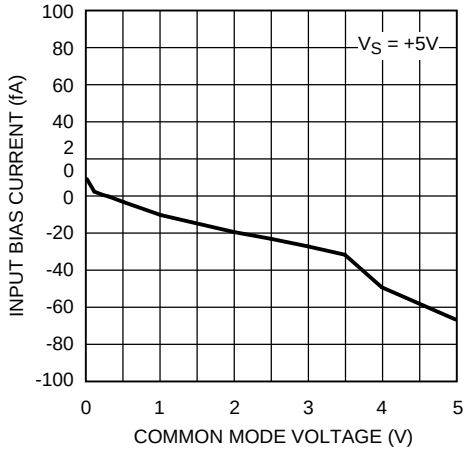


Figure 10.

Output Voltage vs. Supply Voltage

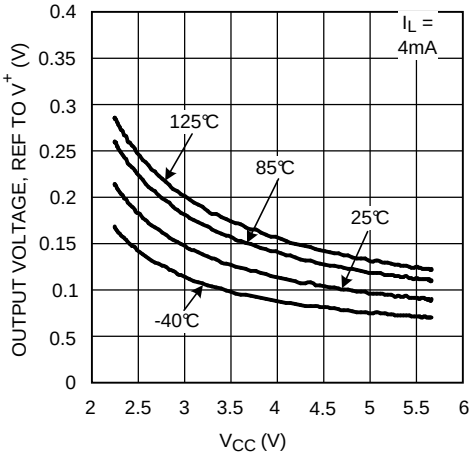


Figure 11.

Typical Performance Characteristics (continued)

Output Voltage vs. Supply Voltage

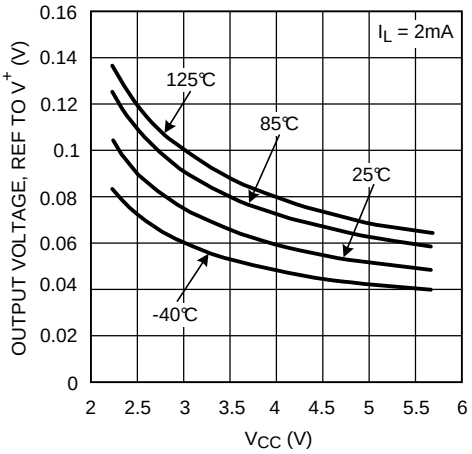


Figure 12.

Output Voltage vs. Supply Voltage

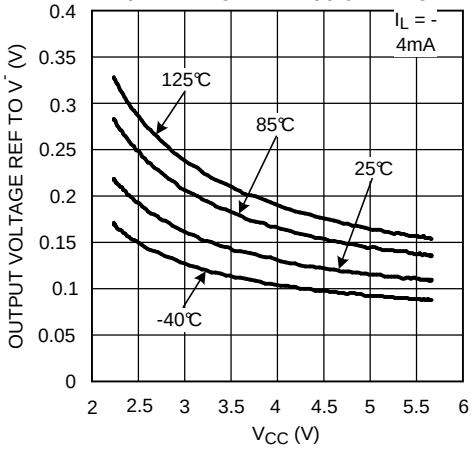


Figure 13.

Output Voltage vs. Supply Voltage

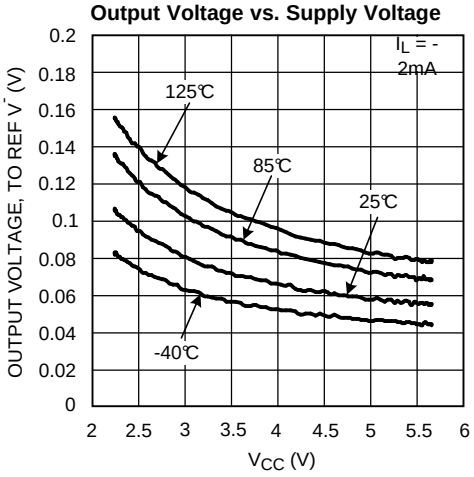


Figure 14.

I_{SOURCE} vs. V_{OUT}

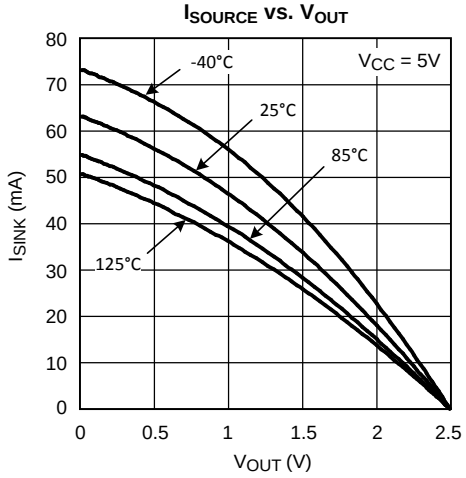


Figure 15.

I_{SINK} vs. V_{OUT}

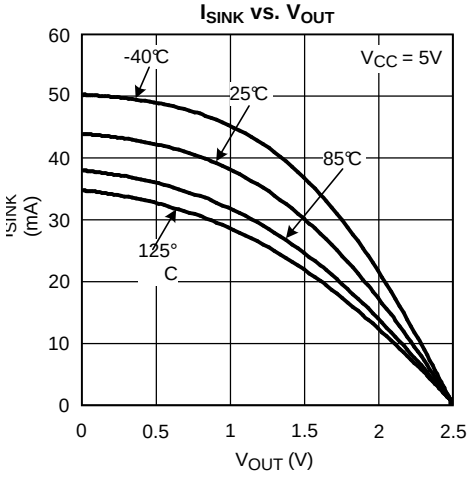


Figure 16.

I_{SOURCE} vs. V_{OUT}

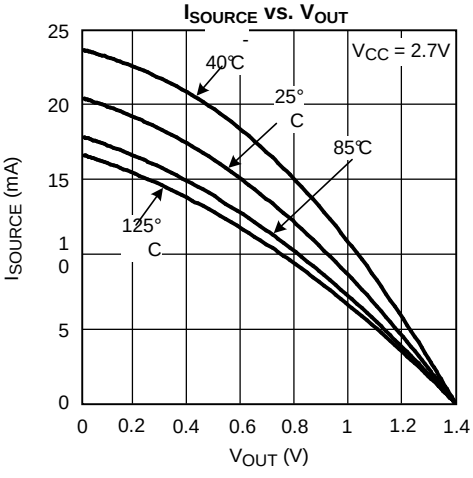


Figure 17.

Typical Performance Characteristics (continued)

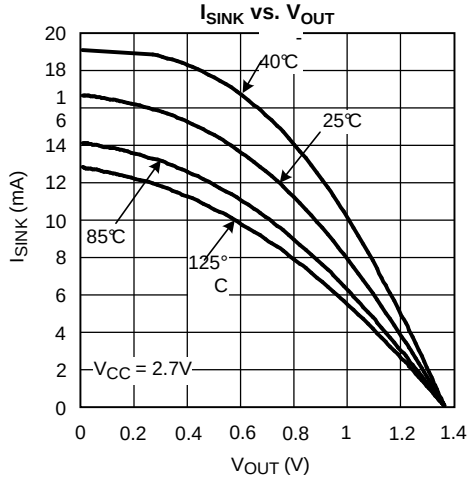


Figure 18.

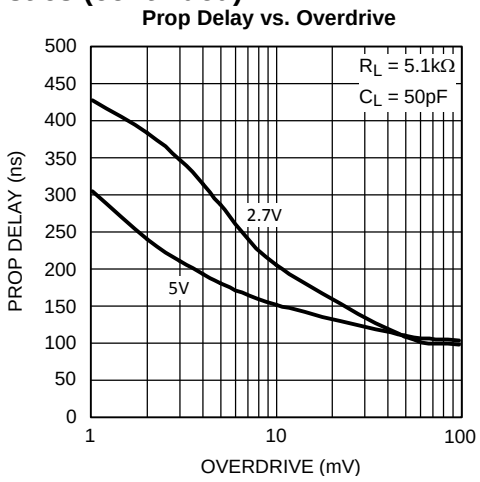


Figure 19.

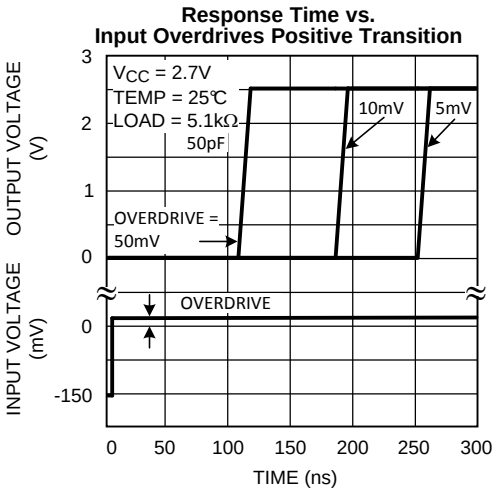


Figure 20.

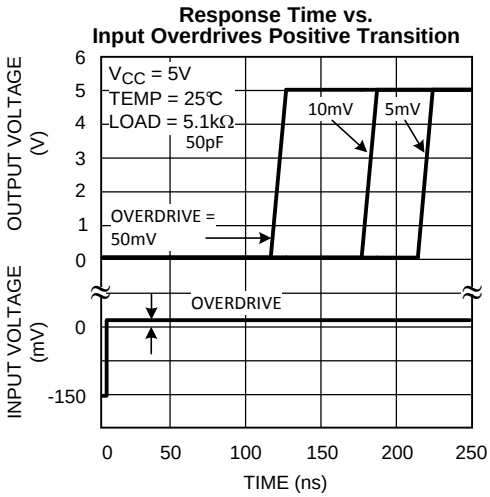


Figure 21.

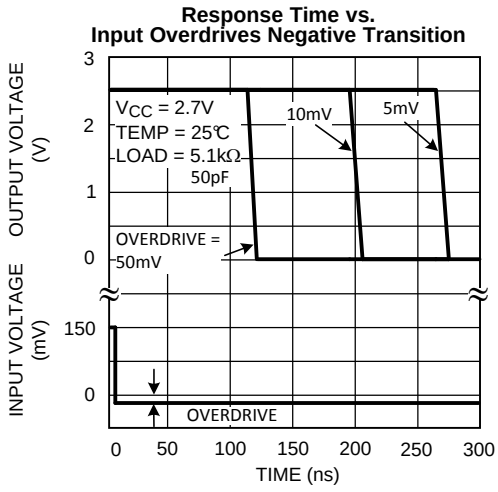


Figure 22.

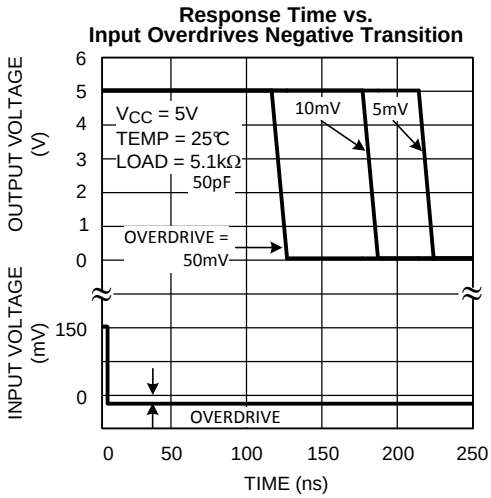


Figure 23.

APPLICATION INFORMATION

BASIC COMPARATOR

A basic comparator circuit is used to convert analog input signals to digital output signals. The comparator compares an input voltage (V_{IN}) at the non-inverting input to the reference voltage (V_{REF}) at the inverting pin. If V_{IN} is less than V_{REF} the output (V_O) is low (V_{OL}). However, if V_{IN} is greater than V_{REF}, the output voltage (V_O) is high (V_{OH}).

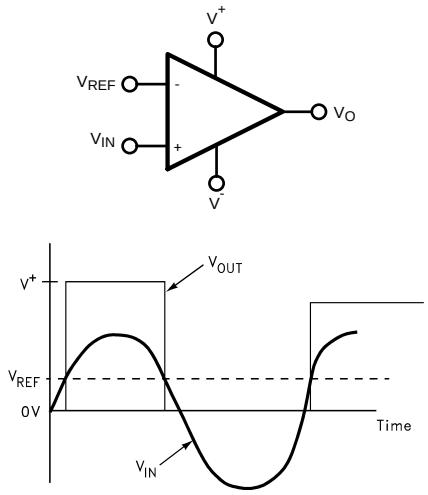


Figure 24. Basic Comparator

HYSTERESIS

The basic comparator configuration may oscillate or produce a noisy output if the applied differential input is near the comparator's input offset voltage. This tends to occur when the voltage on one input is equal or very close to the other input voltage. Adding hysteresis can prevent this problem. Hysteresis creates two switching thresholds (one for the rising input voltage and the other for the falling input voltage). Hysteresis is the voltage difference between the two switching thresholds. When both inputs are nearly equal, hysteresis causes one input to effectively move quickly past the other. Thus, moving the input out of the region in which oscillation may occur.

Hysteresis can easily be added to a comparator in a non-inverting configuration with two resistors and positive feedback Figure 25. The output will switch from low to high when V_{IN} rises up to V_{IN1}, where V_{IN1} is calculated by

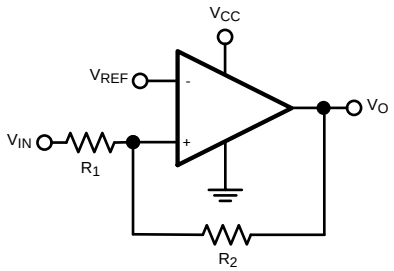
$$V_{IN1} = [V_{REF}(R_1+R_2)] / R_2 \quad (1)$$

The output will switch from high to low when V_{IN} falls to V_{IN2}, where V_{IN2} is calculated by

$$V_{IN2} = [V_{REF}(R_1+R_2) – (V_{CC} R_1)] / R_2 \quad (2)$$

The Hysteresis is the difference between V_{IN1} and V_{IN2}.

$$\Delta V_{IN} = V_{IN1} - V_{IN2} = [V_{REF}(R_1+R_2) / R_2] - [V_{REF}(R_1+R_2)] - [(V_{CC} R_1) / R_2] = V_{CC} R_1 / R_2 \quad (3)$$



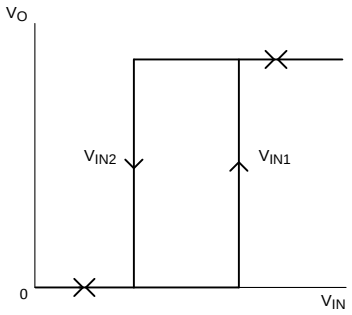


Figure 25. Non-Inverting Comparator Configuration

INPUT

The LMV761/LMV762 have near zero input bias current. This allows very high resistance circuits to be used without any concern for matching input resistances. This also allows the use of very small capacitors in R-C type timing circuits. This reduces the cost of the capacitors and amount of board space used.

SHUTDOWN MODE

The LMV761 features a low-power shutdown pin that is activated by driving $\overline{SD}$ low. In shutdown mode, the output is in a high impedance state, supply current is reduced to 20nA and the comparator is disabled. Driving $\overline{SD}$ high will turn the comparator on. The $\overline{SD}$ pin should not be left unconnected due to the fact that it is a high impedance input. When left unconnected, the output will be at an unknown voltage. Also do not three-state the $\overline{SD}$ pin.

The maximum input voltage for $\overline{SD}$ is 5.5V, referred to ground and is not limited by V_{CC}. This allows the use of 5V logic to drive $\overline{SD}$ while V_{CC} operates at a lower voltage, such as 3V. The logic threshold limits for $\overline{SD}$ are proportional to V_{CC}.

BOARD LAYOUT AND BYPASSING

The LMV761/LMV762 is designed to be stable and oscillation free, but it is still important to include the proper bypass capacitors and ground pickups. Ceramic 0.1µF capacitors should be placed at both supplies to provide clean switching. Minimize the length of signal traces to reduce stray capacitance.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
LMV761MA	ACTIVE	SOIC	D	8	95	TBD	CU SNPB	Level-1-235C-UNLIM	-40 to 125	LMV76 1MA	Samples
LMV761MA/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LMV76 1MA	Samples
LMV761MAX	ACTIVE	SOIC	D	8	2500	TBD	CU SNPB	Level-1-235C-UNLIM	-40 to 125	LMV76 1MA	Samples
LMV761MAX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LMV76 1MA	Samples
LMV761MF	ACTIVE	SOT-23	DBV	6	1000	TBD	CU SNPB	Level-1-260C-UNLIM	-40 to 125	C22A	Samples
LMV761MF/NOPB	ACTIVE	SOT-23	DBV	6	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	C22A	Samples
LMV761MFX	ACTIVE	SOT-23	DBV	6	3000	TBD	CU SNPB	Level-1-260C-UNLIM	-40 to 125	C22A	Samples
LMV761MFX/NOPB	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	C22A	Samples
LMV762MA	ACTIVE	SOIC	D	8	95	TBD	CU SNPB	Level-1-235C-UNLIM	-40 to 125	LMV7 62MA	Samples
LMV762MA/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LMV7 62MA	Samples
LMV762MAX	ACTIVE	SOIC	D	8	2500	TBD	CU SNPB	Level-1-235C-UNLIM	-40 to 125	LMV7 62MA	Samples
LMV762MAX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LMV7 62MA	Samples
LMV762MM	ACTIVE	VSSOP	DGK	8	1000	TBD	CU SNPB	Level-1-260C-UNLIM	-40 to 125	C23A	Samples
LMV762MM/NOPB	ACTIVE	VSSOP	DGK	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	C23A	Samples
LMV762MMX	ACTIVE	VSSOP	DGK	8	3500	TBD	CU SNPB	Level-1-260C-UNLIM	-40 to 125	C23A	Samples
LMV762MMX/NOPB	ACTIVE	VSSOP	DGK	8	3500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	C23A	Samples
LMV762QMA/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LMV76 2QMA	Samples
LMV762QMAX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LMV76 2QMA	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
LMV762QMM/NOPB	ACTIVE	VSSOP	DGK	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	C32A	Samples
LMV762QMMX/NOPB	ACTIVE	VSSOP	DGK	8	3500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	C32A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

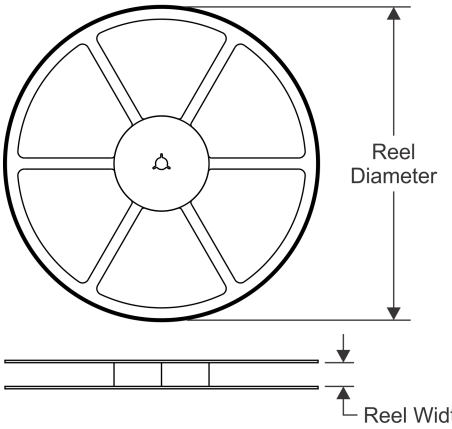
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

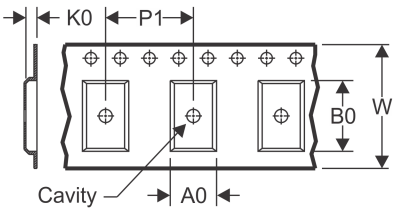
(4) Only one of markings shown within the brackets will appear on the physical device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

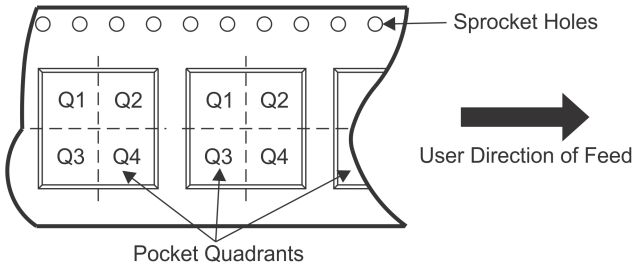


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

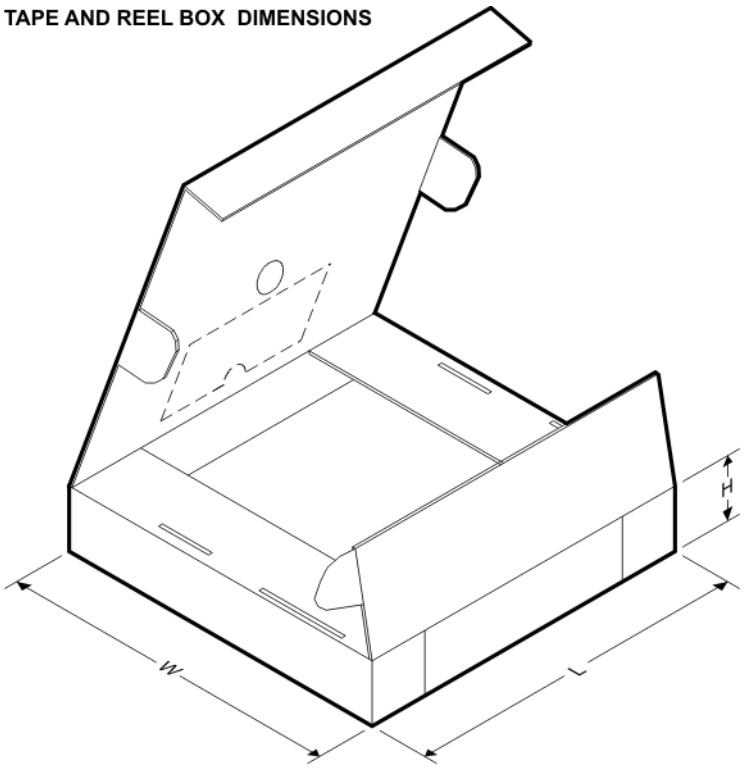
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMV761MAX	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LMV761MAX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LMV761MF	SOT-23	DBV	6	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV761MF/NOPB	SOT-23	DBV	6	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV761MFX	SOT-23	DBV	6	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV761MFX/NOPB	SOT-23	DBV	6	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV762MAX	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LMV762MAX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LMV762MM	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMV762MM/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMV762MMX	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMV762MMX/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMV762QMAX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LMV762QMM/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMV762QMMX/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

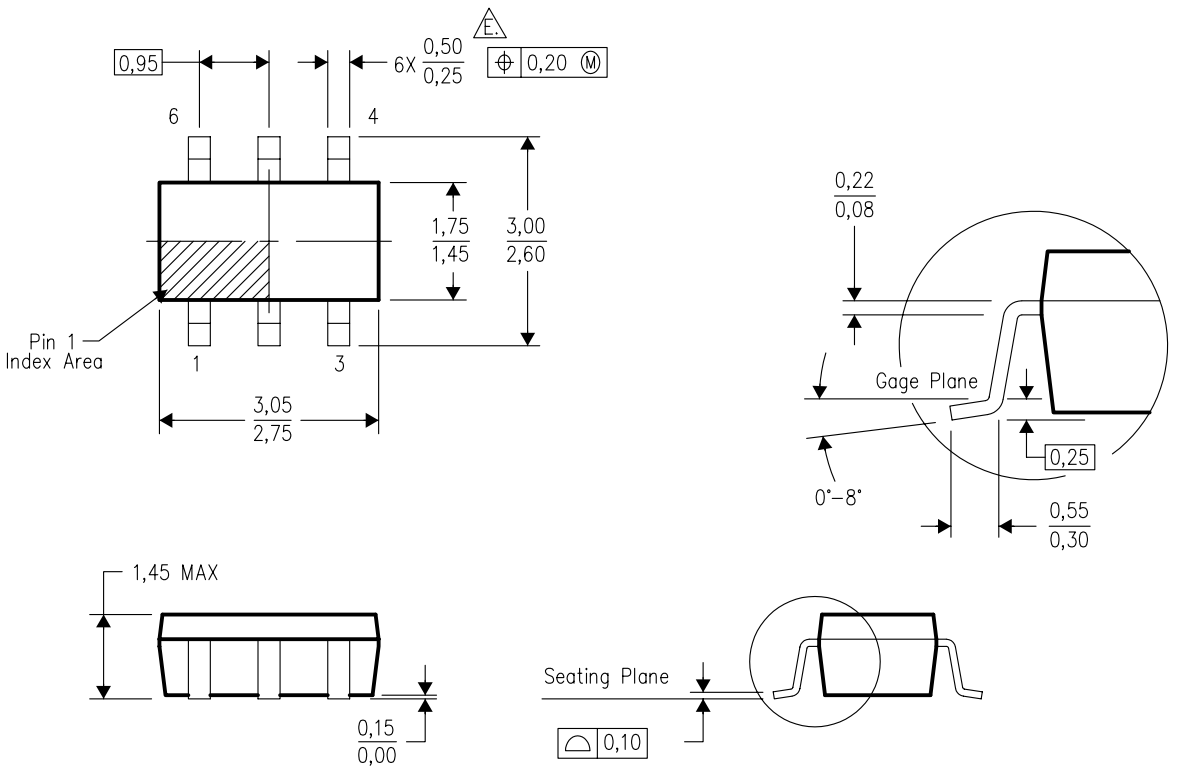
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMV761MAX	SOIC	D	8	2500	349.0	337.0	45.0
LMV761MAX/NOPB	SOIC	D	8	2500	349.0	337.0	45.0
LMV761MF	SOT-23	DBV	6	1000	203.0	190.0	41.0
LMV761MF/NOPB	SOT-23	DBV	6	1000	203.0	190.0	41.0
LMV761MFX	SOT-23	DBV	6	3000	206.0	191.0	90.0
LMV761MFX/NOPB	SOT-23	DBV	6	3000	206.0	191.0	90.0
LMV762MAX	SOIC	D	8	2500	349.0	337.0	45.0
LMV762MAX/NOPB	SOIC	D	8	2500	349.0	337.0	45.0
LMV762MM	VSSOP	DGK	8	1000	203.0	190.0	41.0
LMV762MM/NOPB	VSSOP	DGK	8	1000	203.0	190.0	41.0
LMV762MMX	VSSOP	DGK	8	3500	349.0	337.0	45.0
LMV762MMX/NOPB	VSSOP	DGK	8	3500	349.0	337.0	45.0
LMV762QMAX/NOPB	SOIC	D	8	2500	349.0	337.0	45.0
LMV762QMM/NOPB	VSSOP	DGK	8	1000	203.0	190.0	41.0
LMV762QMMX/NOPB	VSSOP	DGK	8	3500	349.0	337.0	45.0

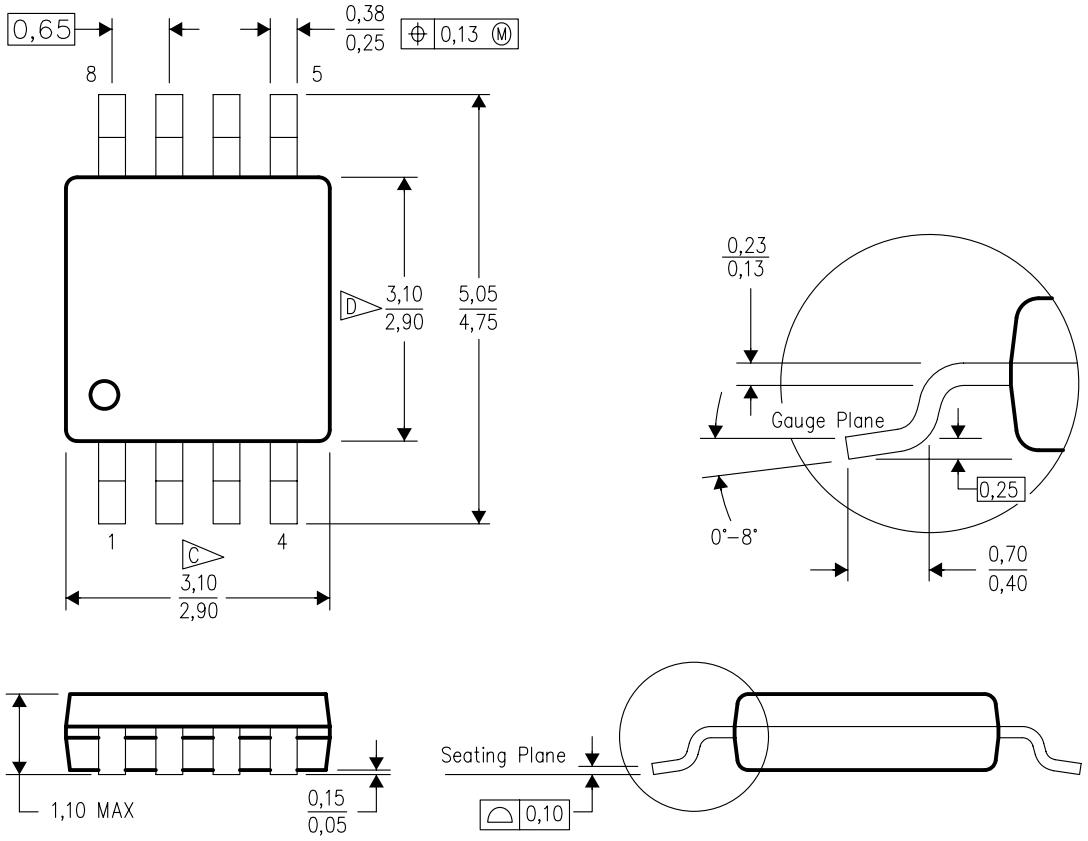
DBV (R–PDSO–G6) PLASTIC SMALL–OUTLINE PACKAGE



4073253–5/K 03/2006

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
E. Falls within JEDEC MO–178 Variation AB, except minimum lead width.

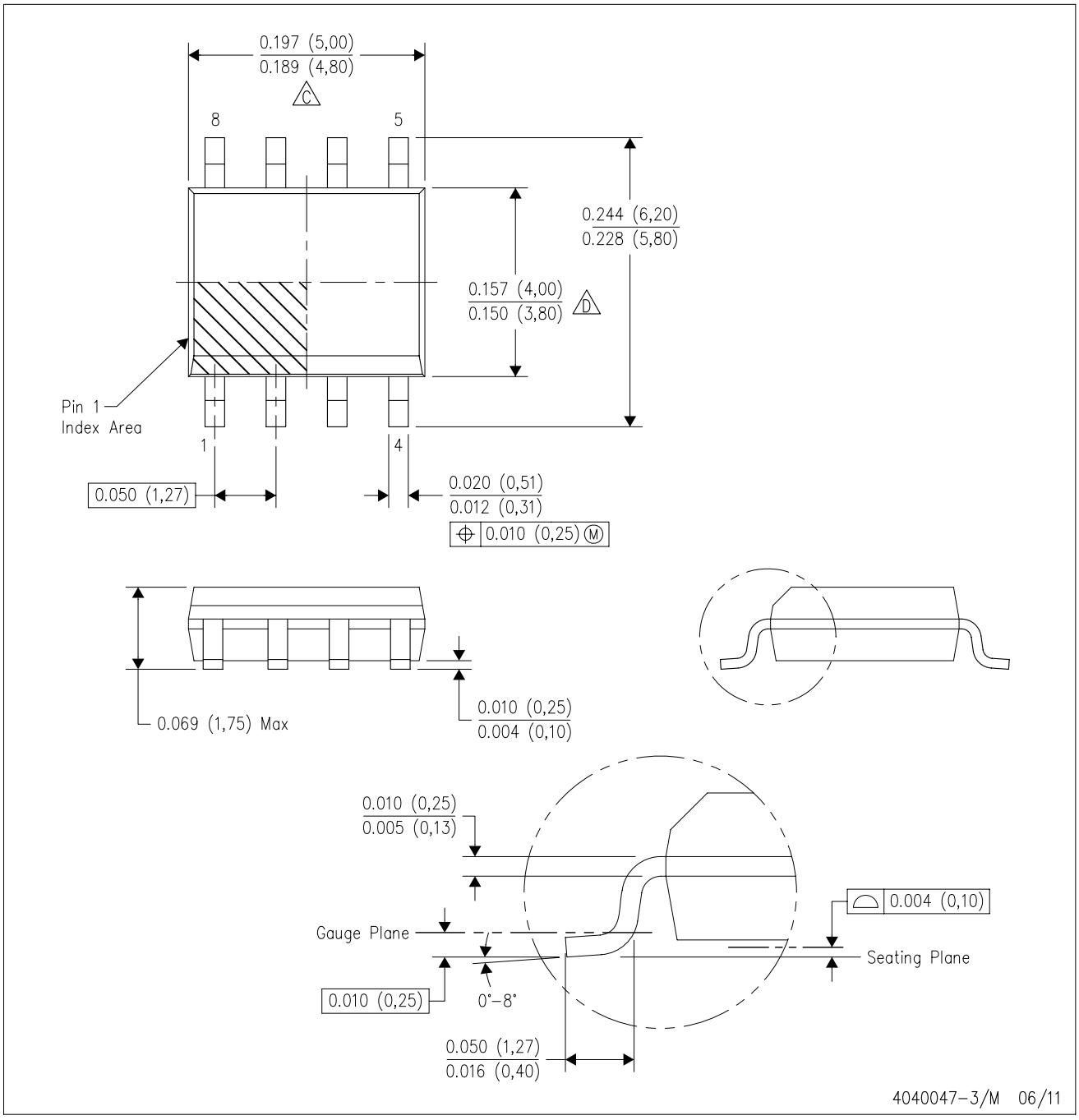
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

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