

# LMV796/LMV796Q/LMV797 17 MHz, Low Noise, CMOS Input, 1.8V Operational Amplifiers

Check for Samples: [LMV796](#), [LMV797](#)

## FEATURES

- (Typical 5V supply, unless otherwise noted)
- Input referred voltage noise  $5.8 \text{ nV}/\sqrt{\text{Hz}}$
- Input bias current 100 fA
- Unity gain bandwidth 17 MHz
- Supply current per channel
  - LMV796/LMV796Q 1.15 mA
  - LMV797 1.30 mA
- Rail-to-rail output swing
  - @ 10 k $\Omega$  load 25 mV from rail
  - @ 2 k $\Omega$  load 45 mV from rail
- Guaranteed 2.5V and 5.0V performance
- Total harmonic distortion 0.01% @ 1kHz, 600 $\Omega$

- Temperature range  $-40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$
- LMV796Q is an Automotive grade product that is AEC-Q100 grade 1 qualified and is manufactured on an automotive grade flow.

## APPLICATIONS

- Photodiode amplifiers
- Active filters and buffers
- Low noise signal processing
- Medical instrumentation
- Sensor interface applications
- Automotive

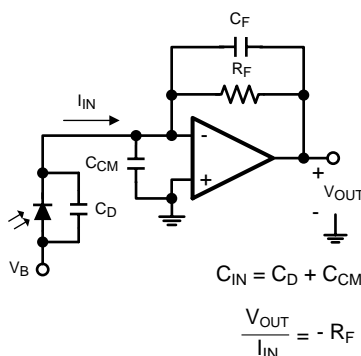
## DESCRIPTION

The LMV796/LMV796Q (Single) and the LMV797 (Dual) low noise, CMOS input operational amplifiers offer a low input voltage noise density of  $5.8 \text{ nV}/\sqrt{\text{Hz}}$  while consuming only 1.15 mA (LMV796/LMV796Q) of quiescent current. The LMV796/LMV796Q and LMV797 are unity gain stable op amps and have gain bandwidth of 17 MHz. The LMV796/LMV796Q/LMV797 have a supply voltage range of 1.8V to 5.5V and can operate from a single supply. The LMV796/LMV796Q/LMV797 each feature a rail-to-rail output stage capable of driving a 600 $\Omega$  load and sourcing as much as 60 mA of current.

The LMV796/LMV796Q family provides optimal performance in low voltage and low noise systems. A CMOS input stage, with typical input bias currents in the range of a few femtoAmperes, and an input common mode voltage range, which includes ground, make the LMV796/LMV796Q and the LMV797 ideal for low power sensor applications.

The LMV796/LMV796Q/LMV797 are manufactured using National's advanced VIP50 process. The LMV796/LMV796Q are offered in 5-pin SOT23 package. The LMV797 is offered in 8-pin MSOP package.

## Typical Application



**Figure 1. Photodiode Transimpedance Amplifier**



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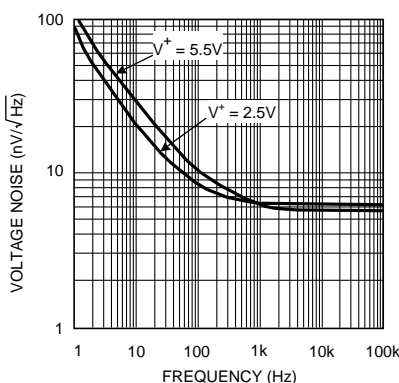


Figure 2. Input Referred Voltage Noise vs. Frequency



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### Absolute Maximum Ratings <sup>(1)</sup>

ESD Tolerance <sup>(2)</sup>	
Human Body Model	2000V
Machine Model	200V
Charge-Device Model	1000V
V <sub>IN</sub> Differential	±0.3V
Supply Voltage (V <sup>+</sup> – V <sup>-</sup> )	6.0V
Input/Output Pin Voltage	V <sup>+</sup> +0.3V, V <sup>-</sup> -0.3V
Storage Temperature Range	-65°C to 150°C
Junction Temperature <sup>(3)</sup>	+150°C
Soldering Information	
Infrared or Convection (20 sec)	235°C
Wave Soldering Lead Temp (10 sec)	260°C

- (1) *Absolute Maximum Ratings* indicate limits beyond which damage to the device may occur. *Operating Ratings* indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the *Electrical Characteristics* tables.
- (2) Human Body Model is 1.5kΩ in series with 100pF. Machine Model is 0Ω in series with 200pF.
- (3) The maximum power dissipation is a function of T<sub>JMAX</sub>, θ<sub>JA</sub>. The maximum allowable power dissipation at any ambient temperature is P<sub>D</sub> = (T<sub>JMAX</sub> - T<sub>A</sub>) / θ<sub>JA</sub>. All numbers apply for packages soldered directly onto a PC Board.

### Operating Ratings <sup>(1)</sup>

Temperature Range <sup>(2)</sup>	-40°C to 125°C
Supply Voltage (V <sup>+</sup> – V <sup>-</sup> )	
-40°C ≤ T <sub>A</sub> ≤ 125°C	2.0V to 5.5V
0°C ≤ T <sub>A</sub> ≤ 125°C	1.8V to 5.5V
Package Thermal Resistance (θ <sub>JA</sub> ) <sup>(2)</sup>	
5-Pin SOT-23	180°C/W
8-Pin MSOP	236°C/W

- (1) *Absolute Maximum Ratings* indicate limits beyond which damage to the device may occur. *Operating Ratings* indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the *Electrical Characteristics* tables.
- (2) The maximum power dissipation is a function of T<sub>JMAX</sub>, θ<sub>JA</sub>. The maximum allowable power dissipation at any ambient temperature is P<sub>D</sub> = (T<sub>JMAX</sub> - T<sub>A</sub>) / θ<sub>JA</sub>. All numbers apply for packages soldered directly onto a PC Board.

## 2.5V Electrical Characteristics

Unless otherwise specified, all limits are guaranteed for  $T_A = 25^\circ\text{C}$ ,  $V^+ = 2.5\text{V}$ ,  $V^- = 0\text{V}$ ,  $V_{CM} = V^+/2 = V_O$ . **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (1)	Typ (2)	Max (1)	Units
$V_{OS}$	Input Offset Voltage			0.1	$\pm 1.35$ <b><math>\pm 1.65</math></b>	mV
TC $V_{OS}$	Input Offset Voltage Temperature Drift	LMV796/LMV796Q <sup>(3)</sup>		-1.0		$\mu\text{V}/^\circ\text{C}$
		LMV797 <sup>(3)</sup>		-1.8		
$I_B$	Input Bias Current	$V_{CM} = 1.0\text{V}$ <sup>(4)</sup> <sup>(5)</sup>		0.05	1 <b>25</b>	pA
		$-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$		0.05	1 <b>100</b>	
$I_{OS}$	Input Offset Current	$V_{CM} = 1.0\text{V}$ <sup>(5)</sup>		10		fA
CMRR	Common Mode Rejection Ratio	$0\text{V} \leq V_{CM} \leq 1.4\text{V}$	80 <b>75</b>	94		dB
PSRR	Power Supply Rejection Ratio	$2.0\text{V} \leq V^+ \leq 5.5\text{V}$ , $V_{CM} = 0\text{V}$	80 <b>75</b>	100		dB
		$1.8\text{V} \leq V^+ \leq 5.5\text{V}$ , $V_{CM} = 0\text{V}$	80	98		
CMVR	Common Mode Voltage Range	CMRR $\geq 60\text{ dB}$ CMRR $\geq 55\text{ dB}$	-0.3 <b>-0.3</b>		1.5 <b>1.5</b>	V
$A_{VOL}$	Open Loop Voltage Gain	$V_{OUT} = 0.15\text{V to } 2.2\text{V}$ , $R_{LOAD} = 2\text{ k}\Omega \text{ to } V^+/2$	LMV796/LMV796Q 85 <b>80</b>	98		dB
			LMV797 82 <b>78</b>	92		
		$V_{OUT} = 0.15\text{V to } 2.2\text{V}$ , $R_{LOAD} = 10\text{ k}\Omega \text{ to } V^+/2$	88 <b>84</b>	110		
$V_{OUT}$	Output Voltage Swing High	$R_{LOAD} = 2\text{ k}\Omega \text{ to } V^+/2$		25	75 <b>82</b>	mV from either rail
		$R_{LOAD} = 10\text{ k}\Omega \text{ to } V^+/2$		20	65 <b>71</b>	
	Output Voltage Swing Low	$R_{LOAD} = 2\text{ k}\Omega \text{ to } V^+/2$		30	75 <b>78</b>	
		$R_{LOAD} = 10\text{ k}\Omega \text{ to } V^+/2$		15	65 <b>67</b>	
$I_{OUT}$	Output Current	Sourcing to $V^-$ $V_{IN} = 200\text{ mV}$ <sup>(6)</sup>	35 <b>28</b>	47		mA
		Sinking to $V^+$ $V_{IN} = -200\text{ mV}$ <sup>(6)</sup>	7 <b>5</b>	15		
$I_S$	Supply Current per Amplifier	LMV796/LMV796Q		0.95	1.30 <b>1.65</b>	mA
		LMV797 per channel		1.1	1.50 <b>1.85</b>	
SR	Slew Rate	$A_V = +1$ , Rising (10% to 90%)		8.5		V/ $\mu\text{s}$
		$A_V = +1$ , Falling (90% to 10%)		10.5		
GBW	Gain Bandwidth			14		MHz
$e_n$	Input Referred Voltage Noise Density	$f = 1\text{ kHz}$		6.2		$\text{nV}/\sqrt{\text{Hz}}$
$i_n$	Input Referred Current Noise Density	$f = 1\text{ kHz}$		0.01		$\text{pA}/\sqrt{\text{Hz}}$
THD+N	Total Harmonic Distortion + Noise	$f = 1\text{ kHz}$ , $A_V = 1$ , $R_{LOAD} = 600\Omega$		0.01		%

- (1) Limits are 100% production tested at  $25^\circ\text{C}$ . Limits over the operating temperature range are guaranteed through correlations using the statistical quality control (SQC) method.
- (2) Typical values represent the parametric norm at the time of characterization.
- (3) Offset voltage average drift is determined by dividing the change in  $V_{OS}$  by temperature change.
- (4) Positive current corresponds to current flowing into the device.
- (5) This parameter is guaranteed by design and/or characterization and is not tested in production.
- (6) The short circuit test is a momentary test, the short circuit duration is 1.5ms.

## 5V Electrical Characteristics

Unless otherwise specified, all limits are guaranteed for  $T_A = 25^\circ\text{C}$ ,  $V^+ = 5\text{V}$ ,  $V^- = 0\text{V}$ ,  $V_{\text{CM}} = V^+/2 = V_O$ . **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (1)	Typ (2)	Max (1)	Units
$V_{\text{OS}}$	Input Offset Voltage			0.1	$\pm 1.35$ <b><math>\pm 1.65</math></b>	mV
TC $V_{\text{OS}}$	Input Offset Voltage Temperature Drift	LMV796/LMV796Q <sup>(3)</sup>		-1.0		$\mu\text{V}/^\circ\text{C}$
		LMV797 <sup>(3)</sup>		-1.8		
$I_B$	Input Bias Current	$V_{\text{CM}} = 2.0\text{V}$ (4) (5)		0.1	1 <b>25</b>	pA
		$-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$		0.1	1 <b>100</b>	
$I_{\text{OS}}$	Input Offset Current	$V_{\text{CM}} = 2.0\text{V}$ (5)		10		fA
CMRR	Common Mode Rejection Ratio	$0\text{V} \leq V_{\text{CM}} \leq 3.7\text{V}$	80 <b>75</b>	100		dB
PSRR	Power Supply Rejection Ratio	$2.0\text{V} \leq V^+ \leq 5.5\text{V}$ , $V_{\text{CM}} = 0\text{V}$	80 <b>75</b>	100		dB
		$1.8\text{V} \leq V^+ \leq 5.5\text{V}$ , $V_{\text{CM}} = 0\text{V}$	80	98		
CMVR	Common Mode Voltage Range	CMRR $\geq 60\text{ dB}$ CMRR $\geq 55\text{ dB}$	-0.3 <b>-0.3</b>		4 <b>4</b>	V
$A_{\text{VOL}}$	Open Loop Voltage Gain	$V_{\text{OUT}} = 0.3\text{V to } 4.7\text{V}$ , $R_{\text{LOAD}} = 2\text{ k}\Omega \text{ to } V^+/2$	LMV796/LMV796Q 85 <b>80</b>	97		dB
			LMV797 82 <b>78</b>	89		
		$V_{\text{OUT}} = 0.3\text{V to } 4.7\text{V}$ , $R_{\text{LOAD}} = 10\text{ k}\Omega \text{ to } V^+/2$	88 <b>84</b>	110		
$V_{\text{OUT}}$	Output Voltage Swing High	$R_{\text{LOAD}} = 2\text{ k}\Omega \text{ to } V^+/2$		35	75 <b>82</b>	mV from either rail
		$R_{\text{LOAD}} = 10\text{ k}\Omega \text{ to } V^+/2$		25	65 <b>71</b>	
	Output Voltage Swing Low	$R_{\text{LOAD}} = 2\text{ k}\Omega \text{ to } V^+/2$	LMV796/LMV796Q 42	42	75 <b>78</b>	
			LMV797 45	45	80 <b>83</b>	
		$R_{\text{LOAD}} = 10\text{ k}\Omega \text{ to } V^+/2$		20	65 <b>67</b>	
$I_{\text{OUT}}$	Output Current	Sourcing to $V^-$ $V_{\text{IN}} = 200\text{ mV}$ <sup>(6)</sup>	45 <b>37</b>	60		mA
		Sinking to $V^+$ $V_{\text{IN}} = -200\text{ mV}$ <sup>(6)</sup>	10 <b>6</b>	21		
$I_S$	Supply Current per Amplifier	LMV796/LMV796Q		1.15	1.40 <b>1.75</b>	mA
		LMV797per channel		1.30	1.70 <b>2.05</b>	
SR	Slew Rate	$A_V = +1$ , Rising (10% to 90%)	6.0	9.5		V/ $\mu\text{s}$
		$A_V = +1$ , Falling (90% to 10%)	7.5	11.5		
GBW	Gain Bandwidth			17		MHz
$e_n$	Input Referred Voltage Noise Density	$f = 1\text{ kHz}$		5.8		$\text{nV}/\sqrt{\text{Hz}}$
$i_n$	Input Referred Current Noise Density	$f = 1\text{ kHz}$		0.01		$\text{pA}/\sqrt{\text{Hz}}$

(1) Limits are 100% production tested at  $25^\circ\text{C}$ . Limits over the operating temperature range are guaranteed through correlations using the statistical quality control (SQC) method.

(2) Typical values represent the parametric norm at the time of characterization.

(3) Offset voltage average drift is determined by dividing the change in  $V_{\text{OS}}$  by temperature change.

(4) Positive current corresponds to current flowing into the device.

(5) This parameter is guaranteed by design and/or characterization and is not tested in production.

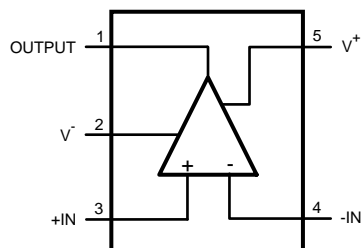
(6) The short circuit test is a momentary test, the short circuit duration is 1.5ms.

## 5V Electrical Characteristics (continued)

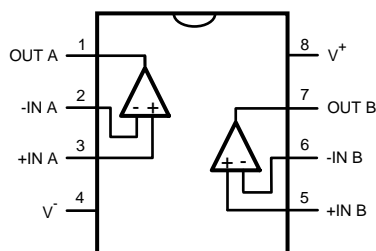
Unless otherwise specified, all limits are guaranteed for  $T_A = 25^\circ\text{C}$ ,  $V^+ = 5\text{V}$ ,  $V^- = 0\text{V}$ ,  $V_{CM} = V^+/2 = V_O$ . **Boldface** limits apply at the temperature extremes.

THD+N	Total Harmonic Distortion + Noise	$f = 1\text{ kHz}$ , $A_V = 1$ , $R_{LOAD} = 600\Omega$	0.01	%
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## Connection Diagram



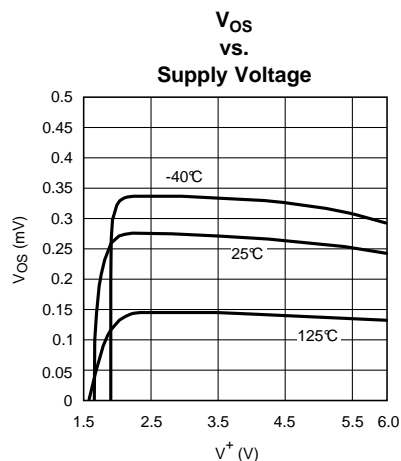
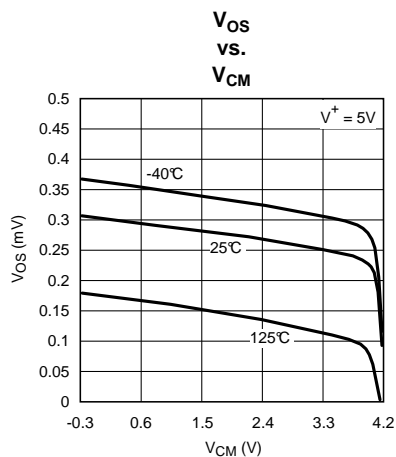
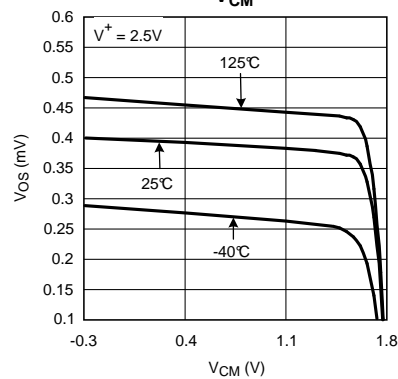
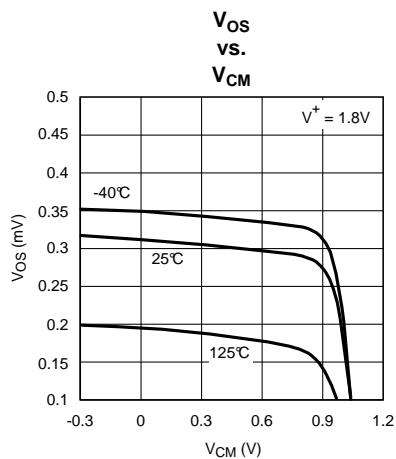
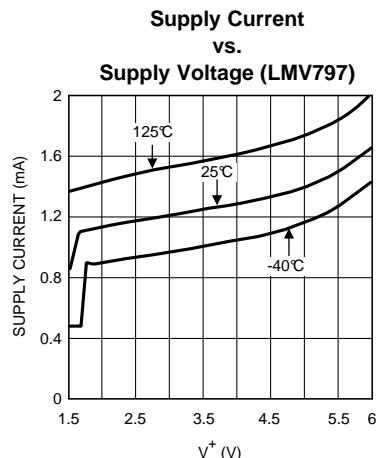
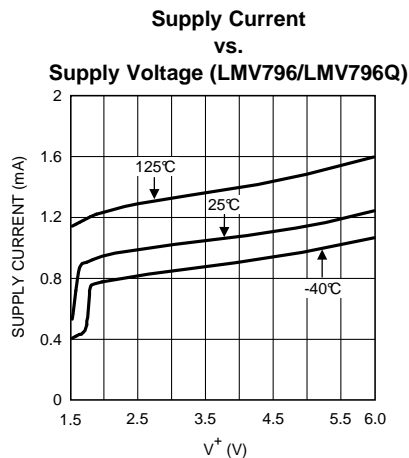
**Figure 3. 5-Pin SOT23 (Top View)**



**Figure 4. 8-Pin MSOP (Top View)**

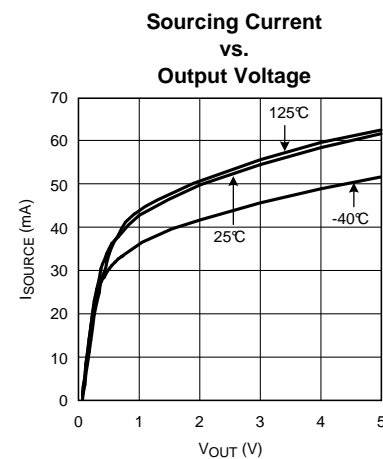
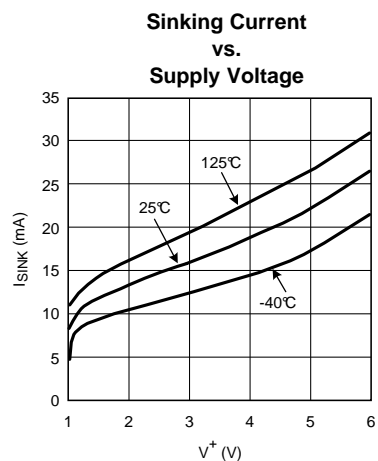
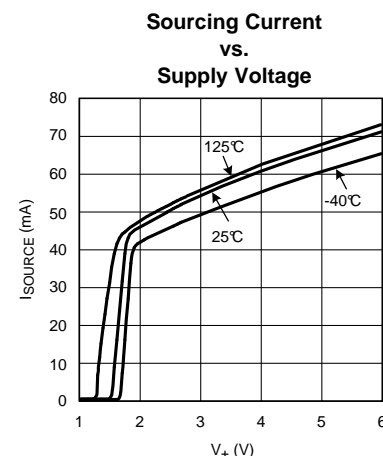
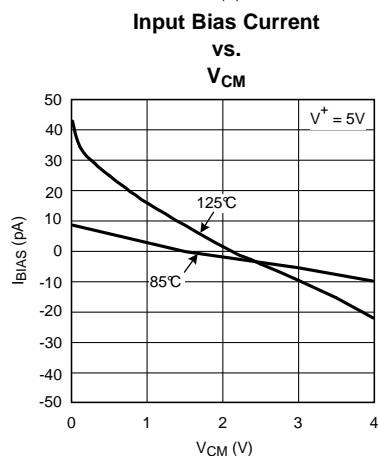
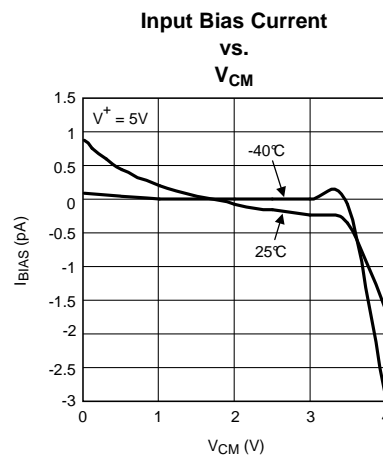
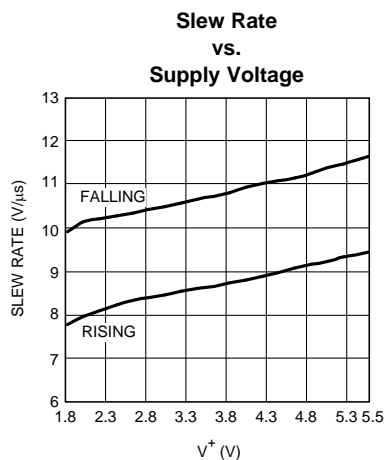
## Typical Performance Characteristics

Unless otherwise specified,  $T_A = 25^\circ\text{C}$ ,  $V^- = 0$ ,  $V^+ = \text{Supply Voltage} = 5\text{V}$ ,  $V_{CM} = V^+/2$ .



## Typical Performance Characteristics (continued)

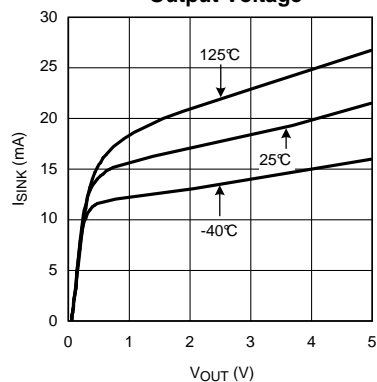
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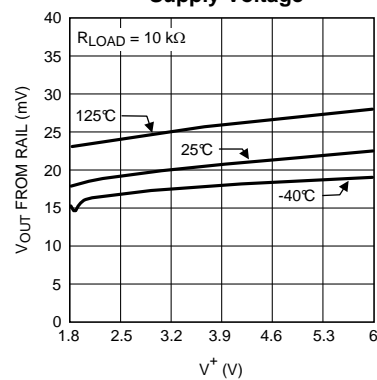
### Typical Performance Characteristics (continued)

Unless otherwise specified,  $T_A = 25^\circ\text{C}$ ,  $V^- = 0$ ,  $V^+ = \text{Supply Voltage} = 5\text{V}$ ,  $V_{CM} = V^+/2$ .

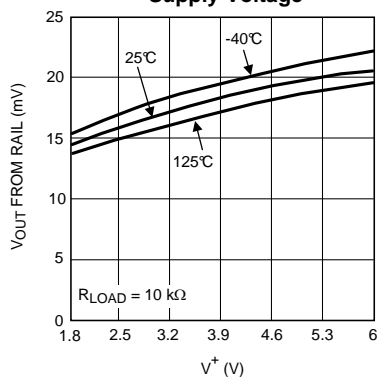
**Sinking Current  
vs.  
Output Voltage**



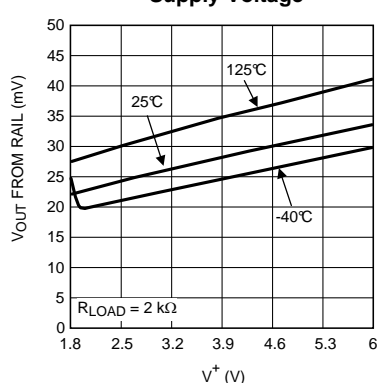
**Positive Output Swing  
vs.  
Supply Voltage**



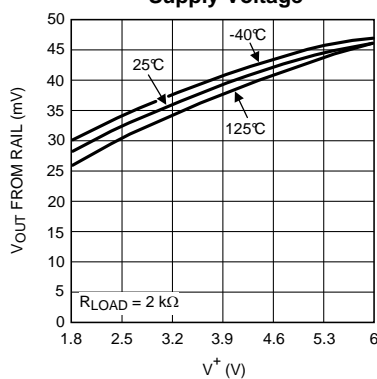
**Negative Output Swing  
vs.  
Supply Voltage**



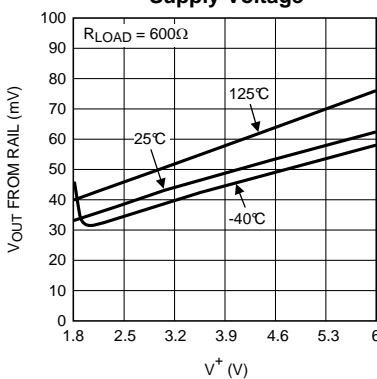
**Positive Output Swing  
vs.  
Supply Voltage**



**Negative Output Swing  
vs.  
Supply Voltage**



**Positive Output Swing  
vs.  
Supply Voltage**

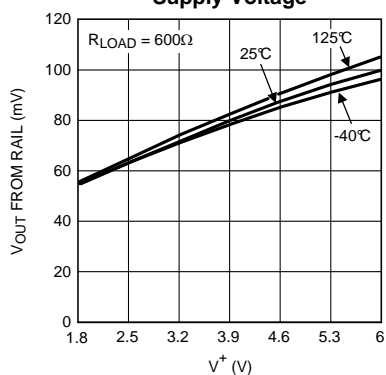




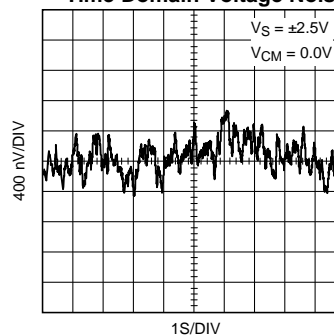
## Typical Performance Characteristics (continued)

Unless otherwise specified,  $T_A = 25^\circ\text{C}$ ,  $V^- = 0$ ,  $V^+ = \text{Supply Voltage} = 5\text{V}$ ,  $V_{CM} = V^+/2$ .

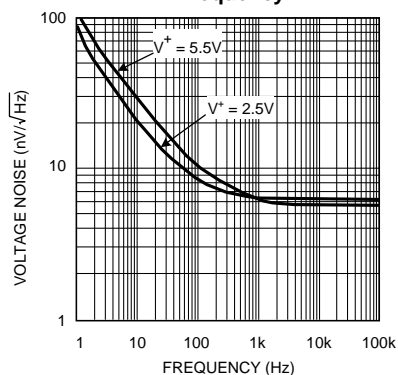
**Negative Output Swing  
vs.  
Supply Voltage**



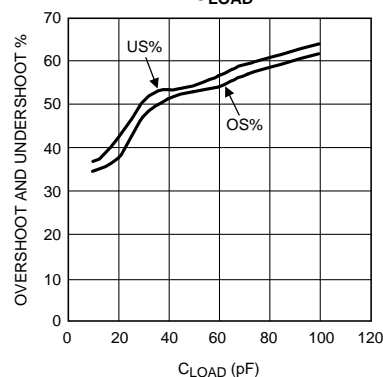
**Time Domain Voltage Noise**



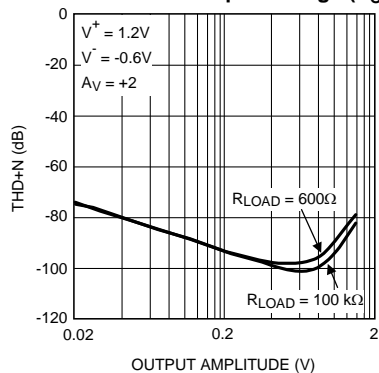
**Input Referred Voltage Noise  
vs.  
Frequency**



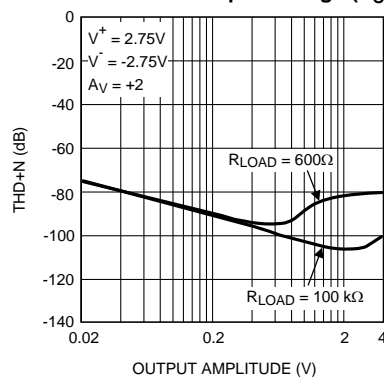
**Overshoot and Undershoot  
vs.  
CLOAD**



**THD+N  
vs.  
Peak-to-Peak Output Voltage ( $V_{OUT}$ )**

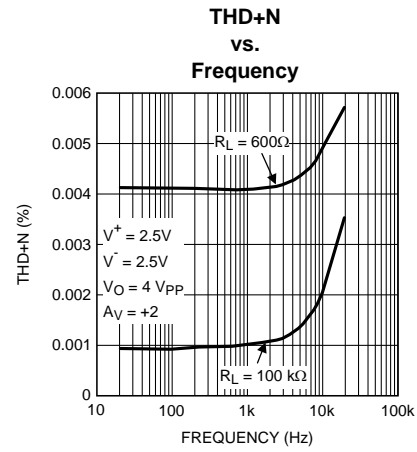
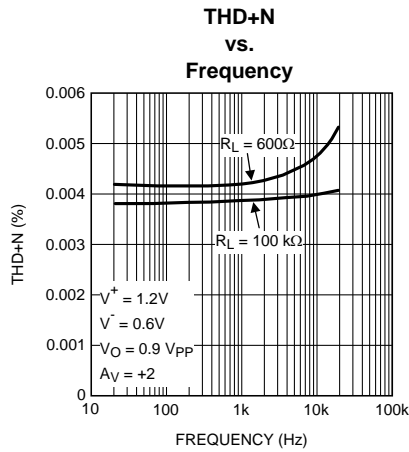


**THD+N  
vs.  
Peak-to-Peak Output Voltage ( $V_{OUT}$ )**

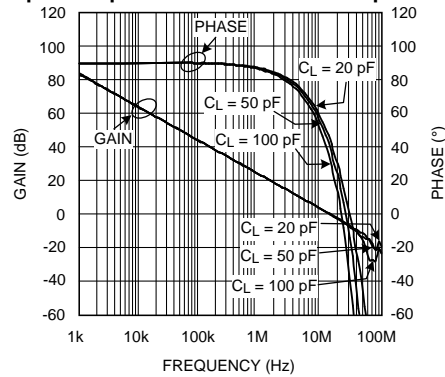


## Typical Performance Characteristics (continued)

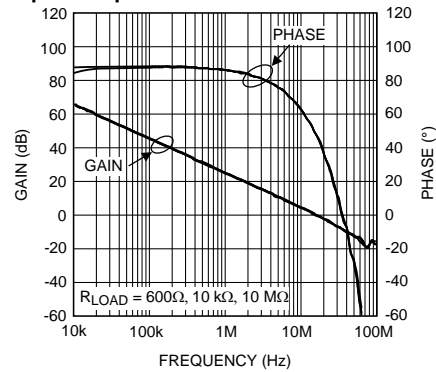
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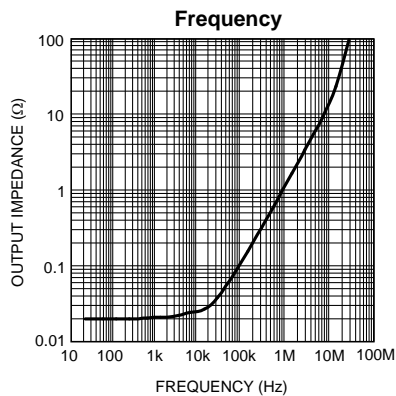
**Open Loop Gain and Phase with Capacitive Load**



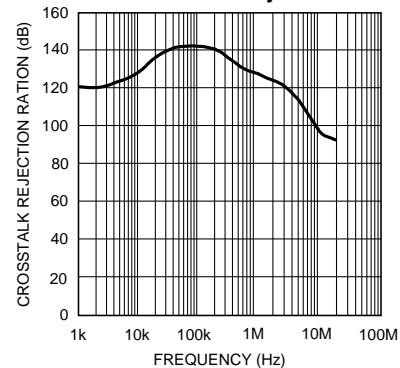
**Open Loop Gain and Phase with Resistive Load**



**Closed Loop Output Impedance vs. Frequency**



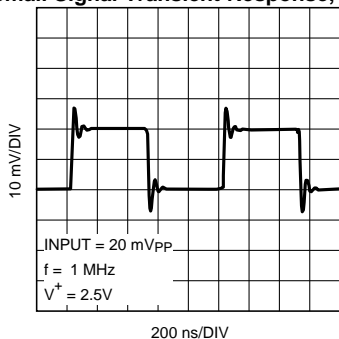
**Crosstalk Rejection**



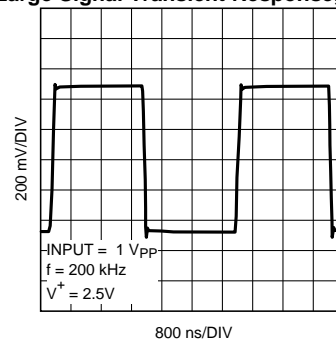
## Typical Performance Characteristics (continued)

Unless otherwise specified,  $T_A = 25^\circ\text{C}$ ,  $V^- = 0$ ,  $V^+ = \text{Supply Voltage} = 5\text{V}$ ,  $V_{CM} = V^+/2$ .

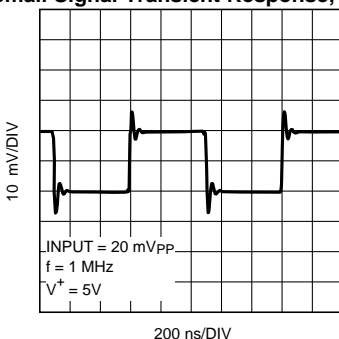
Small Signal Transient Response,  $A_V = +1$



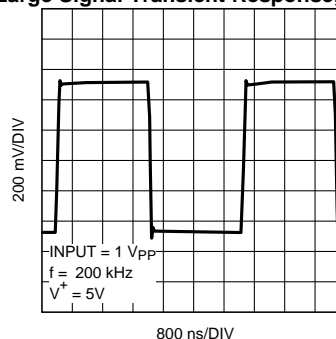
Large Signal Transient Response,  $A_V = +1$



Small Signal Transient Response,  $A_V = +1$

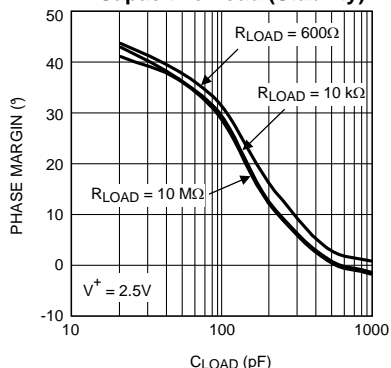


Large Signal Transient Response,  $A_V = +1$



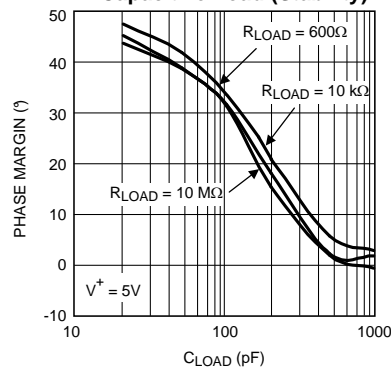
Phase Margin  
vs.

Capacitive Load (Stability)



Phase Margin  
vs.

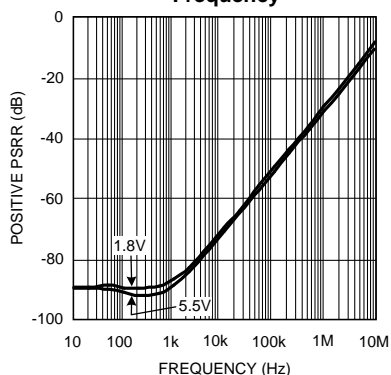
Capacitive Load (Stability)



Positive PSRR

vs.

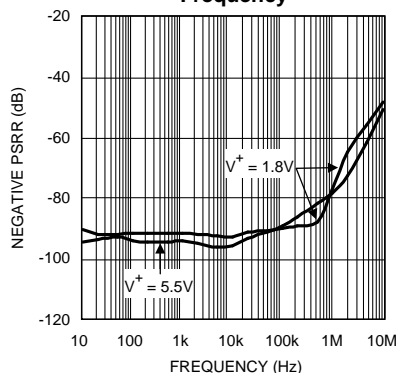
Frequency



Negative PSRR

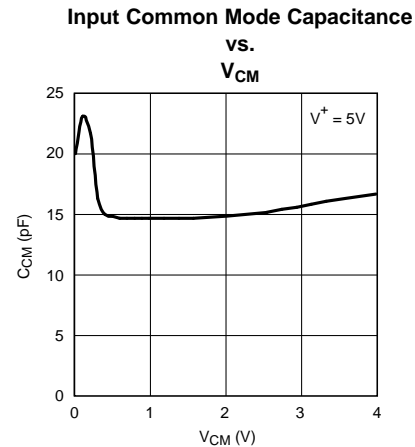
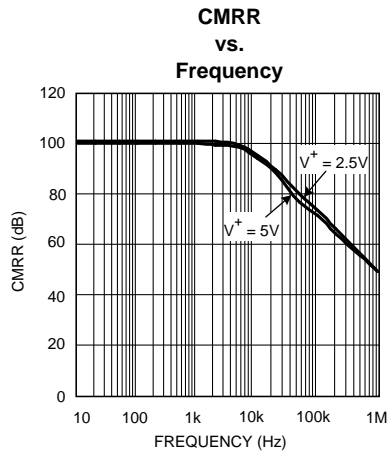
vs.

Frequency



### Typical Performance Characteristics (continued)

Unless otherwise specified,  $T_A = 25^\circ\text{C}$ ,  $V^- = 0$ ,  $V^+ = \text{Supply Voltage} = 5\text{V}$ ,  $V_{CM} = V^+/2$ .



## Application Information

### ADVANTAGES OF THE LMV796/LMV797

#### Wide Bandwidth at Low Supply Current

The LMV796 and LMV797 are high performance op amps that provide a unity gain bandwidth of 17 MHz while drawing a low supply current of 1.15 mA. This makes them ideal for providing wideband amplification in portable applications.

#### Low Input Referred Noise and Low Input Bias Current

The LMV796/LMV797 have a very low input referred voltage noise density ( $5.8 \text{ nV}/\sqrt{\text{Hz}}$  at 1 kHz). A CMOS input stage ensures a small input bias current (100 fA) and low input referred current noise ( $0.01 \text{ pA}/\sqrt{\text{Hz}}$ ). This is very helpful in maintaining signal fidelity, and makes the LMV796 and LMV797 ideal for audio and sensor based applications.

#### Low Supply Voltage

The LMV796 and the LMV797 have performance guaranteed at 2.5V and 5V supply. The LMV796 family is guaranteed to be operational at all supply voltages between 2.0V and 5.5V, for ambient temperatures ranging from  $-40^\circ\text{C}$  to  $125^\circ\text{C}$ , thus utilizing the entire battery lifetime. The LMV796 and LMV797 are also guaranteed to be operational at 1.8V supply voltage, for temperatures between  $0^\circ\text{C}$  and  $125^\circ\text{C}$ . This makes the LMV796 family ideal for usage in low-voltage commercial applications.

#### RRO and Ground Sensing

Rail-to-rail output swing provides maximum possible dynamic range at the output. This is particularly important when operating at low supply voltages. An innovative positive feedback scheme is used to boost the current drive capability of the output stage. This allows the LMV796 and the LMV797 to source more than 40 mA of current at 1.8V supply. This also limits the performance of the LMV796 family as comparators, and hence the usage of the LMV796 and the LMV797 in an open-loop configuration is not recommended. The input common-mode range includes the negative supply rail which allows direct sensing at ground in single supply operation.

#### Small Size

The small footprint of the LMV796 and the LMV797 package saves space on printed circuit boards, and enables the design of smaller electronic products, such as cellular phones, pagers, or other portable systems. Long traces between the signal source and the op amp make the signal path susceptible to noise. By using the physically smaller LMV796 or LMV797 package, the op amp can be placed closer to the signal source, reducing noise pickup and increasing signal integrity.

## CAPACITIVE LOAD TOLERANCE

The LMV796 and LMV797 can directly drive 120 pF in unity-gain without oscillation. The unity-gain follower is the most sensitive configuration to capacitive loading. Direct capacitive loading reduces the phase margin of amplifiers. The combination of the amplifier's output impedance and the capacitive load induces phase lag. This results in either an underdamped pulse response or oscillation. To drive a heavier capacitive load, the circuit in [Figure 5](#) can be used.

In [Figure 5](#), the isolation resistor  $R_{ISO}$  and the load capacitor  $C_L$  form a pole to increase stability by adding more phase margin to the overall system. The desired performance depends on the value of  $R_{ISO}$ . The bigger the  $R_{ISO}$  resistor value, the more stable  $V_{OUT}$  will be. Increased  $R_{ISO}$  would, however, result in a reduced output swing and short circuit current.

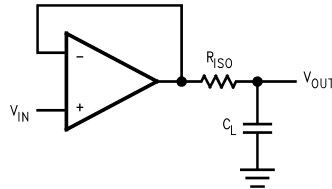
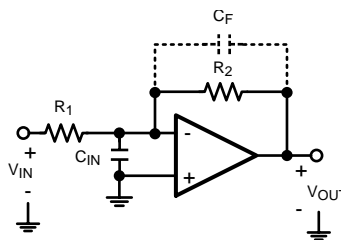


Figure 5. Isolation of  $C_L$  to Improve Stability

## INPUT CAPACITANCE AND FEEDBACK CIRCUIT ELEMENTS

The LMV796 family has a very low input bias current (100 fA) and a low  $1/f$  noise corner frequency (400 Hz), which makes it ideal for sensor applications. However, to obtain this performance a large CMOS input stage is used, which adds to the input capacitance of the op amp,  $C_{IN}$ . Though this does not affect the DC and low frequency performance, at higher frequencies the input capacitance interacts with the input and the feedback impedances to create a pole, which results in lower phase margin and gain peaking. This can be controlled by being selective in the use of feedback resistors, as well as, by using a feedback capacitance,  $C_F$ . For example, in the inverting amplifier shown in [Figure 6](#), if  $C_{IN}$  and  $C_F$  are ignored and the open loop gain of the op amp is considered infinite then the gain of the circuit is  $-R_2/R_1$ . An op amp, however, usually has a dominant pole, which causes its gain to drop with frequency. Hence, this gain is only valid for DC and low frequency. To understand the effect of the input capacitance coupled with the non-ideal gain of the op amp, the circuit needs to be analyzed in the frequency domain using a Laplace transform.



$$A_V = - \frac{V_{OUT}}{V_{IN}} = - \frac{R_2}{R_1}$$

Figure 6. Inverting Amplifier

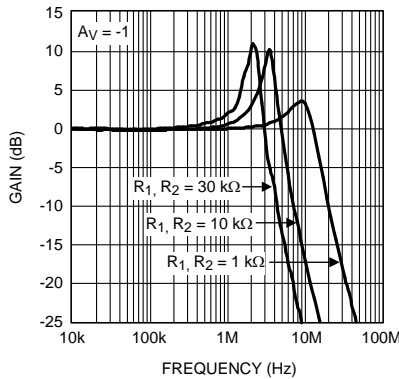
For simplicity, the op amp is modeled as an ideal integrator with a unity gain frequency of  $A_0$ . Hence, its transfer function (or gain) in the frequency domain is  $A_0/s$ . Solving the circuit equations in the frequency domain, ignoring  $C_F$  for the moment, results in an expression for the gain shown in [Equation 1](#).

$$\frac{V_{OUT}}{V_{IN}}(s) = \frac{-R_2/R_1}{1 + \frac{s}{\left(\frac{A_0 R_1}{R_1 + R_2}\right)} + \frac{s^2}{\left(\frac{A_0}{C_{IN} R_2}\right)}} \quad (1)$$

It can be inferred from the denominator of the transfer function that it has two poles, whose expressions can be obtained by solving for the roots of the denominator and are shown in [Equation 2](#).

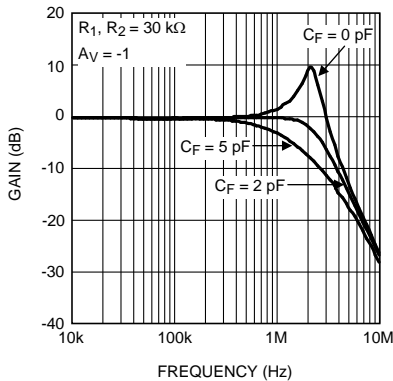
$$P_{1,2} = \frac{-1}{2C_{IN}} \left[ \frac{1}{R_1} + \frac{1}{R_2} \pm \sqrt{\left( \frac{1}{R_1} + \frac{1}{R_2} \right)^2 - \frac{4 A_0 C_{IN}}{R_2}} \right] \quad (2)$$

Equation 2 shows that as the values of  $R_1$  and  $R_2$  are increased, the magnitude of the poles, and hence the bandwidth of the amplifier, is reduced. This theory is verified by using different values of  $R_1$  and  $R_2$  in the circuit shown in Figure 5 and by comparing their frequency responses. In Figure 7 the frequency responses for three different values of  $R_1$  and  $R_2$  are shown. When both  $R_1$  and  $R_2$  are 1 k $\Omega$ , the response is flattest and widest; whereas, it narrows and peaks significantly when both their values are changed to 10 k $\Omega$  or 30 k $\Omega$ . So it is advisable to use lower values of  $R_1$  and  $R_2$  to obtain a wider and flatter response. Lower resistances also help in high sensitivity circuits since they add less noise.



**Figure 7. Gain Peaking Caused by Large  $R_1$ ,  $R_2$**

A way of reducing the gain peaking is by adding a feedback capacitance  $C_F$  in parallel with  $R_2$ . This introduces another pole in the system and prevents the formation of pairs of complex conjugate poles which cause the gain to peak. Figure 8 shows the effect of  $C_F$  on the frequency response of the circuit. Adding a capacitance of 2 pF removes the peak, while a capacitance of 5 pF creates a much lower pole and reduces the bandwidth excessively.



**Figure 8. Gain Peaking Eliminated by  $C_F$**

## AUDIO PREAMPLIFIER WITH BAND PASS FILTERING

With low input referred voltage noise, low supply voltage and current, and a low harmonic distortion, the LMV796 family is ideal for audio applications. Its wide unity gain bandwidth allows it to provide large gain for a wide range of frequencies and it can be used to design a preamplifier to drive a load of as low as 600Ω with less than 0.01% distortion. Two amplifier circuits are shown in Figure 9 and Figure 10. Figure 9 is an inverting amplifier, with a 10 kΩ feedback resistor,  $R_2$ , and a 1 kΩ input resistor,  $R_1$ , and hence provides a gain of -10. Figure 10 is a non-inverting amplifier, using the same values of  $R_1$  and  $R_2$ , and provides a gain of 11. In either of these circuits, the coupling capacitor  $C_{C1}$  decides the lower frequency at which the circuit starts providing gain, while the feedback capacitor  $C_F$  decides the frequency at which the gain starts dropping off. Figure 11 shows the frequency response of the inverting amplifier with different values of  $C_F$ .

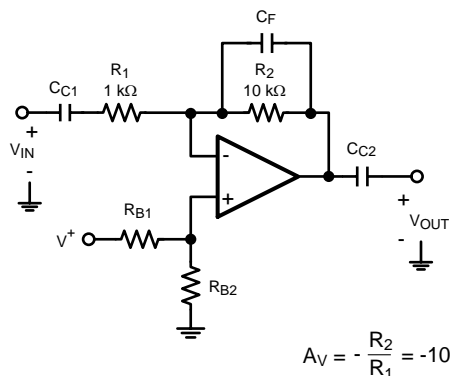


Figure 9. Inverting Audio Preamplifier

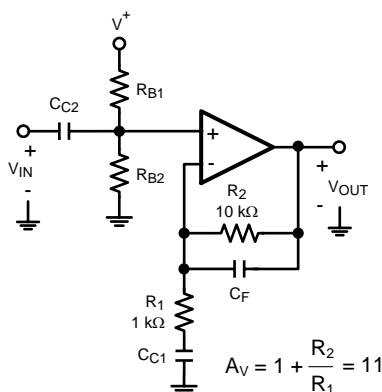
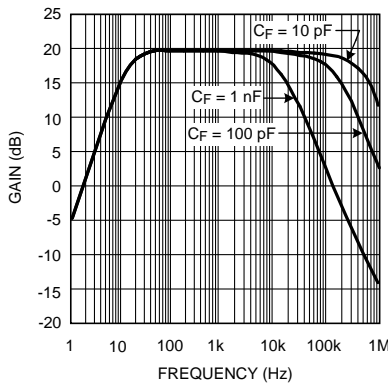


Figure 10. Non-inverting Audio Preamplifier



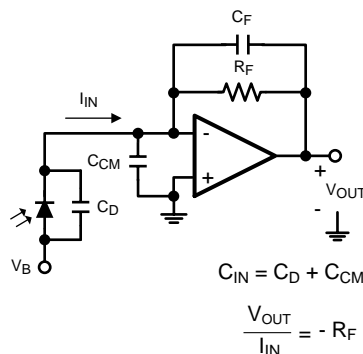
**Figure 11. Frequency Response of the Inverting Audio Preamplifier**

### TRANSIMPEDANCE AMPLIFIER

CMOS input op amps are often used in transimpedance applications as they have an extremely high input impedance. A transimpedance amplifier converts a small input current into a voltage. This current is usually generated by a photodiode. The transimpedance gain, measured as the ratio of the output voltage to the input current, is expected to be large and wide-band. Since the circuit deals with currents in the range of a few nA, low noise performance is essential. The LMV796/LMV797 are CMOS input op amps providing wide bandwidth and low noise performance, and are hence ideal for transimpedance applications.

Usually, a transimpedance amplifier is designed on the basis of the current source driving the input. A photodiode is a very common capacitive current source, which requires transimpedance gain for transforming its miniscule current into easily detectable voltages. The photodiode and the amplifier's gain are selected with respect to the speed and accuracy required of the circuit. A faster circuit would require a photodiode with lesser capacitance and a faster amplifier. A more sensitive circuit would require a sensitive photodiode and a high gain. A typical transimpedance amplifier is shown in [Figure 12](#). The output voltage of the amplifier is given by the equation  $V_{OUT} = -I_{IN}R_F$ . Since the output swing of the amplifier is limited,  $R_F$  should be selected such that all possible values of  $I_{IN}$  can be detected.

The LMV796/LMV797 have a large gain-bandwidth product (17 MHz), which enables high gains at wide bandwidths. A rail-to-rail output swing at 5.5V supply allows detection and amplification of a wide range of input currents. A CMOS input stage with negligible input current noise and low input voltage noise allows the LMV796/LMV797 to provide high fidelity amplification for wide bandwidths. These properties make the LMV796/LMV797 ideal for systems requiring wide-band transimpedance amplification.



**Figure 12. Photodiode Transimpedance Amplifier**



As mentioned earlier, the following parameters are used to design a transimpedance amplifier: the amplifier gain-bandwidth product,  $A_0$ ; the amplifier input capacitance,  $C_{CM}$ ; the photodiode capacitance,  $C_D$ ; the transimpedance gain required,  $R_F$ ; and the amplifier output swing. Once a feasible  $R_F$  is selected using the amplifier output swing, these numbers can be used to design an amplifier with the desired transimpedance gain and a maximally flat frequency response.

An essential component for obtaining a maximally flat response is the feedback capacitor,  $C_F$ . The capacitance seen at the input of the amplifier,  $C_{IN}$ , combined with the feedback capacitor,  $R_F$ , generate a phase lag which causes gain-peaking and can destabilize the circuit.  $C_{IN}$  is usually just the sum of  $C_D$  and  $C_{CM}$ . The feedback capacitor  $C_F$  creates a pole,  $f_p$  in the noise gain of the circuit, which neutralizes the zero in the noise gain,  $f_z$ , created by the combination of  $R_F$  and  $C_{IN}$ . If properly positioned, the noise gain pole created by  $C_F$  can ensure that the slope of the gain remains at 20 dB/decade till the unity gain frequency of the amplifier is reached, thus ensuring stability. As shown in Figure 13,  $f_p$  is positioned such that it coincides with the point where the noise gain intersects the op amp's open loop gain. In this case,  $f_p$  is also the overall -3 dB frequency of the transimpedance amplifier. The value of  $C_F$  needed to make it so is given by Equation 3. A larger value of  $C_F$  causes excessive reduction of bandwidth, while a smaller value fails to prevent gain peaking and instability.

$$C_F = \frac{1 + \sqrt{1 + 4\pi R_F C_{IN} A_0}}{2\pi R_F A_0} \quad (3)$$

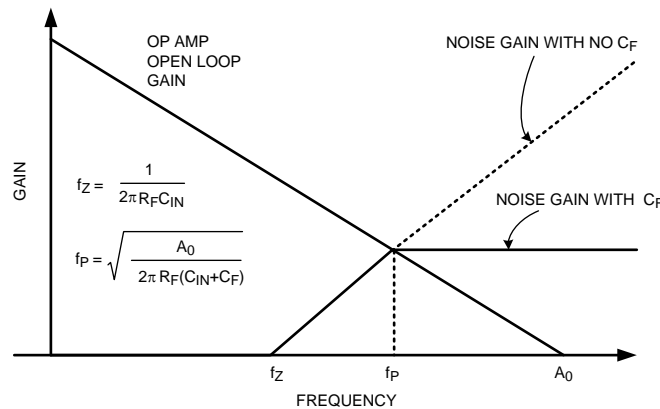


Figure 13.  $C_F$  Selection for Stability

Calculating  $C_F$  from Equation 3 can sometimes return unreasonably small values ( $<1$  pF), especially for high speed applications. In these cases, it is often more practical to use the circuit shown in Figure 14 in order to allow more reasonable values. In this circuit, the capacitance  $C_F'$  is  $(1 + R_B/R_A)$  times the effective feedback capacitance,  $C_F$ . A larger capacitor can now be used in this circuit to obtain a smaller effective capacitance.

For example, if a  $C_F$  of 0.5 pF is needed, while only a 5 pF capacitor is available,  $R_B$  and  $R_A$  can be selected such that  $R_B/R_A = 9$ . This would convert a  $C_F'$  of 5 pF into a  $C_F$  of 0.5 pF. This relationship holds as long as  $R_A \ll R_F$ .

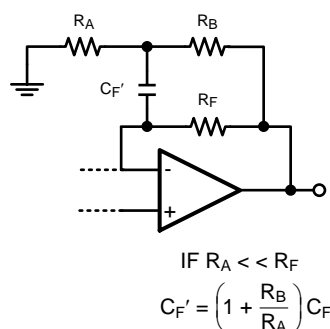


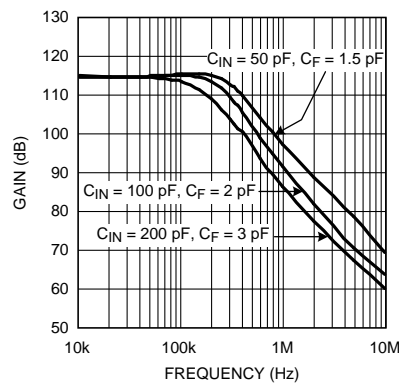
Figure 14. Obtaining Small  $C_F$  from Large  $C_F'$

## LMV796 AS A TRANSIMPEDANCE AMPLIFIER

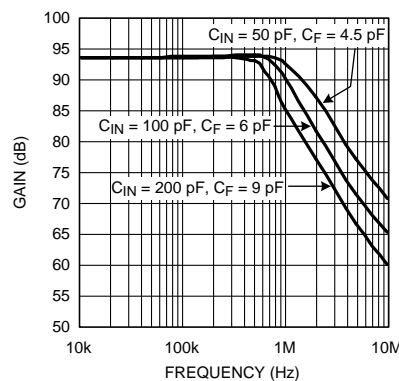
The LMV796 was used in the designs for a number of amplifiers with varying transimpedance gains and source capacitances. The gains, bandwidths and feedback capacitances of the circuits created are summarized in [Table 1](#). The frequency responses are presented in [Figure 15](#) and [Figure 16](#). The feedback capacitances are slightly different from the formula in [Equation 3](#), since the parasitic capacitance of the board and the feedback resistor  $R_F$  had to be accounted for.

**Table 1.**

Transimpedance, $A_{TI}$	$C_{IN}$	$C_F$	-3 dB Frequency
470000	50 pF	1.5 pF	350 kHz
470000	100 pF	2.0 pF	250 kHz
470000	200 pF	3.0 pF	150 kHz
47000	50 pF	4.5 pF	1.5 MHz
47000	100 pF	6.0 pF	1 MHz
47000	200 pF	9.0 pF	700 kHz



**Figure 15. Frequency Response for  $A_{TI} = 470000$**

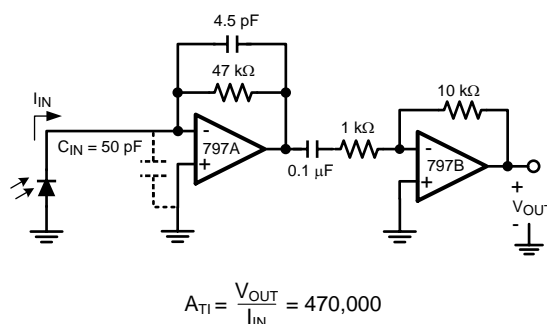


**Figure 16. Frequency Response for  $A_{TI} = 47000$**

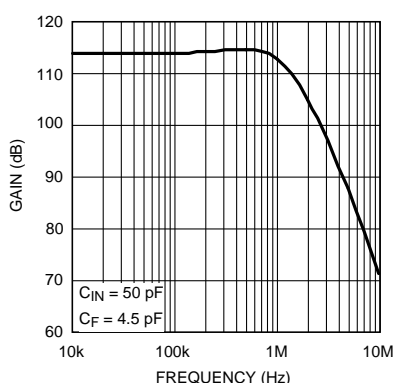
## HIGH GAIN WIDEBAND TRANSIMPEDANCE AMPLIFIER USING THE LMV797

The LMV797 dual, low noise, wide bandwidth, CMOS input op amp IC can be used for compact, robust and integrated solutions for sensing and amplifying wide-band signals obtained from sensitive photodiodes. One of the two op amps available can be used to obtain transimpedance gain while the other can be used for amplifying the output voltage to further enhance the transimpedance gain. The wide bandwidth of the op amps (17 MHz) ensures that they are capable of providing high gain for a wide range of frequencies. The low input referred noise (5.8 nV/ $\sqrt{\text{Hz}}$ ) allows the amplifier to deliver an output with a high SNR (signal to noise ratio). The small 8-pin MSOP footprint saves space on printed circuit boards and allows ease of design in portable products.

The circuit shown in Figure 17, has the first op amp acting as a transimpedance amplifier with a gain of 47000, while the second stage provides a voltage gain of 10. This provides a total transimpedance gain of 470000 with a –3 dB bandwidth of about 1.5 MHz, for a total input capacitance of 50 pF. The frequency response for the circuit is shown in Figure 18



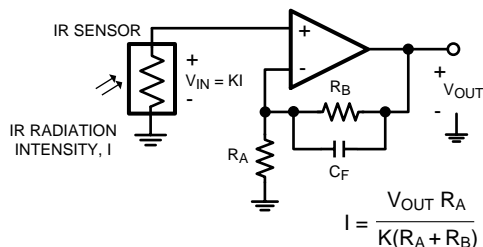
**Figure 17. 1.5 MHz Transimpedance Amplifier with  $A_{TI} = 470000$**



**Figure 18. 1.5 MHz Transimpedance Amplifier Frequency Response**

## SENSOR INTERFACES

The low input bias current and low input referred noise of the LMV796 and LMV797 make them ideal for sensor interfaces. These circuits are required to sense voltages of the order of a few  $\mu\text{V}$  and currents amounting to less than a nA hence, the op amp needs to have low voltage noise and low input bias current. Typical applications include infra-red (IR) thermometry, thermocouple amplifiers and pH electrode buffers. Figure 19 is an example of a typical circuit used for measuring IR radiation intensity, often used for estimating the temperature of an object from a distance. The IR sensor generates a voltage proportional to  $I$ , which is the intensity of the IR radiation falling on it. As shown in Figure 19,  $K$  is the constant of proportionality relating the voltage across the IR sensor ( $V_{IN}$ ) to the radiation intensity,  $I$ . The resistances  $R_A$  and  $R_B$  are selected to provide a high gain to amplify this voltage, while  $C_F$  is added to filter out the high frequency noise.



**Figure 19. IR Radiation Sensor**

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
LMV796MF	ACTIVE	SOT-23	DBV	5	1000	TBD	CU SNPB	Level-1-260C-UNLIM	-40 to 125	AT3A	<a href="#">Samples</a>
LMV796MF/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	AT3A	<a href="#">Samples</a>
LMV796MFX	ACTIVE	SOT-23	DBV	5	3000	TBD	CU SNPB	Level-1-260C-UNLIM	-40 to 125	AT3A	<a href="#">Samples</a>
LMV796MFX/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	AT3A	<a href="#">Samples</a>
LMV796QMF/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	AD7A	<a href="#">Samples</a>
LMV796QMFX/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	AD7A	<a href="#">Samples</a>
LMV797MM	ACTIVE	VSSOP	DGK	8	1000	TBD	CU SNPB	Level-1-260C-UNLIM	-40 to 125	AU3A	<a href="#">Samples</a>
LMV797MM/NOPB	ACTIVE	VSSOP	DGK	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	AU3A	<a href="#">Samples</a>
LMV797MMX	ACTIVE	VSSOP	DGK	8	3500	TBD	CU SNPB	Level-1-260C-UNLIM	-40 to 125	AU3A	<a href="#">Samples</a>
LMV797MMX/NOPB	ACTIVE	VSSOP	DGK	8	3500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	AU3A	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

<sup>(4)</sup> Only one of markings shown within the brackets will appear on the physical device.

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**OTHER QUALIFIED VERSIONS OF LMV796, LMV796-Q1 :**

- Catalog: [LMV796](#)
- Automotive: [LMV796-Q1](#)

**NOTE: Qualified Version Definitions:**

- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

**TAPE AND REEL INFORMATION**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMV796MF	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV796MF/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV796MFX	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV796MFX/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV796QMF/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV796QMFX/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV797MM	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMV797MM/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMV797MMX	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMV797MMX/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

## TAPE AND REEL BOX DIMENSIONS

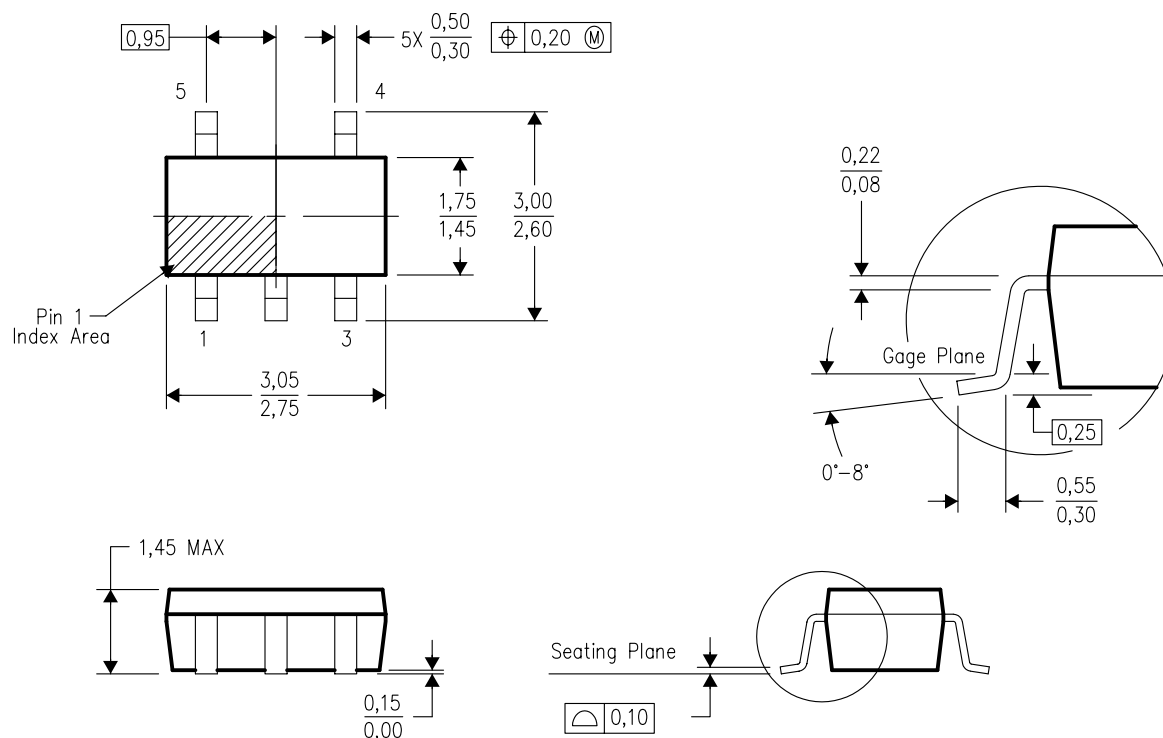


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMV796MF	SOT-23	DBV	5	1000	203.0	190.0	41.0
LMV796MF/NOPB	SOT-23	DBV	5	1000	203.0	190.0	41.0
LMV796MFX	SOT-23	DBV	5	3000	206.0	191.0	90.0
LMV796MFX/NOPB	SOT-23	DBV	5	3000	206.0	191.0	90.0
LMV796QMF/NOPB	SOT-23	DBV	5	1000	203.0	190.0	41.0
LMV796QMFX/NOPB	SOT-23	DBV	5	3000	206.0	191.0	90.0
LMV797MM	VSSOP	DGK	8	1000	203.0	190.0	41.0
LMV797MM/NOPB	VSSOP	DGK	8	1000	203.0	190.0	41.0
LMV797MMX	VSSOP	DGK	8	3500	349.0	337.0	45.0
LMV797MMX/NOPB	VSSOP	DGK	8	3500	349.0	337.0	45.0

## DBV (R-PDSO-G5)

## PLASTIC SMALL-OUTLINE PACKAGE



4073253-4/K 03/2006

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
  - D. Falls within JEDEC MO-178 Variation AA.



DBV (R-PDSO-G5)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
  - D. Publication IPC-7351 is recommended for alternate designs.
  - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

## DGK (S-PDSO-G8)

## PLASTIC SMALL-OUTLINE PACKAGE



## NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
- E. Falls within JEDEC MO-187 variation AA, except interlead flash.

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