LMX2370 PLLatinum™ Dual Frequency Synthesizer for RF Personal Communications LMX2370 2.5 GHz/1.2 GHz

Check for Samples: LMX2370, LMX2371, LMX2372

FEATURES

- **2.7V–5.5V Operation**
- **Ultra Low Current Consumption**
- **Low Phase Detector Noise Floor**
- **Low Voltage MICROWIRE Interface (1.8V up to V_{CC})**
- **Low Prescaler Values**
  - **32/33 at $f_{IN} \leq 2.5$ GHz**
  - **16/17 at $f_{IN} \leq 1.2$ GHz**
- **Selectable Charge Pump Current Levels**
- **Selectable FastLock mode**
- **Enhanced ESD Protection**
- **Available in Small 24-pad PLGA Package (3.5 x 4.5 x 1.0 mm)**
- **Available in Small 24-pad Chip Thin Scale Package (3.5 x 4.5 x 0.8 mm)**

APPLICATIONS

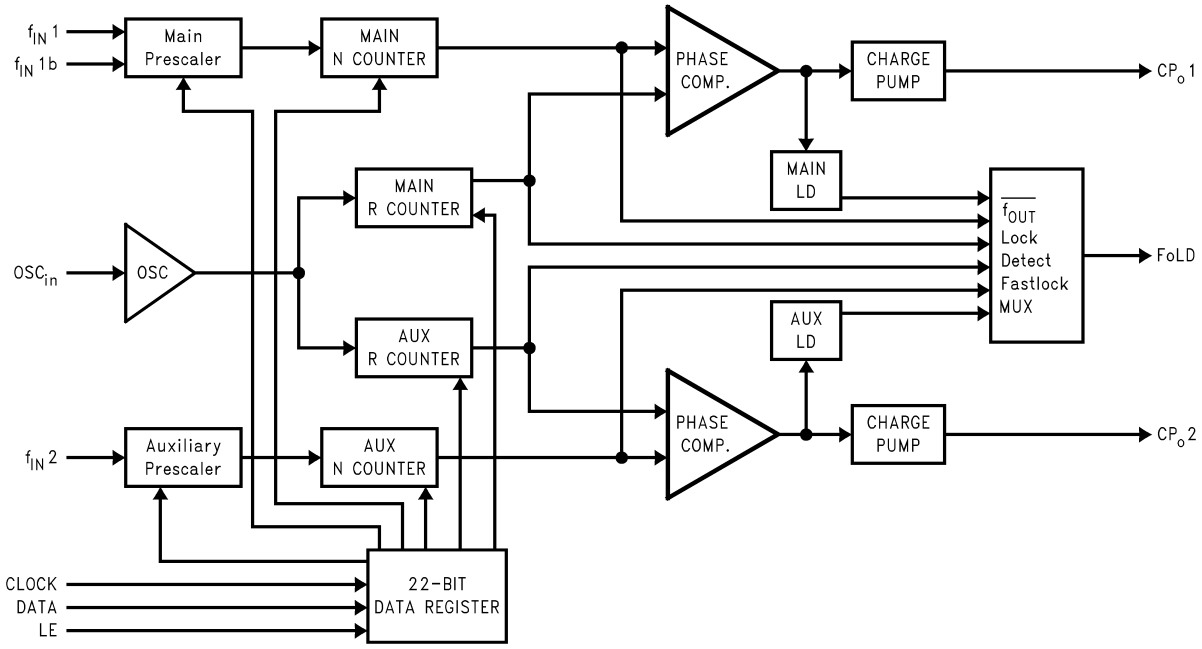
- **Portable Wireless Communications (PCS/PCN, cordless)**
- **Dual Mode Cellular Telephone Systems**
- **Spread Spectrum Communication Systems (CDMA)**
- **Cable TV Tuners (CATV)**

DESCRIPTION

The LMX2370 monolithic, integrated dual frequency synthesizer, including prescalers, is designed to be used as a first and second local oscillator for dual mode or dual conversion transceivers. It is fabricated using TI's 0.5u ABiCV silicon BiCMOS process. The LMX2370 contains two dual modulus prescalers. A 32/33 or a 16/17 prescaler can be selected for the Main synthesizer and a 16/17 or 8/9 prescaler can be selected for the Aux synthesizer. Using a digital phase locked loop technique, the LMX2370 generates very stable, low noise control signals for UHF and VHF voltage controlled oscillators (VCOs). Serial data is transferred into the LMX2370 via a 1.8 V three wire interface (Data, Enable, Clock) compatible with low voltage baseband processors. Supply voltage can range from 2.7V to 5.5V. The LMX2370 features very low current consumption typically: - 6.0 mA at 3V.

The LMX2370 is available in a 24-pad PLGA, 24-pad thin chip scale (TCSP) or 20-pin TSSOP surface mount plastic packages.

Functional Block Diagram



Connection Diagram

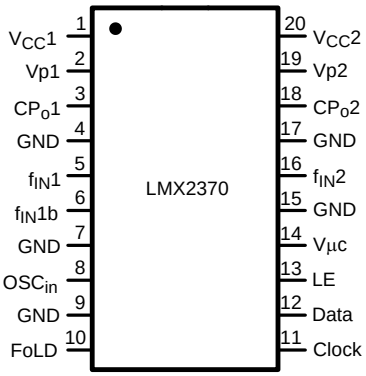


Figure 1. Top View
TSSOP 20-Pin Package
See Package Number PW0020A

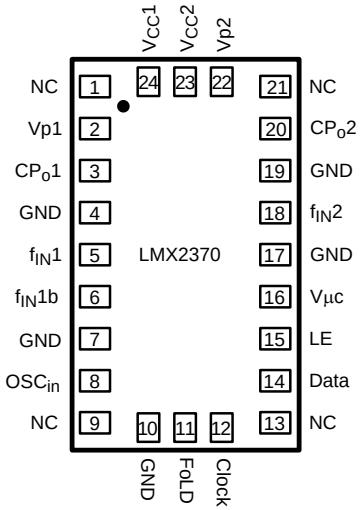
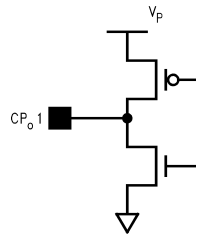
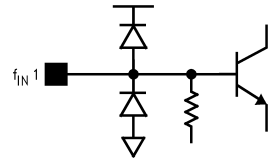
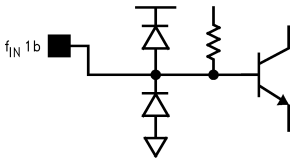
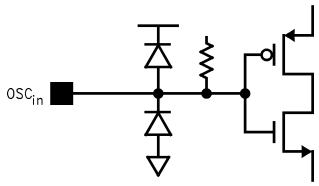
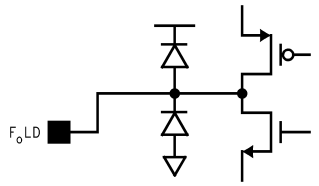
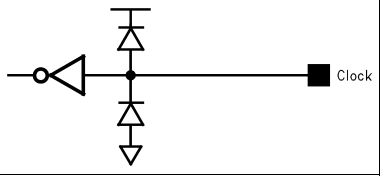
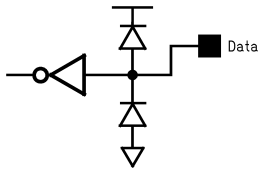
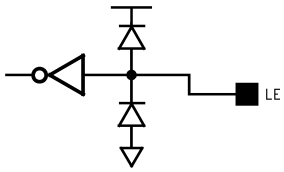
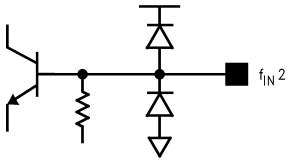
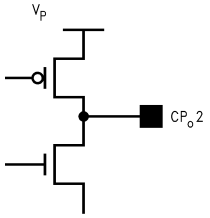


Figure 2. Top View
PLGA/TCSP 24-Pin Package
See Package Number NPH0024A
See Package Number SLD24A

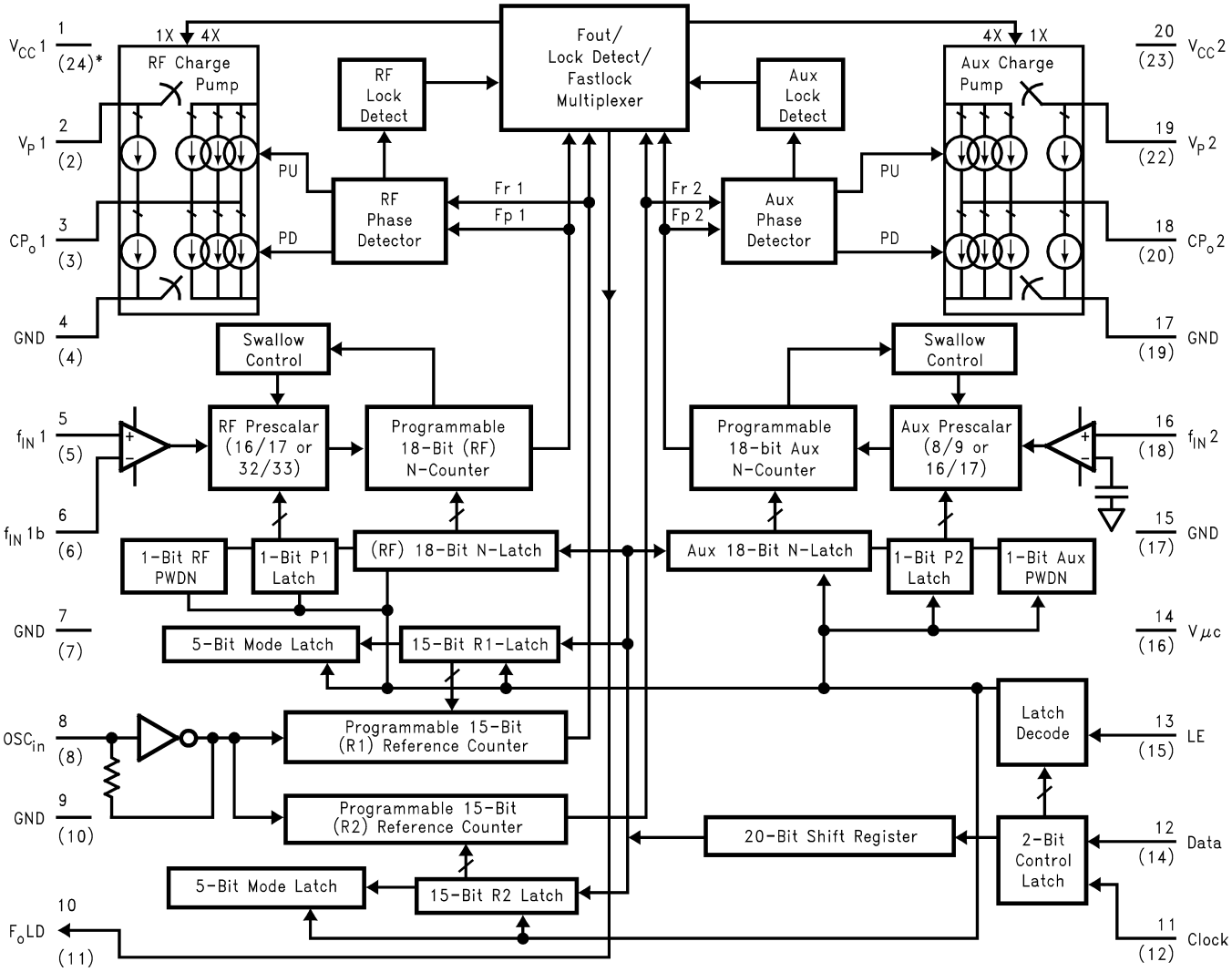
PIN DESCRIPTIONS

Pin No.		Pin Name	I/O	Description	
24-Pin PLGA/TCSP	20-Pin TSSOP				
24	1	$V_{CC}1$	—	Power supply voltage input for RF analog and RF digital circuits. Input may range from 2.7V to 5.5V. $V_{CC}1$ must equal $V_{CC}2$. Bypass capacitors should be placed as close as possible to this pin and be connected directly to the ground plane.	
2	2	Vp1	—	Power supply for Main charge pump. Must be ≥ V_{CC}.	
3	3	CP_o1	O	Internal Main charge pump output. For connection to a loop filter for driving the input of an external VCO.	
4	4	GND	—	Ground for Main digital circuitry.	
5	5	$f_{IN}1$	I	Main prescaler input. Small signal input from the VCO.	
6	6	$f_{IN}1b$	I	Main prescaler complementary input. For single ended operation, a bypass capacitor should be placed as close as possible to this pin and be connected directly to the ground plane.	
7	7	GND	—	Ground for Main analog circuitry.	
8	8	OSC_{in}	I	Oscillator input. The input has a $V_{CC}/2$ input threshold and can be driven from an external CMOS or TTL logic gate.	
10	9	GND	—	Ground for Aux digital, MICROWIRE, FoLD, and oscillator circuits.	
11	10	Fo/LD	O	Multiplexed output of the Main/Aux programmable or reference dividers, Main/Auxiliary lock detect signals and Fastlock mode. CMOS output *(see PROGRAMMABLE MODES in the Datasheet).*	
12	11	Clock	I	High impedance CMOS Clock input. Data for the various counters is clocked in on the rising edge, into the 22-bit shift register.	

PIN DESCRIPTIONS (continued)

Pin No.		Pin Name	I/O	Description	
24-Pin PLGA/T CSP	20-Pin TSSOP				
14	12	Data	I	Binary serial data input. Data entered MSB first. The last two bits are the control bits. High impedance CMOS input.	
15	13	LE	I	Load enable. High impedance CMOS input. When LE goes HIGH, data stored in the shift registers is loaded into one of the 4 appropriate latches (control bit dependent).	
16	14	Vμc	—	Power supply for MICROWIRE circuitry. Must be ≤ V_{CC}. Typically connected to same supply level as μprocessor or baseband controller to enable programming at low voltages.	
17	15	GND	—	Ground for Aux analog circuitry.	
18	16	$f_{IN}2$	I	Auxiliary prescaler input. Small signal input from the VCO.	
19	17	GND	—	Ground for Aux digital, MICROWIRE, FoLD, and oscillator.	
20	18	CP_o2	O	Aux internal charge pump output. For connection to a loop filter for driving the input of an external VCO.	
22	19	Vp2	—	Power supply for Aux charge pump. Must be ≥ V_{CC}.	
23	20	$V_{CC}2$	—	Power supply voltage input for Aux analog, Aux digital, FoLD, and oscillator circuits. Input may range from 2.7V to 5.5V. $V_{CC}2$ must equal $V_{CC}1$. Bypass capacitors should be placed as close as possible to this pin and be connected directly to the ground plane.	
1, 9, 13, 21	—	NC	—	No Connect	

Block Diagram



NOTE: * The numbers in () represent the equivalent PLGA pinout

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings(1)(2)(3)

Power Supply Voltage	
$V_{CC}1$	−0.3V to 6.5V
$V_{CC}2$	−0.3V to 6.5V
Vp1	−0.3V to 6.5V
Vp2	−0.3V to 6.5V
Vμc	−0.3V to 6.5V
Voltage on any pin with	
GND = 0V (V_I)	−0.3V to V_{CC} +0.3V
Storage Temperature Range (T_S)	−65°C to +150°C
Lead Temperature (solder, 4 sec.) (T_L)	+260°C
ESD - Human Body Model (1)	< 2 keV

(1) This device is a high performance RF integrated circuit and is ESD sensitive. Handling and assembly of this device should only be done at ESD free workstations.
(2) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see the Electrical Characteristics. The ensured specifications apply only for the test conditions listed.
(3) If Military/Aerospace specified devices are required, please contact the TI Sales Office/ Distributors for availability and specifications.

Recommended Operating Conditions(1)

Power Supply Voltage	
$V_{CC}1$	2.7V to 5.5V
$V_{CC}2$	2.7V to 5.5V
$V_{CC}1$–$V_{CC}2$	−0.2V to 0.2V
Vp1	V_{CC} to 5.5V
Vp2	V_{CC} to 5.5V
Vμc	1.72V to V_{CC}
Operating Temperature (T_A)	−40°C to +85°C

(1) V_{CC} is defined as $V_{CC} = V_{CC}1 = V_{CC}2$.

Electrical Characteristics

(V_{CC} = Vp = Vμc = 3.0V; −40°C < T_A < 85°C except as specified).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
GENERAL						
I_{CC}	Power Supply Current	Main = On, Aux = On		6	8.5	mA
		Aux Only		2	3.25	mA
$I_{CC\text{-}PWDN}$	Power Down Current	EN_Main, EN_Aux = 0		15	50	μA
$f_{IN}1$	Main PLL Operating Frequency	P = 32/33	1.2		2.5	GHz
		P = 16/17	45		1200	MHz
$f_{IN}2$	Auxiliary PLL Operating Frequency	P = 16/17	45		1200	MHz
		P = 8/9	45		550	MHz
fφ	Phase Detector Frequency				10	MHz
$Pf_{IN}1$, $Pf_{IN}2$	RF Input Sensitivity	2.7 ≤ V_{CC} ≤ 3.6V	−15		0	dBm
		3.6 ≤ V_{CC} ≤ 5.5V	−10		0	dBm

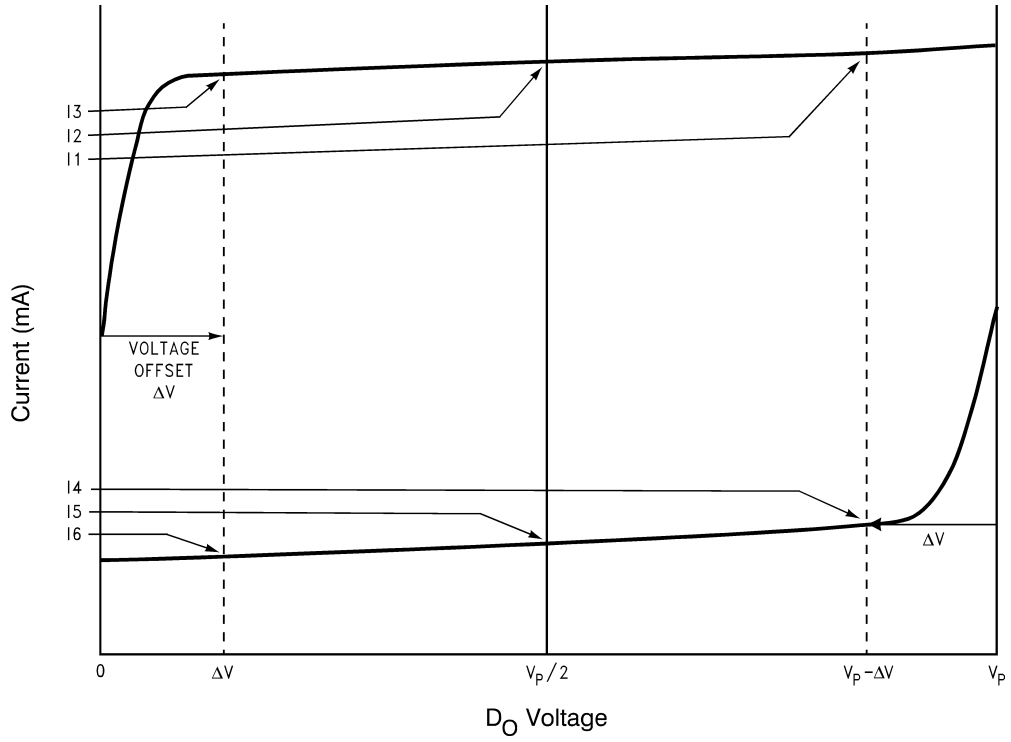
Electrical Characteristics (continued)

(V_{CC} = Vp = Vμc = 3.0V; −40°C < T_A < 85°C except as specified).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
OSCILLATOR INPUT						
OSC_{in}	Reference Oscillator Input Operating Frequency		2		50	MHz
V_{OSC}	Oscillator Input Sensitivity	OSC_{in}	0.5		V_{CC}	V_{PP}
I_{IH}	OSC_{in} Input Current	V_{IH} = V_{CC} = 5.5V			100	μA
I_{IL}	OSC_{in} Input Current	V_{IL} = 0, V_{CC} = 5.5V	−100			μA
CHARGE PUMP						
$ICP_{o\text{-}source}$	Main and Auxiliary Charge Pump Output Current (1)	VCP_o = Vp/2, **ICP_o_4X** = 0		- 1.0		mA
$ICP_{o\text{-}sink}$		VCP_o = Vp/2, **ICP_o_4X** = 0		1.0		mA
$ICP_{o\text{-}source}$		VCP_o = Vp/2, **ICP_o_4X** = 1		- 4.0		mA
$ICP_{o\text{-}sink}$		VCP_o = Vp/2, **ICP_o_4X** = 1		4.0		mA
$ICP_{o\text{-}TRI}$	Charge Pump TRI-STATE Current	0.5 ≤ VCP_o ≤ Vp − 0.5, −40°C < T_A < 85°C	−2.5	0.1	2.5	nA
$ICP_{o\text{-}sink}$ vs $ICP_{o\text{-}source}$	CP Sink vs Source Mismatch	VCP_o = Vp/2, T_A = 25°C		3	10	%
ICP_o vs VCP_o	CP Current vs Voltage	0.5 ≤ VCP_o ≤ Vp − 0.5, T_A = 25°C		8	15	%
ICP_o vs T_A	CP Current vs Temperature	VCP_o = Vp/2, −40°C < T_A < 85°C		8		%
DIGITAL INTERFACE (DATA, CLOCK, LE)						
V_{IH}	High-Level Input Voltage	Vμc = 1.72V to 5.5V	0.8 Vμc			V
V_{IL}	Low-Level Input Voltage	Vμc = 1.72V to 5.5V			0.2 Vμc	V
I_{IH}	High-Level Input Current	V_{IH} = Vμc = 5.5V	−1.0		1.0	μA
I_{IL}	Low-Level Input Current	V_{IL} = 0, Vμc = 5.5V	−1.0		1.0	μA
V_{OL}	Low-Level Output Current	I_{OL} = 1.0 mA, V_{EXT} = 1.8V (2)		0.1	0.4	V
MICROWIRE TIMING						
t_{CS}	Data to Clock Setup Time	See Data Input Timing	50			ns
t_{CH}	Data to Clock Hold Time	See Data Input Timing	20			ns
t_{CWH}	Clock Pulse Width High	See Data Input Timing	50			ns
t_{CWL}	Clock Pulse Width Low	See Data Input Timing	50			ns
t_{ES}	Clock to Load Enable Setup Time	See Data Input Timing	50			ns
t_{EW}	Load Enable Pulse Width	See Data Input Timing	50			ns

(1) Main and Auxiliary Charge Pump magnitude are controlled by Main_ICP_o_4X and Aux_ICP_o_4X bits respectively.
(2) Lock Detect open drain output only pulled up to V_{EXT}. Typically V_{EXT} = V_{CC}.

Charge Pump Current Specification Definitions



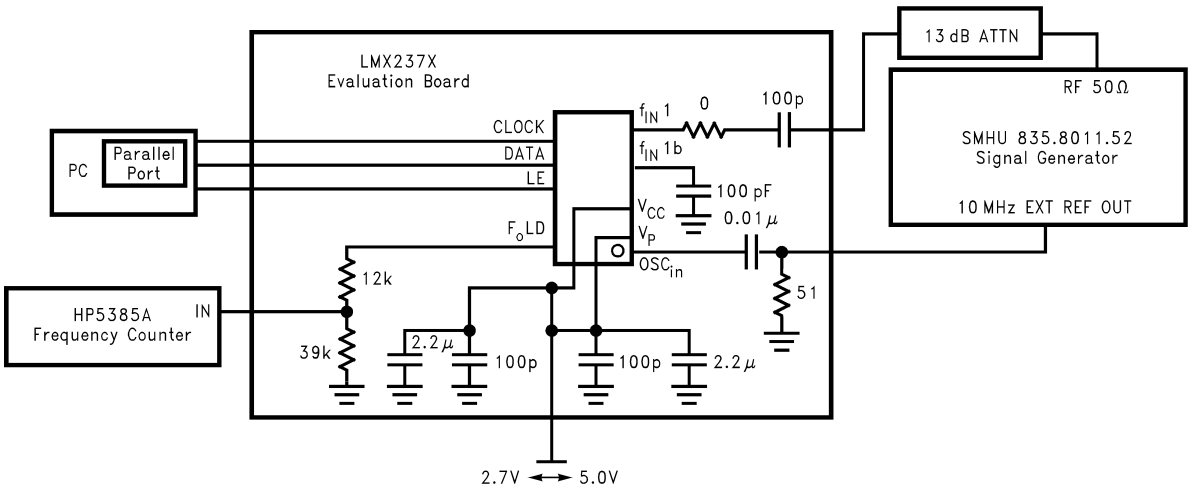
I1 = CP sink current at $V_{Do} = V_P - \Delta V$
I2 = CP sink current at $V_{Do} = V_P/2$
I3 = CP sink current at $V_{Do} = \Delta V$
I4 = CP source current at $V_{Do} = V_P - \Delta V$
I5 = CP source current at $V_{Do} = V_P/2$
I6 = CP source current at $V_{Do} = \Delta V$
ΔV = Voltage offset from positive and negative rails. Dependent on VCO tuning range relative to V_{CC} and ground. Typical values are between 0.5V and 1.0V.

(1) I_{Do} vs V_{Do} = Charge Pump Output Current magnitude variation vs Voltage = [½ * {|I1| − |I3|}]/[½ * {|I1| + |I3|}] * 100% and [½ * {|I4| − |I6|}]/[½ * {|I4| + |I6|}] * 100%

(2) $I_{Do\text{-}sink}$ vs $I_{Do\text{-}source}$ = Charge Pump Output Current Sink vs Source Mismatch = [|I2| − |I5|]/[½ * {|I2| + |I5|}] * 100%

(3) I_{Do} vs T_A = Charge Pump Output Current magnitude variation vs Temperature = [|I2 @ temp| − |I2 @ 25°C|]/|I2 @ 25°C| * 100% and [|I5 @ temp| − |I5 @ 25°C|]/|I5 @ 25°C| * 100%

RF Sensitivity Test Block Diagram



Note: N = 10,000 R = 50 P = 64

Sensitivity limit is reached when the error of the divided RF output, F_oLD, is ≥ 1 Hz.

Typical Performance Characteristics

I_{CC} vs V_{CC} LMX2370

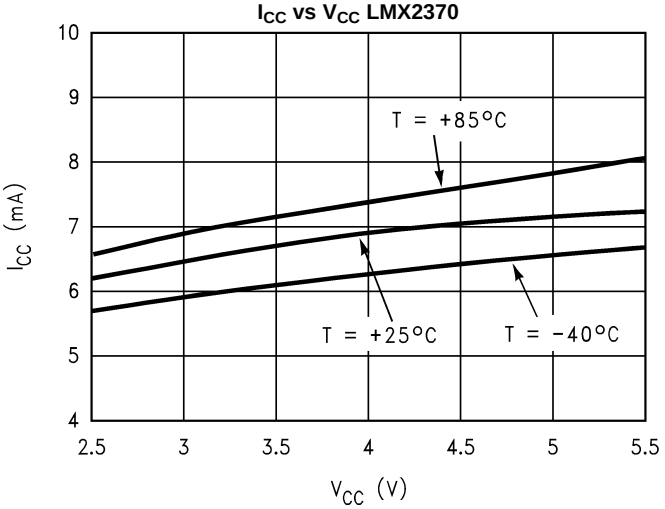


Figure 3.

ICP_o TRI-STATE vs CP_O Voltage

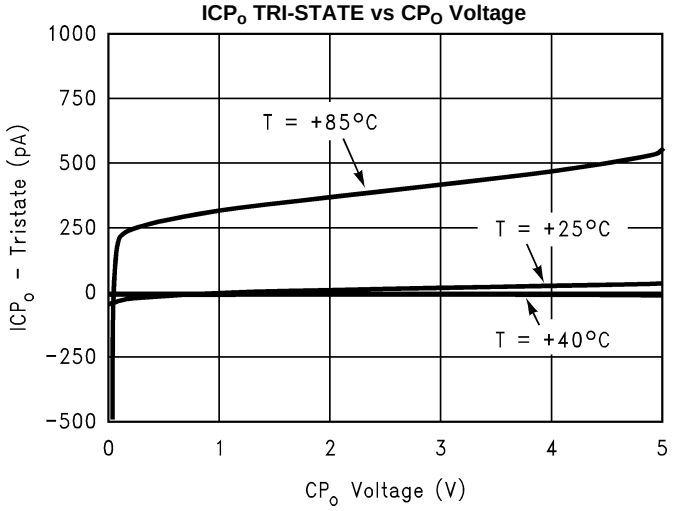


Figure 4.

Charge Pump Current vs CP_O Voltage ICP_O = HIGH

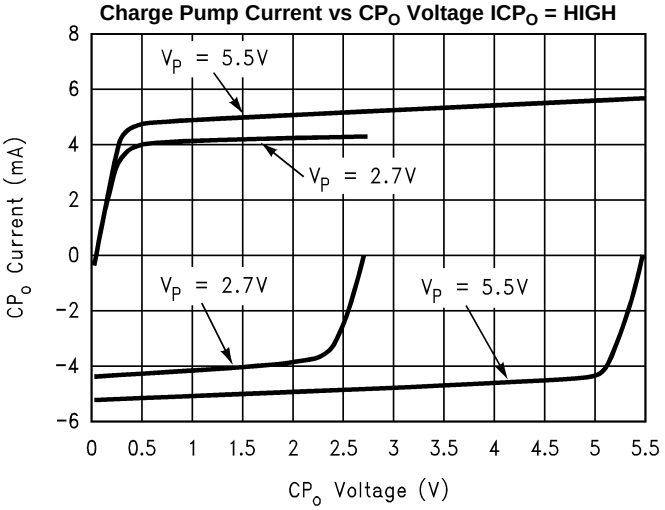


Figure 5.

Charge Pump Current vs CP_O Voltage ICP_O = LOW

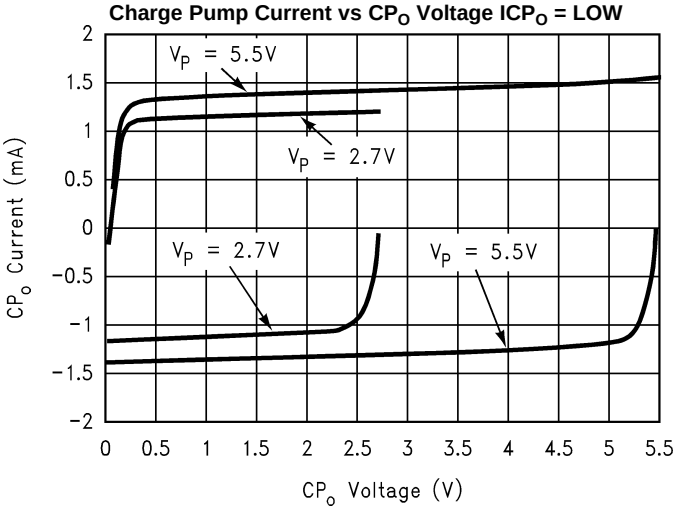


Figure 6.

Sink vs Source 1x-Mode Mismatch (See note (2) under Charge Pump Current Specification Definitions)

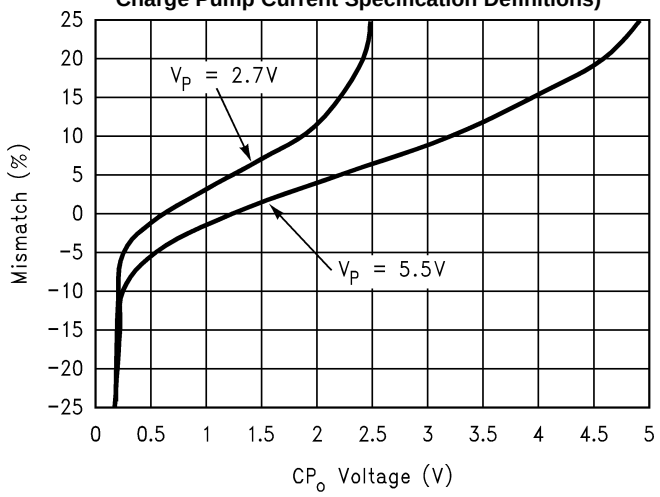


Figure 7.

Sink vs Source 4x-Mode Mismatch (See note (2) under Charge Pump Current Specification Definitions)

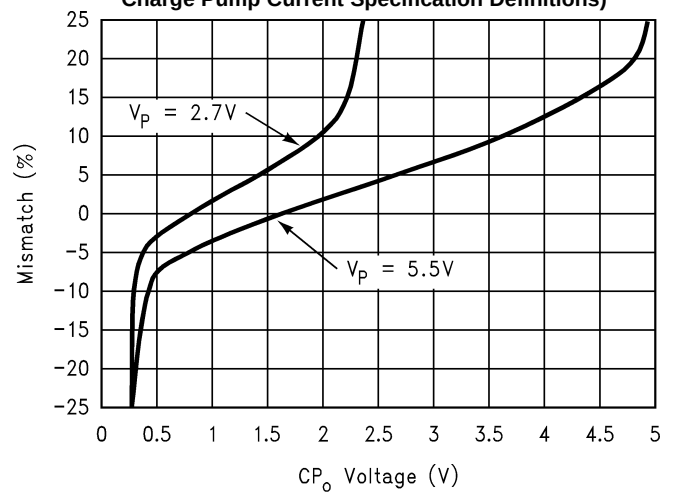
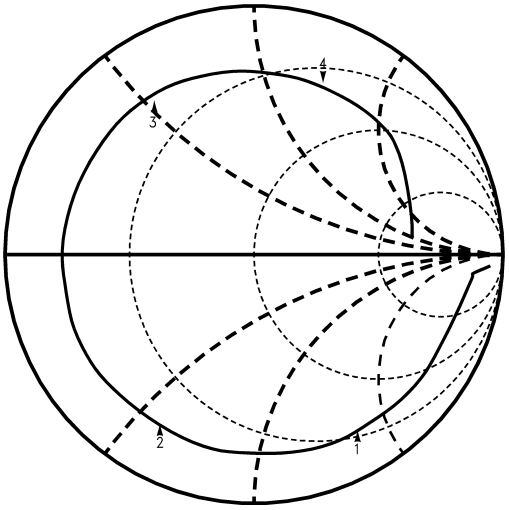


Figure 8.

Typical Performance Characteristics (continued)

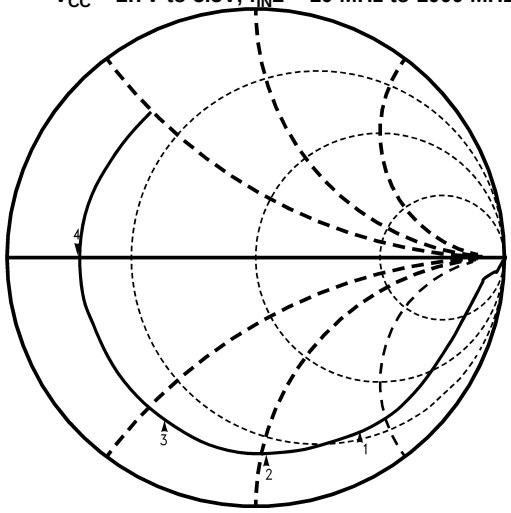
RF Input Impedance, T = 25°C V_{CC} = 2.7V to 5.5V, $f_{IN}1$ = 30 kHz to 3 GHz



Marker 1 = 500 MHz, Real = 21.602, Imag. = −84.160
Marker 2 = 1 GHz, Real = 9.2314, Imag. = −28.793
Marker 3 = 2 GHz, Real = 9.9365, Imag. = 27.582
Marker 4 = 2.5 GHz, Real = 25.867, Imag. = 71.137

Figure 9.

AUX Input Impedance, T = 25°C V_{CC} = 2.7V to 5.5V, $f_{IN}2$ = 10 MHz to 1000 MHz



Marker 1 = 500 MHz, Real = 21.836, Imag. = −85.836
Marker 2 = 750 MHz, Real = 12.824, Imag. = −50.973
Marker 3 = 1 GHz, Real = 9.6270, Imag. = −29.989

Figure 10.

LMX2370 RF Sensitivity vs Frequency

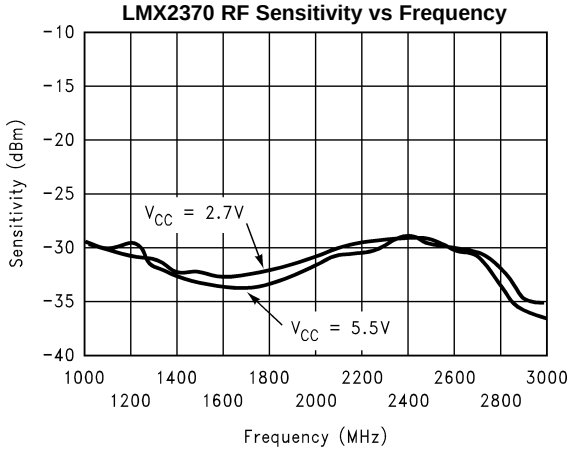


Figure 11.

Auxiliary Input Sensitivity vs Frequency

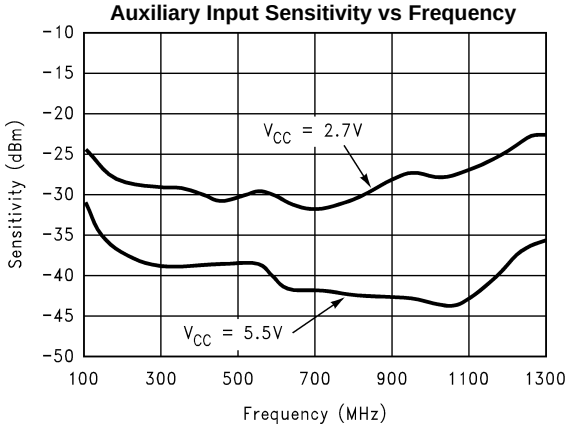


Figure 12.

Oscillator Input Sensitivity vs Frequency

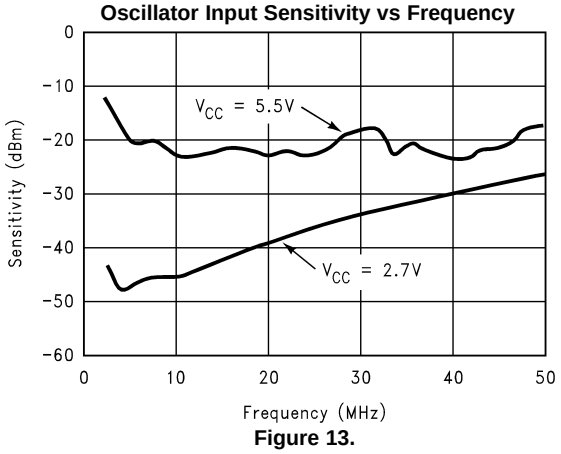


Figure 13.

FUNCTIONAL DESCRIPTION

The basic phase-lock-loop (PLL) configuration consists of a high-stability crystal reference oscillator, a frequency synthesizer such as the Texas Instruments LMX2370, a voltage controlled oscillator (VCO), and a passive loop filter. The frequency synthesizer includes a phase detector, a current mode charge pump, as well as programmable reference [R] and feedback [N] frequency dividers. The VCO frequency is established by dividing the crystal reference signal down via the R-counter to obtain a comparison reference frequency. This reference signal (f_R) is then presented to the input of a phase/frequency detector and compared with the feedback signal (f_N), which is obtained by dividing the VCO frequency down by way of the N-counter. The phase/frequency detector's current source output pumps charge into the loop filter, which then integrates into the VCO's control voltage. The function of the phase/frequency comparator is to adjust the control voltage presented to the VCO until the feedback signal frequency and phase match that of the reference signal. When this “Phase-Locked” condition exists, the VCO frequency will be N times that of the comparison frequency, where N is the integer divide ratio.

REFERENCE OSCILLATOR INPUT

The reference oscillator frequency for the Main and Auxiliary PLLs is provided from the external reference through the OSC_{in} pin. OSC_{in} can operate up to 50 MHz with input sensitivity of 0.5 V_{PP}. The OSC_{in} pin drives both the Main R-counter and the Auxiliary R-counter. The input has a $V_{CC}/2$ input threshold that can be driven from an external CMOS or TTL logic gate. Typically, the OSC_{in} is connected to the output of a crystal oscillator.

REFERENCE DIVIDERS (R-COUNTERS)

The Main and Auxiliary R-counters are both clocked through the oscillator block in common. The maximum frequency is 50 MHz. Both R-counters are CMOS design and 15-bit in length with programmable divider ratio from 2 to 32,767.

PRESCALERS

The complimentary f_{IN} and f_{INB} inputs drive a differential-pair amplifier which feeds to the respective prescaler. The Main PLL complementary $f_{IN}1$ and $f_{IN}1b$ inputs can be driven differentially, or the negative input can be AC coupled to ground through an external capacitor for single ended configuration. The Auxiliary PLL has the complimentary input AC coupled to ground through an internal 10 pF capacitor. The Auxilary PLL complimentary input is not brought out to a pin, and is intended for single ended configuration only. The LMX2370 has a dual modulus prescaler with 2 selectable modulo. A 32/33 or 16/17 prescaler is available on the Main PLL and a 16/17 or 8/9 prescaler is available on the Auxilary PLL. Both the Main and Auxiliary prescalers' outputs drive the subsequent CMOS flip-flop chain comprising the programmable N feedback counters. The proper prescaler value must be chosen to in order not to exceed the maximum CMOS frequency. For $f_{IN} > 1.2$ GHz, the 32/33 prescaler must be selected, similarly for $f_{IN} > 550$ MHz, the prescaler value must be at least 16/17, and for $f_{IN} < 550$ MHz, an 8/9 prescaler value is allowable.

FEEDBACK DIVIDERS (N-COUNTERS)

The Main and Auxiliary N-counters are clocked by the output of Main and Aux prescalers respectively. The N-counter is composed of a 13-bit integer divider and a 5-bit swallow counter. Selecting a 32/33 prescaler provides a minimum continuous divider range from 992 to 262,143 while selecting a 16/17 or 8/9 prescaler value allows for continuous divider values between and 240 to 131,087 and 56 to 65,559 respectively.

PHASE/FREQUENCY DETECTORS

The phase/frequency detectors are driven from their respective N- and R-counter outputs. The maximum frequency at the phase detector inputs is 10 MHz unless limited by the minimum continuous divide ratio of the dual-modulus prescaler. The phase detector output controls the charge pump. The polarity of the pump-up or pump-down control is programmed using **Main_PD_POL** or **Aux_PD_POL**, depending on whether Main or Auxiliary VCO characteristics is positive or negative. The phase detector also receives a feedback signal from the charge pump in order to eliminate dead zone.

CHARGE PUMPS

The phase detector's current source output pumps charge into an external loop filter, which then integrates into the VCO's control voltage. The charge pump steers the charge pump output CP_o to V_P (pump-up) or Ground (pump-down). When locked, CP_o is primarily in a TRI-STATE mode with small corrections. The charge pump output current magnitude can be selected as 1.0 mA or 4.0 mA by programming the **Main_ICP$_o$_4X** or **Aux_ICP$_o$_4X** bits.

MICROWIRE SERIAL INTERFACE

The programmable register set is accessed through the Microwire serial interface. The interface is comprised of three signal pins: clock, data and load enable (LE). The supply for the MICROWIRE circuitry is separate from the rest of the IC to allow for controller voltages down to 1.8V. Serial data is clocked into the 22-bit shift register upon the rising edge of clock. The MSB bit of data shifts first. The last two bits decode the internal register address. On the rising edge of LE, data stored in the shift register is loaded into one of the four latches according to the address bits. The synthesizer can be programmed even in power down state. A complete programming description is followed in Section 2.0.

MULTIFUNCTION OUTPUTS

The LMX2370 FoLD output pin can be configured as the FastLock output or CMOS programmed output, analog lock detects as well as showing the internal block status such as the counter outputs.

Lock Detect Output

An analog lock detect status generated from the phase detector is available on the Fo/LD output pin, if selected. The lock detect output goes high when the charge pump is inactive. It goes low when the charge pump is active during a comparison cycle. The lock detect signal output is an open drain configuration. When a PLL is in power down mode, the respective lock detect output is always high.

FastLock Outputs

When configured as FastLock mode, the current can be increased 4× while maintaining loop stability by synchronously switching a parallel loop filter resistor to ground, resulting in a ~2× change in loop bandwidth. The zero gain crossover point of the open loop gain, or the loop bandwidth is effectively shifted up in frequency by a factor of $\sqrt{4} = 2$ during FastLock mode. For $\omega' = 2\omega$, the phase margin during FastLock will also remain constant. The charge pump current is programmed via MICROWIRE interface. When the charge pump circuit receives an input to deliver 4 times the normal current per unit phase error, an open drain NMOS on chip device (FoLD) switches in a second resistor element to ground. The user calculates the loop filter component values for the normal steady state considerations. The device configuration ensures that as long as a second resistor equal to the primary resistor value is wired in appropriately, the loop will lock faster without any additional stability considerations to account for.

POWER CONTROL

Each PLL is individually power controlled by device power-down (**PWDN**) bits. The **Main_PWDN** and **Aux_PWDN** bits determine the state of power control. Activation of any PLL power-down condition results in the disabling of the respective N-counter and de-biasing of its respective f_{IN} input (to a high impedance state). The R-counter functionality also becomes disabled under this condition.

The reference oscillator input block is powered down when both Main_PWDN and Aux_PWDN bits are asserted. The OSC_{in} pin reverts to a high impedance state when this condition exists. Power down forces the respective charge pump and phase comparator logic to a TRI-STATE condition. During the power down condition, both N- and R-counters are held at reset. Upon powering up, the N-counter resumes counting in “close” alignment with the R-counter. The maximum error is at most one prescaler cycle. The MICROWIRE interface remains active and it is capable of loading and latching in data during all of the power down modes.

Programming Description

MICROWIRE INTERFACE

The LMX237x register set can be accessed through the MICROWIRE interface. A 22-bit shift register is used as a temporary register to indirectly program the on-chip registers. The shift register consists of a 20-bitDATA[19:0] field and a 2-bit ADDRESS[1:0] field as shown below. The address field is used to decode the internal register address. Data is clocked into the shift register in the direction from MSB to LSB, when the CLOCK signal goes high. On the rising edge of Load Enable (LE) signal, data stored in the shift register is loaded into the addressed latch.

MSB					LSB
DATA[19:0]			ADDRESS[1:0]		
21		2	1		0

Registers' Address Map

When Load Enable (LE) is transitioned high, data is transferred from the 22-bit shift register into the appropriate latch depending on the state of the ADDRESS[1:0] bits. A multiplexing circuit decodes these address bits and writes the data field to the corresponding internal register.

ADDRESS[1:0]		REGISTER
FIELD		ADDRESSED
0	0	Aux_R Register
0	1	Aux_N Register
1	0	Main_R Register
1	1	Main_N Register

Table 1. Registers' Truth Table

	Most Significant Bit						SHIFT REGISTER BIT LOCATION											Least Significant Bit				
	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Data Field																				*Address Field*	
Aux_R	FoLD 1	FoLD 0	Aux_CP$_{o}$_TRI	Aux_CP$_{o}$_4X	Aux_PD_POL	Aux_R_CNTR[14:0]															0	0
	Aux_R19	Aux_R18	Aux_R17	Aux_R16	Aux_R15	Aux_R14	Aux_R13	Aux_R12	Aux_R11	Aux_R10	Aux_R9	Aux_R8	Aux_R7	Aux_R6	Aux_R5	Aux_R4	Aux_R3	Aux_R2	Aux_R1	Aux_R0		
Aux_N	Aux_PWDN	P_Aux	Aux_B_CNTR[12:0]													Aux_A_CNTR[4:0]					0	1
	Aux_N19	Aux_N18	Aux_N17	Aux_N16	Aux_N15	Aux_N14	Aux_N13	Aux_N12	Aux_N11	Aux_N10	Aux_N9	Aux_N8	Aux_N7	Aux_N6	Aux_N5	Aux_N4	Aux_N3	Aux_N2	Aux_N1	Aux_N0		
Main_R	FoLD 3	FoLD 2	Main_CP$_{o}$_TRI	Main_CP$_{o}$_4X	Main_PD_POL	Main_R_CNTR[14:0]															1	0
	Main_R19	Main_R18	Main_R17	Main_R16	Main_R15	Main_R14	Main_R13	Main_R12	Main_R11	Main_R10	Main_R9	Main_R8	Main_R7	Main_R6	Main_R5	Main_R4	Main_R3	Main_R2	Main_R1	Main_R0		
Main_N	Main_PWDN	P_Main	Main_B_CNTR[12:0]													Main_A_CNTR[4:0]					1	1
	Main_N19	Main_N18	Main_N17	Main_N16	Main_N15	Main_N14	Main_N13	Main_N12	Main_N11	Main_N10	Main_N9	Main_N8	Main_N7	Main_N6	Main_N5	Main_N4	Main_N3	Main_N2	Main_N1	Main_N0		

PROGRAMMABLE REFERENCE DIVIDERS (Main and Aux R Counters)

Aux_R Register

If the ADDRESS[1:0] field is set to 0 0, data is transferred from the 22-bit shift register into the Aux_R register when Load Enable (LE) signal goes high. The Aux_R register sets the Aux PLL's 15-bit R-counter divide ratio and various programmable modes. The divide ratio is put into the Aux_R_CNTR[14:0] field. The divider ratio must be ≥ 2. For the description of bits Aux_R15–Aux_R19 see PROGRAMMABLE MODES.

	Most Significant Bit						SHIFT REGISTER BIT LOCATION											Least Significant Bit				
	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Data Field																				*Address Field*	
Aux_R	FoLD 1	FoLD 0	Aux_CP$_o$_TRI	Aux_CP$_o$_4X	Aux_PD_POL	Aux_R_CNTR[14:0]															0	0
	Aux_R19	Aux_R18	Aux_R17	Aux_R16	Aux_R15	Aux_R14	Aux_R13	Aux_R12	Aux_R11	Aux_R10	Aux_R9	Aux_R8	Aux_R7	Aux_R6	Aux_R5	Aux_R4	Aux_R3	Aux_R2	Aux_R1	Aux_R0		

Main_R Register

If the ADDRESS[1:0] field is set to 1 0, data is transferred from the 22-bit shift register into the Main_R register which sets the Main PLL's 15-bit R-counter divide ratio when Load Enable (LE) signal goes high. The divide ratio is put into the Main_R_CNTR[14:0] field. The divider ratio must be ≥ 2. For the description of bits Main_R15–Main_R19 see PROGRAMMABLE MODES.

	Most Significant Bit						SHIFT REGISTER BIT LOCATION											Least Significant Bit				
	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Data Field																				*Address Field*	
Main_R	FoLD 3	FoLD 2	Main_CP$_o$_TRI	Main_CP$_o$_4X	Main_PD_POL	Main_R_CNTR[14:0]															1	0
	Main_R19	Main_R18	Main_R17	Main_R16	Main_R15	Main_R14	Main_R13	Main_R12	Main_R11	Main_R10	Main_R9	Main_R8	Main_R7	Main_R6	Main_R5	Main_R4	Main_R3	Main_R2	Main_R1	Main_R0		

Reference Divide Ratio (Main and Auxiliary R-Counters)

If the ADDRESS[1:0] field is set to 0 0 or 1 0 (00 for Aux and 10 for Main) data is transferred MSB first from the 22-bit shift register into a latch which sets the respective 15-bit R-counter. Serial data format is shown below.

	Main_R_CNTR[14:0] or Aux_R_CNTR[14:0]														
Divide Ratio	**R14**	**R13**	**R12**	**R11**	**R10**	**R9**	**R8**	**R7**	**R6**	**R5**	**R4**	**R3**	**R2**	**R1**	**R0**
2	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
3	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
32,767	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

PROGRAMMABLE FEEDBACK [N] DIVIDERS

Aux_N Register

If the ADDRESS[1:0] field is set to 0 1, data is transferred from the 22-bit shift register into the Aux_N register which sets the Auxiliary PLL's 18-bit N-counter, prescaler value and power-down bit. The 18-bit N-counter consists of a 5-bit swallow counter, Aux_A_CNTR[4:0], and a 13-bit programmable counter, Aux_B_CNTR[12:0]. Serial data format is shown below.

	Most Significant Bit						SHIFT REGISTER BIT LOCATION											Least Significant Bit				
	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Data Field																				Address Field	
Aux_N	Aux_PWDN	P_Aux	Aux_B_CNTR[12:0]													Aux_A_CNTR[4:0]					0	1
	Aux_N19	Aux_N18	Aux_N17	Aux_N16	Aux_N15	Aux_N14	Aux_N13	Aux_N12	Aux_N11	Aux_N10	Aux_N9	Aux_N8	Aux_N7	Aux_N6	Aux_N5	Aux_N4	Aux_N3	Aux_N2	Aux_N1	Aux_N0		

Main_N Register

If the ADDRESS[1:0] field is set to 1 1, data is transferred from the 22-bit shift register into the Main_N register which sets the Main PLL's 18-bit N-counter, prescaler value and power-down bit. The 18-bit N-counter consists of a 5-bit swallow counter, Main_A_CNTR[4:0], and a 13-bit programmable counter, Main_B_CNTR[12:0]. Serial data format is shown below.

	Most Significant Bit						SHIFT REGISTER BIT LOCATION											Least Significant Bit				
	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Data Field																				Address Field	
Main_N	Main_PWDN	P_Main	Main_B_CNTR[12:0]													Main_A_CNTR[4:0]					1	1
	Main_N19	Main_N18	Main_N17	Main_N16	Main_N15	Main_N14	Main_N13	Main_N12	Main_N11	Main_N10	Main_N9	Main_N8	Main_N7	Main_N6	Main_N5	Main_N4	Main_N3	Main_N2	Main_N1	Main_N0		

Table 2. Feedback Divide Ratio (Main B Counter, Auxiliary B Counter)

	Main_B_CNTR[12:0] or Aux_B_CNTR[12:0]												
Divide Ratio	N17	N16	N15	N14	N13	N12	N11	N10	N9	N8	N7	N6	N5
3	0	0	0	0	0	0	0	0	0	0	0	1	1
4	0	0	0	0	0	0	0	0	0	0	1	0	1
•	•	•	•	•	•	•	•	•	•	•	•	•	•
8,191	1	1	1	1	1	1	1	1	1	1	1	1	1

Swallow Counter Divide Ratio (Main A Counter, Auxiliary A Counter)

	Main_A_CNTR[4:0] or Aux_A_CNTR[4:0]				
Divide Ratio	Main_N4	Main_N3	Main_N2	Main_N1	Main_N0
0	0	0	0	0	0
1	0	0	0	0	1
•	•	•	•	•	•
31	1	1	1	1	1

PLL Prescaler Select (P_Aux, P_Main)

The LMX2370 contains two dual modulus prescalers. A 32/33 or a 16/17 prescaler can be selected for the Main synthesizer and a 16/17 or 8/9 prescaler can be selected for the Aux synthesizer.

	Prescaler Value	
P_Main, (Main_N18) or P_Aux (Aux_N18)	2.5 GHz PLL	1.2 GHz PLL
0	16/17	8/9
1	32/33	16/17

	Allowable Prescaler Values	
PLL Input Frequency	2.5 GHz PLL	1.2 GHz PLL
f_{IN} > 1.2 GHz	32/33	NA
550 < f_{IN} < 1200 MHz	16/17 or 32/33	16/17

	Allowable Prescaler Values	
PLL Input Frequency	**2.5 GHz PLL**	**1.2 GHz PLL**
f_{IN} < 550 MHz	16/17 or 32/33	8/9 or 16/17

Pulse Swallow Function

$f_{VCO} = [(P \times B) + A] \times f_{OSC}/R$

f_{VCO}: Output frequency of external voltage controlled oscillator (VCO)

B: Preset divide ratio of binary 13-bit programmable counter (3 to 8191)

A: Preset divide ratio of binary 5-bit swallow counter
0 ≤ A ≤ 31 {P=32}
0 ≤ A ≤ 15 {P=16}
0 ≤ A ≤ 7 {P=8}
A ≤ B

f_{osc}: Output frequency of the external reference frequency oscillator

R: Preset divide ratio of binary 15-bit programmable reference counter (3 to 32767)

P: Preset modulus of dual modulus prescaler (P = 8, 16, or 32)

PLL Power Down Control (Aux_PWDN, Main_PWDN)

The **Aux_PWDN (Aux_N19)** and **Main_PWDN (Main_N19**) bits are used to power down either the Main or Auxiliary PLL's charge pump portion, or the entire PLL block depending on the setting of the respective charge pump TRI-STATE bit (Aux_CP_o_TRI or Main_CP_o_TRI) in the R_CNTR register. The power-down mechanism is described below. The R and N counters for each respective PLL are disabled and held at reset during the synchronous and asynchronous power down modes. This will allow a smooth acquisition of the Main RF signal when the oscillator input buffer is still active (Auxiliary loop powered up) and vice versa. Upon powering up, both R and N counters will start at the “zero” state, and the relationship between R and N will not be random.

Synchronous Power Down Mode

One of the PLL loops can be synchronously powered down by first setting the respective loop's TRI-STATE mode bit LOW (R17 = 0) and then asserting its power down mode bit (N19 = 1). The power down function is gated by the charge pump. Once the power down program bits Aux_PWDN (Aux_N19) and Main_PWDN (Main_N19) and TRI-STATE bits Aux_CP_o_TRI (Aux_R17) or Main_CP_o_TRI (Main_R17) are loaded, the part will go into power down mode upon the completion of a charge pump pulse event.

Asynchronous Power Down Mode

One of the PLL loops can be asynchronously powered down by first setting the respective loop's TRI-STATE mode bit HI (R17 = 1) and then asserting its power down mode bit (N19 = 1). The power down function is NOT gated by the charge pump. Once the power down program bits Aux_PWDN (Aux_N19) and Main_PWDN (Main_N19) and its respective TRI-STATE bit Aux_CP_o_TRI (Aux_R17) or Main_CP_o_TRI (Main_R17) are loaded, the part will go into power down mode immediately.

Power Down Mode Table

Main PLL	Auxiliary PLL	Main Counters	Auxiliary Counters	OSC_{in} Buffer
Active	Active	ON	ON	ON
Active	Powered Down	ON	OFF	ON
Powered Down	Active	OFF	ON	ON
Powered Down	Powered Down	OFF	OFF	OFF

PROGRAMMABLE MODES

Several modes of operation can be programmed with bits R15–R19 including the phase detector polarity, charge pump magnitude, charge pump TRI-STATE and the output of the Fo/LD pin. The programmable modes are shown in Table 1. Truth table for the programmable modes and Fo/LD output are shown in Table 2 and Table 3.

Programmable Modes Table

R19	R18	R17	R16	R15	Address[1:0]
f_{OUT}/Lock Detect		Charge Pump TRI-STATE	Charge Pump Magnitude	Phase Detector Polarity	
FoLD 1	FoLD 0	Aux_CP_o_TRI	Aux_CP_o_4X	Aux_PD_POL	0 0
FoLD 3	FoLD 2	Main_CP_o_TRI	Main_CP_o_4X	Main_PD_POL	1 0

Mode Select Truth Table

	CP_o_TRI (1)	CP_o_4X (2)	PD_POL (3)
0	Normal Operation	1X Current	LOW
1	TRI-STATE	4X Current	HIGH

(1) Both synchronous and asynchronous power down modes are available with the LMX237x family to be able to adapt to different types of applications. The MICROWIRE control register remains active and capable of loading and latching in data during all of the powerdown modes.
(2) ICP_o (charge pump current magnitude) is dependent on Vp. The ICP_o LOW current state = 1/4 x ICP_o HIGH current.
(3) See Phase Detector Polarity (Aux_PD_POL, Main_PD_POL).

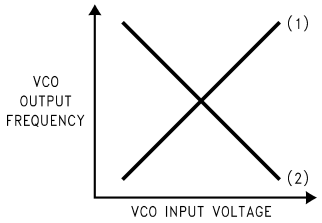
Phase Detector Polarity (Aux_PD_POL, Main_PD_POL)

Depending upon VCO characteristics, the Aux_PD_POL (Aux_R15) and Main_PD_POL (Main_R15) bits should be set accordingly:

When VCO characteristics are positive like (1), R15 should be set HIGH;

When VCO characteristics are negative like (2), R15 should be set LOW.

Figure 14. VCO CHARACTERISTICS



The FoLD Output Truth Table

Main R[18]	Aux R[18]	Main R[19]	Aux R[19]	Fo/LD Output State
0	0	0	0	Disabled
0	1	0	0	Aux Lock Detect (1)
1	0	0	0	Main Lock Detect (1)
1	1	0	0	Main/Aux Lock Detect (1)
X	0	0	1	Aux Reference Divider Output
X	0	1	0	Main Reference Divider Output
X	1	0	1	Aux Programmable Divider Output
X	1	1	0	Main Programmable Divider Output
0	0	1	1	FastLock Output. Open Drain Output (2)

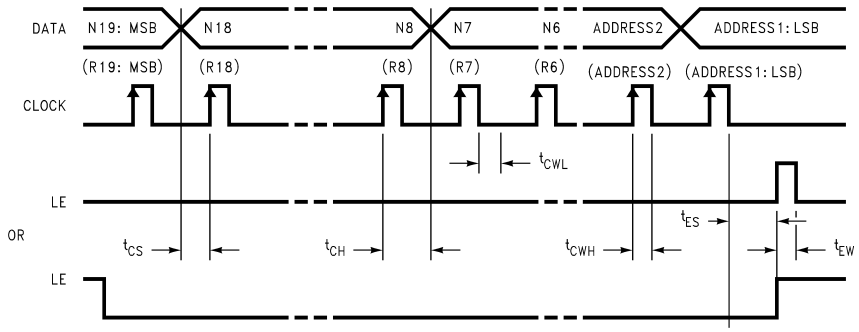
(1) Open drain lock detect output is provided to indicate when the VCO frequency is in “lock”. When the loop is locked and a lock detect mode is selected, the pin is HIGH, with narrow pulses LOW. In the Main/Aux lock detect mode a locked condition is indicated when Main and Aux are both locked.
(2) The FastLock mode utilizes the FoLD output pin to switch a second loop filter damping resistor to ground during FastLock operation. Activation of FastLock occurs whenever the Main loop's ICP_o magnitude bit R[16] is selected HI while the R[18] and R[19] mode bits are set.

Main R[18]	Aux R[18]	Main R[19]	Aux R[19]	Fo/LD Output State
0	1	1	1	Reset Aux R and N Counters and TRI-STATE Aux Charge Pump (3)
1	0	1	1	Reset Main R and N Counters and TRI-STATE Main Charge Pump (3)
1	1	1	1	Reset All Four Counters and TRI-STATE both Charge Pumps (3)

(3) Aux and Main PLLs can be reset independently from each other by using the R[18] and R[19] bits. The Aux Counter Reset mode resets Aux PLL's R and N counters and brings Aux charge pump output to TRI-STATE condition. The Main Counter Reset mode resets Main PLL's R and N counters and brings Main charge pump output to a TRI-STATE condition. The Aux and Main Counter Reset modes reset all counters and bring both charge pump outputs to a TRI-STATE condition. Upon removal of the Reset bits, the N counter resumes counting in “close” alignment with the R counter. (The maximum error is one prescaler cycle.)

SERIAL DATA INPUT TIMING

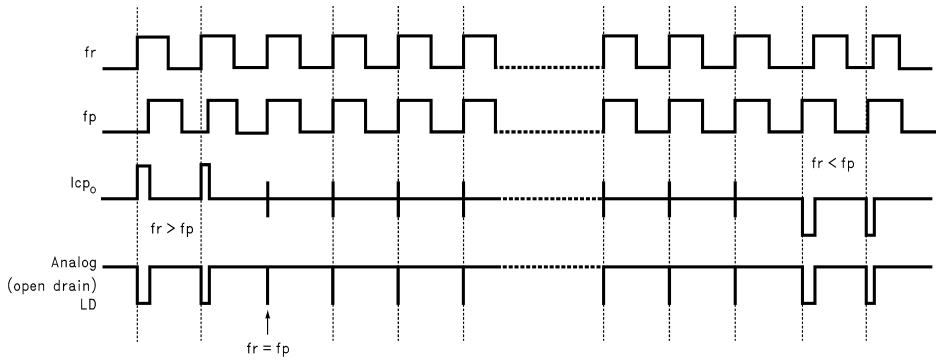
Figure 15. Serial Data Input Timing



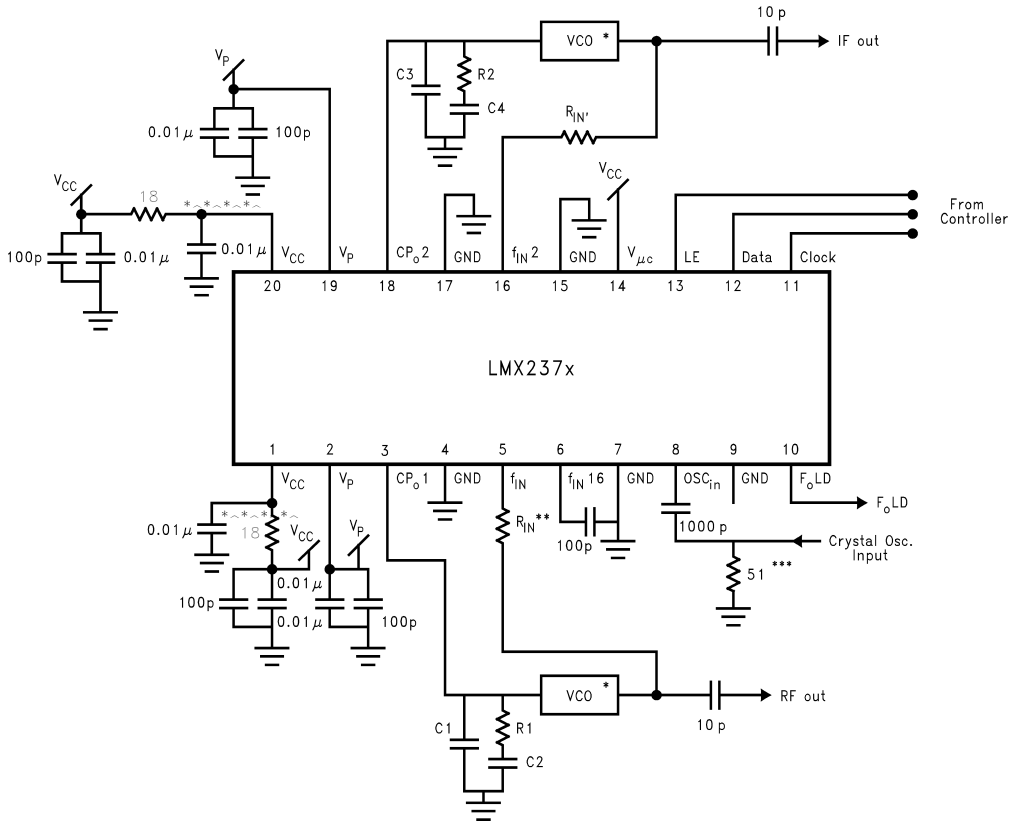
NOTES: Parenthesis data indicates programmable reference divider data.
Data shifted into register on clock rising edge.
Data is shifted in MSB first.
TEST CONDITIONS: The Serial Data Input Timing is tested using a symmetrical waveform around $V_{CC}/2$. The test waveform has an edge rate of 0.6 V/ns with amplitudes of 2.2V @ V_{CC} = 2.7V and 2.6V @ V_{CC} = 5.5V.

TYPICAL LOCK DETECT TIMING

Figure 16. Typical Lock Detect Timing



Typical Application Example



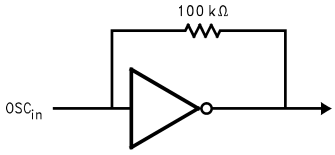
Operational Notes:

***** VCO is assumed AC coupled.

****** R_{IN} increases impedance so that VCO output power is provided to the load rather than the PLL. Typical values are 10Ω to 200Ω depending on the VCO power level. f_{IN} RF impedance ranges from 40Ω to 100Ω. f_{IN} IF impedances are higher.

******* 50Ω termination is often used on test boards to allow use of external reference oscillator. For most typical products a CMOS clock is used and no terminating resistor is required. OSC_{in} may be AC or DC coupled. AC coupling is recommended because the input circuit provides its own bias. (See *Figure* below)

******** Adding RC filters to the V_{CC} line is recommended to reduce loop-to-loop noise coupling.



Proper use of grounds and bypass capacitors is essential to achieve a high level of performance. Crosstalk between pins can be reduced by careful board layout.
This is an electrostatic sensitive device. It should be handled only at static free work stations.

Application Information

A block diagram of the basic phase locked loop is shown in Figure 17.

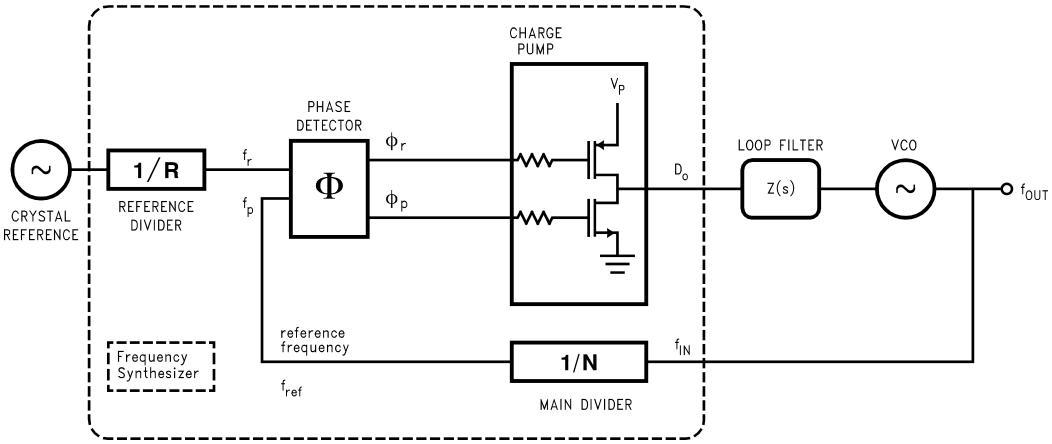


Figure 17. Basic Charge Pump Phase Locked Loop

LOOP GAIN EQUATIONS

A linear control system model of the phase feedback for a PLL in the locked state is shown in Figure 18. The open loop gain is the product of the phase comparator gain (Kφ), the VCO gain (K_{VCO}/s), and the loop filter gain Z(s) divided by the gain of the feedback counter modulus (N). The passive loop filter configuration used is displayed in Figure 19, while the complex impedance of the filter is given in Equation 2.

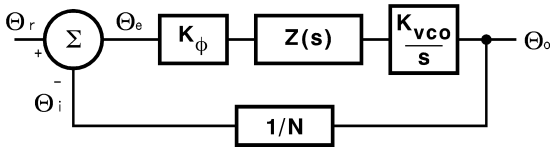


Figure 18. PLL Linear Model

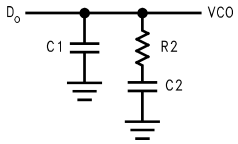


Figure 19. Passive Loop Filter

$$\text{Open loop gain} = H(s)\,G(s) = \frac{\Theta_i}{\Theta_e} = \frac{K_\phi Z(s) K_{VCO}}{Ns} \tag{1}$$

$$Z(s) = \frac{s(C2 \bullet R2) + 1}{s^2(C1 \bullet C2 \bullet R2) + sC1 + sC2} \tag{2}$$

The time constants which determine the pole and zero frequencies of the filter transfer function can be defined as

$$T1 = R2 \bullet \frac{C1 \bullet C2}{C1 + C2} \tag{3}$$

and

$$T2 = R2 \bullet C2 \tag{4}$$

The 3rd order PLL Open Loop Gain can be calculated in terms of frequency, ω, the filter time constants T1 and T2, and the design constants K_ϕ, K_{VCO}, and N.

$$G(s) \bullet H(s)\,|_{s = j \bullet \omega} = \frac{-K_\phi \bullet K_{VCO}\,(1 + j\omega \bullet T2)}{\omega^2 C1 \bullet N(1 + J\omega \bullet T1)} \bullet \frac{T1}{T2} \tag{5}$$

From Equation 3 we can see that the phase term will be dependent on the single pole and zero such that the phase margin is determined in Equation 6.

$$\varphi(\omega) = \tan^{-1}(\omega \bullet T2) - \tan^{-1}(\omega \bullet T1) + 180° \quad (6)$$

A plot of the magnitude and phase of G(s)H(s) for a stable loop, is shown in Figure 20 with a solid trace. The parameter φ_p shows the amount of phase margin that exists at the point the gain drops below zero (the cutoff frequency wp of the loop). In a critically damped system, the amount of phase margin would be approximately 45 degrees.

If we were now to redefine the cut off frequency, wp', as double the frequency which gave us our original loop bandwidth, wp, the loop response time would be approximately halved. Because the filter attenuation at the comparison frequency also diminishes, the spurs would have increased by approximately 6 dB. In the proposed Fastlock scheme, the higher spur levels and wider loop filter conditions would exist only during the initial lock-on phase—just long enough to reap the benefits of locking faster. The objective would be to open up the loop bandwidth but not introduce any additional complications or compromises related to our original design criteria. We would ideally like to momentarily shift the curve of Figure 20 over to a different cutoff frequency, illustrated by the dotted line, without affecting the relative open loop gain and phase relationships. To maintain the same gain/phase relationship at twice the original cutoff frequency, other terms in the gain and phase Equation 5 Equation 6 will have to compensate by the corresponding “1/w” or “$1/w^2$” factor. Examination of Equation 3 Equation 4 Equation 6 indicates the damping resistor variable R2 could be chosen to compensate the “w” terms for the phase margin. This implies that another resistor of equal value to R2 will need to be switched in parallel with R2 during the initial lock period. We must also ensure that the magnitude of the open loop gain, H(s)G(s) is equal to zero at wp' = 2wp. K_{VCO}, Kφ, N, or the net product of these terms can be changed by a factor of 4, to counteract the w^2 term present in the denominator of Equation 3 Equation 4. The Kφ term was chosen to complete the transformation because it can readily be switch between 1X and 4X values. This is accomplished by increasing the charge pump output current from 1 mA in the standard mode to 4 mA in Fastlock.

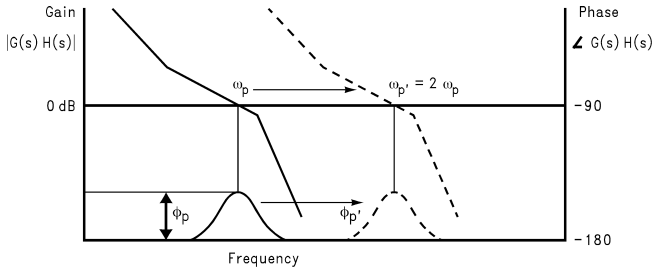


Figure 20. Open Loop Response Bode Plot

FASTLOCK CIRCUIT IMPLEMENTATION

A diagram of the Fastlock scheme as implemented in Texas Instruments LMX233xA PLL is shown in Figure 21. When a new frequency is loaded, and the RF Icp_o bit is set high the charge pump circuit receives an input to deliver 4 times the normal current per unit phase error while an open drain NMOS on chip device switches in a second R2 resistor element to ground. The user calculates the loop filter component values for the normal steady state considerations. The device configuration ensures that as long as a second identical damping resistor is wired in appropriately, the loop will lock faster without any additional stability considerations to account for. Once locked on the correct frequency, the user can return the PLL to standard low noise operation by sending a MICROWIRE instruction with the RF Icp_o bit set low. This transition does not affect the charge on the loop filter capacitors and is enacted synchronous with the charge pump output. This creates a nearly seamless change between Fastlock and standard mode.

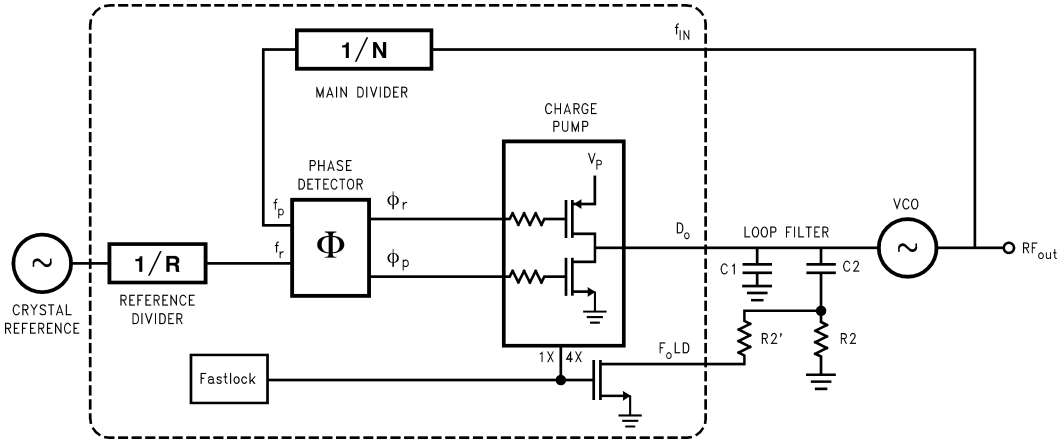


Figure 21. Fastlock PLL Architecture

REVISION HISTORY

Changes from Revision C (March 2013) to Revision D	Page
• Changed layout of National Data Sheet to TI format	23

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