LP38691-ADJ
LP38693-ADJ 500mA Low Dropout CMOS Linear Regulators with Adjustable Output
Stable with Ceramic Output Capacitors

Check for Samples: LP38691-ADJ, LP38693-ADJ

FEATURES

- **All LLP options are available as AEC-Q100 Grade 1**
- **Output voltage range of 1.25V - 9V**
- **2.0% adjust pin voltage accuracy (25°C)**
- **Low dropout voltage: 250mV @ 500mA (typ, 5V out)**
- **Wide input voltage range (2.7V to 10V)**
- **Precision (trimmed) bandgap reference**
- **Guaranteed specs for -40°C to +125°C**
- **1μA off-state quiescent current**
- **Thermal overload protection**
- **Foldback current limiting**
- **SOT-223 and 6-Lead LLP packages**
- **Enable pin (LP38693-ADJ)**

APPLICATIONS

- **Hard Disk Drives**
- **Notebook Computers**
- **Battery Powered Devices**
- **Portable Instrumentation**

DESCRIPTION

The LP38691/3-ADJ low dropout CMOS linear regulators provide 2.0% precision reference voltage, extremely low dropout voltage (250mV @ 500mA load current, V_{OUT} = 5V) and excellent AC performance utilizing ultra low ESR ceramic output capacitors.

The low thermal resistance of the LLP and SOT-223 packages allow the full operating current to be used even in high ambient temperature environments.

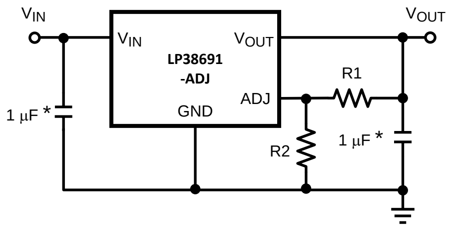
The use of a PMOS power transistor means that no DC base drive current is required to bias it allowing ground pin current to remain below 100 µA regardless of load current, input voltage, or operating temperature.

Dropout Voltage: 250 mV (typ) @ 500mA (typ. 5V out).

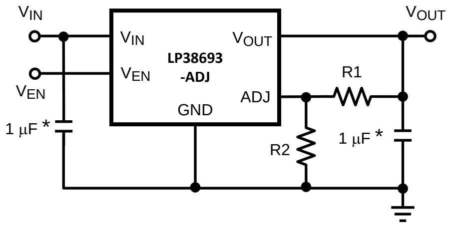
Ground Pin Current: 55 µA (typ) at full load.

Adjust Pin Voltage: 2.0% (25°C) accuracy.

Typical Application Circuits



*Minimum value required for stability.



*Minimum value required for stability.

$$V_{OUT} = V_{ADJ} \times (1 + R1/R2) \quad (1)$$

Connection Diagram

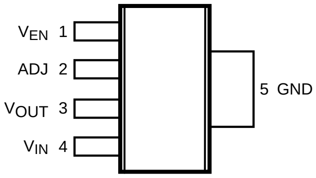


Figure 1. SOT-223, Top View
LP38693MP-ADJ

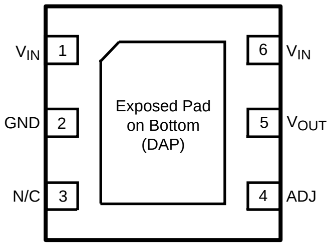


Figure 2. 6-Lead LLP, Top View
LP38691SD-ADJ

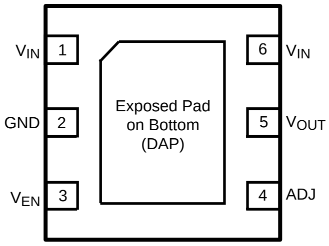


Figure 3. 6-Lead LLP, Top View
LP38693SD-ADJ

Pin Functions

Pin Descriptions

Pin	Description
V_{IN}	This is the input supply voltage to the regulator. For LLP package devices, both V_{IN} pins must be tied together for full current operation (250mA maximum per pin).
GND	Circuit ground for the regulator. For the SOT-223 package this is thermally connected to the die and functions as a heat sink when the soldered down to a large copper plane.
V_{OUT}	Regulated output voltage.
V_{EN}	The enable pin allows the part to be turned ON and OFF by pulling this pin high or low.
ADJ	The adjust pin is used to set the regulated output voltage by connecting it to the external resistors R1 and R2 (see Typical Application Circuit).
DAP	LLP Only - The DAP (Exposed Pad) functions as a thermal connection when soldered to a copper plane. See LLP MOUNTING section in Application Hints for more information.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1)

Storage Temperature Range	−65°C to +150°C
Lead Temp. (Soldering, 5 seconds)	260°C
ESD Rating (2)	2 kV
Power Dissipation (3)	Internally Limited
V(max) All pins (with respect to GND)	-0.3V to 12V
I_{OUT}	Internally Limited
Junction Temperature	−40°C to +150°C

(1) Absolute maximum ratings indicate limits beyond which damage to the component may occur. Operating ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications, see Electrical Characteristics. Specifications do not apply when operating the device outside of its rated operating conditions.

(2) ESD is tested using the human body model which is a 100pF capacitor discharged through a 1.5k resistor into each pin.

(3) At elevated temperatures, device power dissipation must be derated based on package thermal resistance and heatsink values (if a heatsink is used). The junction-to-ambient thermal resistance (θ_{J-A}) for the SOT-223 is approximately 125 °C/W for a PC board mounting with the device soldered down to minimum copper area (less than 0.1 square inch). If one square inch of copper is used as a heat dissipator for the SOT-223, the θ_{J-A} drops to approximately 70 °C/W. The θ_{J-A} values for the LLP package are also dependent on trace area, copper thickness, and the number of thermal vias used (refer to application note AN-1187 and the LLP MOUNTING section in this datasheet). If power dissipation causes the junction temperature to exceed specified limits, the device will go into thermal shutdown.

Operating Ratings

V_{IN} Supply Voltage	2.7V to 10V
Operating Junction Temperature Range	−40°C to +125°C

Electrical Characteristics

Limits in standard typeface are for T_J = 25°C, and limits in **boldface type** apply over the full operating temperature range. Unless otherwise specified: $V_{IN} = V_{OUT} + 1V$, $C_{IN} = C_{OUT} = 10\ \mu F$, I_{LOAD} = 10mA. Min/Max limits are guaranteed through testing, statistical correlation, or design.

Symbol	Parameter	Conditions	Min	Typ (1)	Max	Units
V_{ADJ}	ADJ Pin Voltage	V_{IN} = 2.7V	1.225	1.25	1.275	V
		$3.2V \le V_{IN} \le 10V$ $100\ \mu A < I_L < 0.5A$	**1.200**	1.25	**1.300**	
$\Delta V_O/\Delta V_{IN}$	Output Voltage Line Regulation (2)	$V_O + 0.5V \le V_{IN} \le 10V$ I_L = 25mA		0.03	**0.1**	%/V
$\Delta V_O/\Delta I_L$	Output Voltage Load Regulation (3)	$1\ mA < I_L < 0.5A$ $V_{IN} = V_O + 1V$		1.8	**5**	%/A
$V_{IN} - V_O$	Dropout Voltage (4)	(V_O = 2.5V) I_L = 0.1A I_L = 0.5A		80 430	**145** **725**	mV
		(V_O = 3.3V) I_L = 0.1A I_L = 0.5A		65 330	**110** **550**	
		(V_O = 5V) I_L = 0.1A I_L = 0.5A		45 250	**100** **450**	
I_Q	Quiescent Current	$V_{IN} \le 10V$, I_L = 100 µA - 0.5A		55	**100**	µA
		$V_{EN} \le 0.4V$, (LP38693-ADJ Only)		0.001	1	
I_L(MIN)	Minimum Load Current	$V_{IN} - V_O \le 4V$			**100**	
I_{FB}	Foldback Current Limit	$V_{IN} - V_O > 5V$		350		mA
		$V_{IN} - V_O < 4V$		850		
PSRR	Ripple Rejection	$V_{IN} = V_O + 2V$(DC), with 1V(p-p) / 120Hz Ripple		55		dB
T_{SD}	Thermal Shutdown Activation (Junction Temp)			160		°C
T_{SD} (HYST)	Thermal Shutdown Hysteresis (Junction Temp)			10		
I_{ADJ}	ADJ Input Leakage Current	V_{ADJ} = 0 - 1.5V V_{IN} = 10V	-100	0.01	100	nA
e_n	Output Noise	BW = 10Hz to 10kHz V_O = 3.3V		0.7		$\mu V/\sqrt{Hz}$
V_O (LEAK)	Output Leakage Current	$V_O = V_O(NOM) + 1V$ @ V_{IN} = 10V		0.5	2	µA
V_{EN}	Enable Voltage (LP38693-ADJ Only)	Output = OFF			**0.4**	V
		Output = ON, V_{IN} = 4V	**1.8**			
		Output = ON, V_{IN} = 6V	**3.0**			
		Output = ON, V_{IN} = 10V	**4.0**			
I_{EN}	Enable Pin Leakage (LP38693-ADJ Only)	V_{EN} = 0V or 10V, V_{IN} = 10V	-1	0.001	1	µA

(1) Typical numbers represent the most likely parametric norm for 25°C operation.
(2) Output voltage line regulation is defined as the change in output voltage from nominal value resulting from a change in input voltage.
(3) Output voltage load regulation is defined as the change in output voltage from nominal value as the load current increases from 1mA to full load.
(4) Dropout voltage is defined as the minimum input to output differential required to maintain the output within 100mV of nominal value.

Block Diagrams

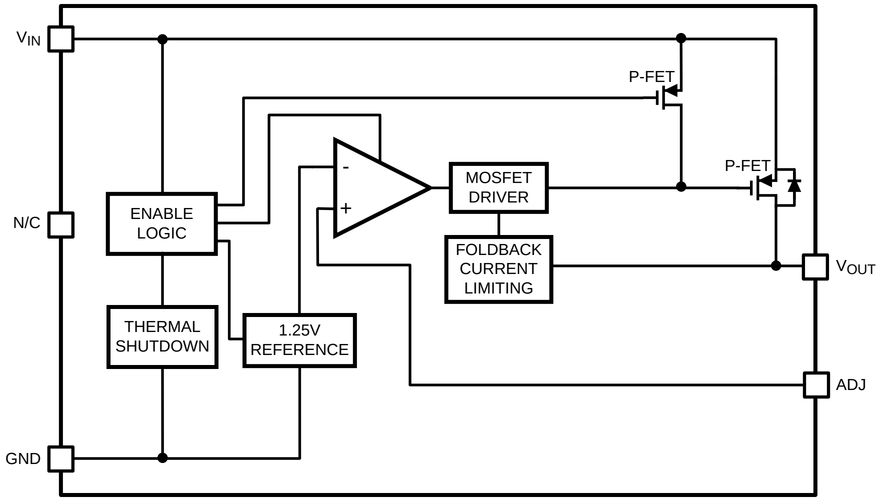


Figure 4. LP38691-ADJ Functional Diagram (LLP)

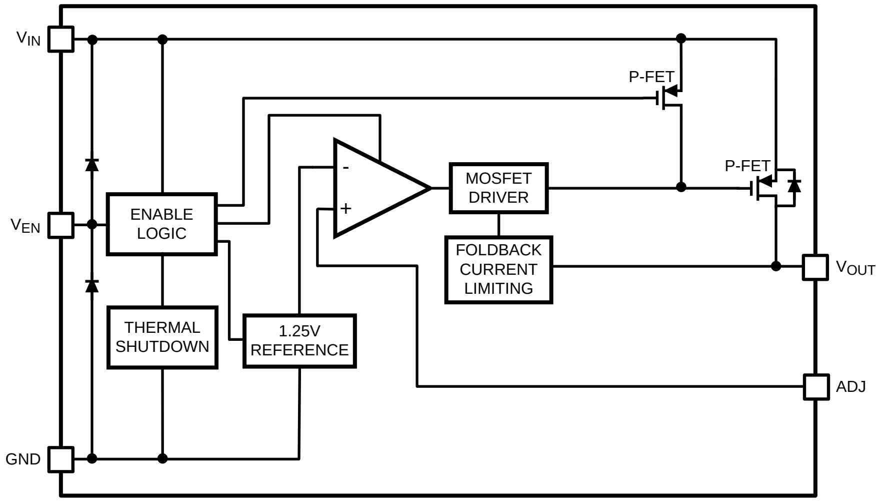
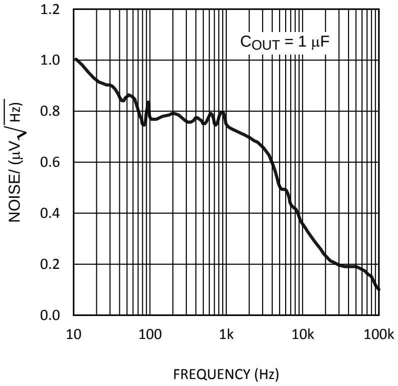


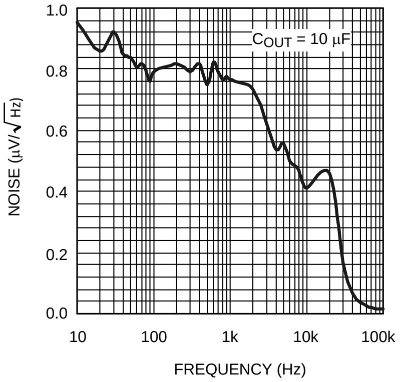
Figure 5. LP38693-ADJ Functional Diagram (SOT-223, LLP)

Typical Performance Characteristics

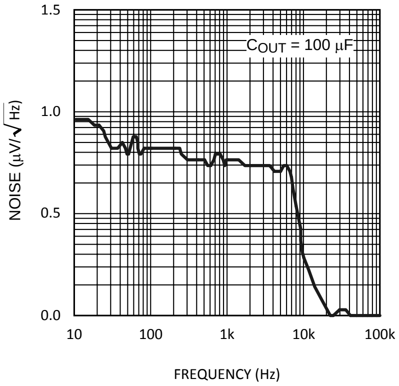
Unless otherwise specified: T_J = 25°C, C_{IN} = C_{OUT} = 10 µF, enable pin is tied to V_{IN} (LP38693-ADJ only), V_O = 1.25V, V_{IN} = 2.7V, I_L = 10mA.



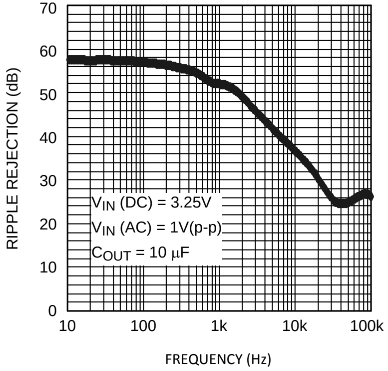
Noise vs Frequency



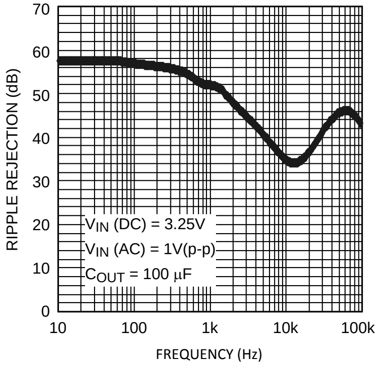
Noise vs Frequency



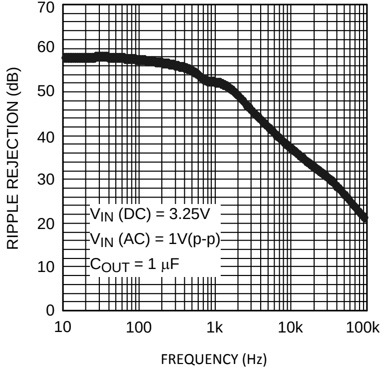
Noise vs Frequency



Ripple Rejection



Ripple Rejection

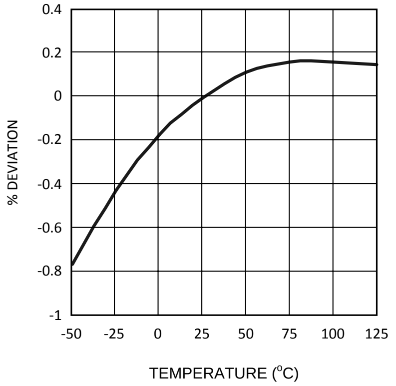


Ripple Rejection

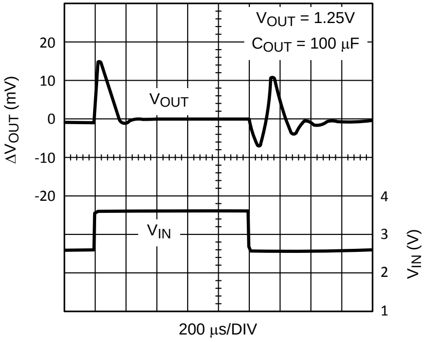
Typical Performance Characteristics (continued)

Unless otherwise specified: T_J = 25°C, C_{IN} = C_{OUT} = 10 µF, enable pin is tied to V_{IN} (LP38693-ADJ only), V_O = 1.25V, V_{IN} = 2.7V, I_L = 10mA.

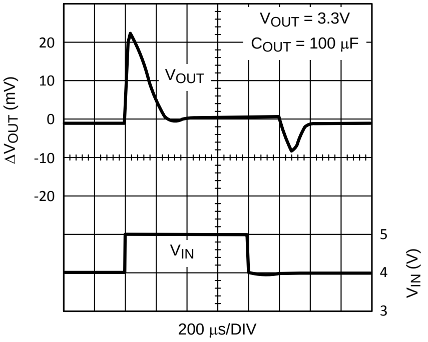
V_{REF}
vs
Temperature



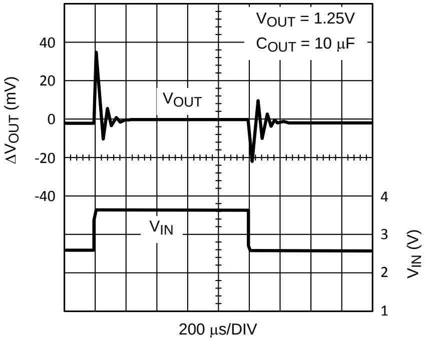
Line Transient Response



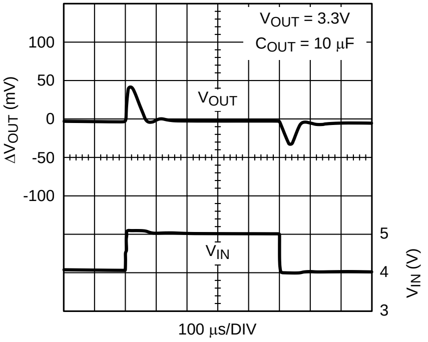
Line Transient Response



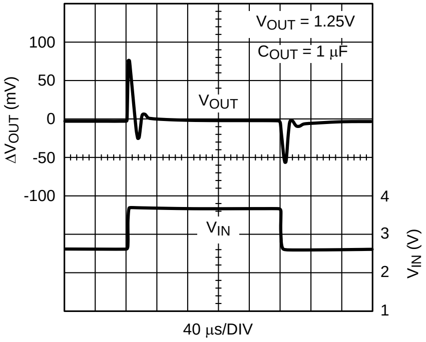
Line Transient Response



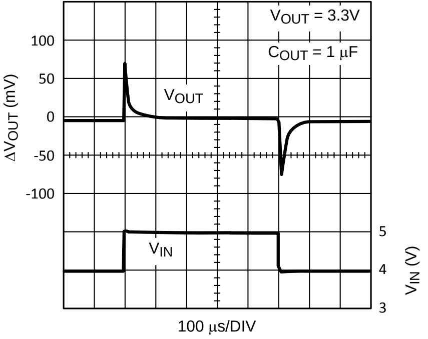
Line Transient Response



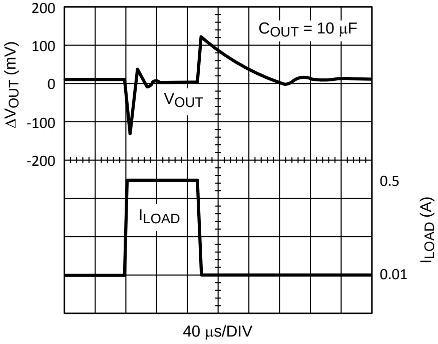
Line Transient Response



Line Transient Response

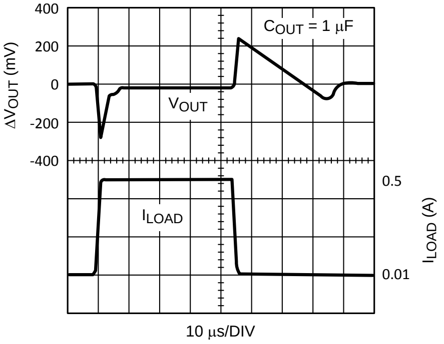


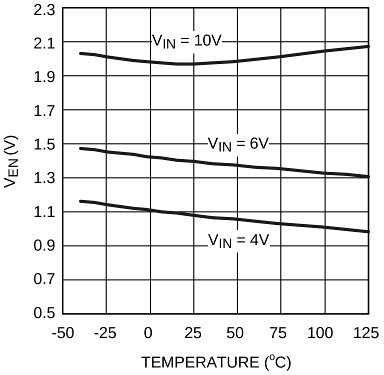
Load Transient Response

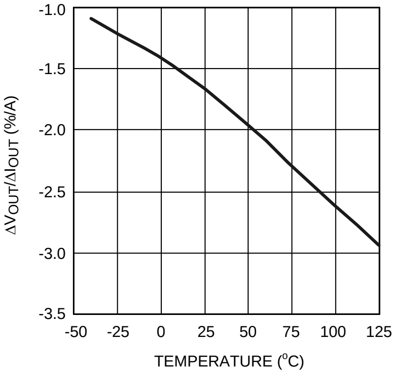


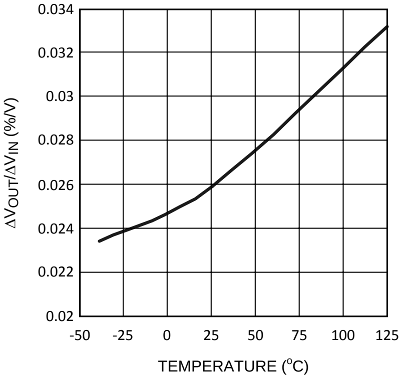
Typical Performance Characteristics (continued)

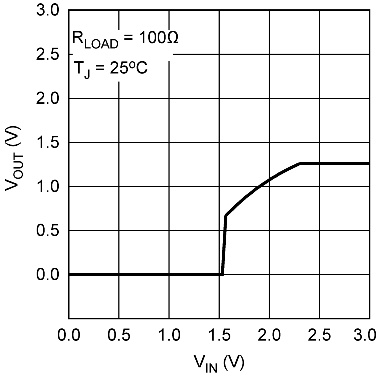
Unless otherwise specified: T_J = 25°C, C_{IN} = C_{OUT} = 10 µF, enable pin is tied to V_{IN} (LP38693-ADJ only), V_O = 1.25V, V_{IN} = 2.7V, I_L = 10mA.

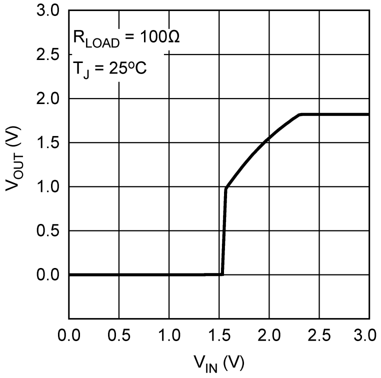

Load Transient Response


Enable Voltage vs Temperature


Load Regulation vs Temperature


Line Regulation vs Temperature

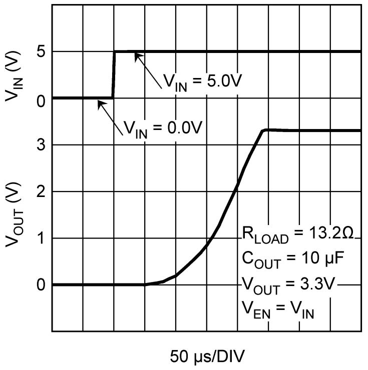

V_{OUT} vs V_{IN}, V_{OUT} = 1.25V


V_{OUT} vs V_{IN}, V_{OUT} = 1.80V

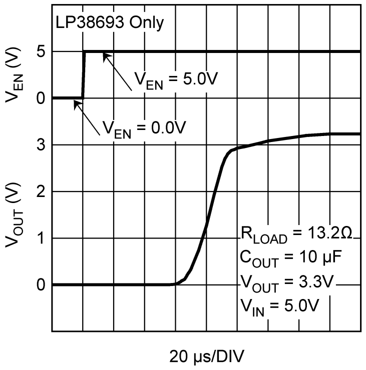
Typical Performance Characteristics (continued)

Unless otherwise specified: T_J = 25°C, $C_{IN} = C_{OUT}$ = 10 µF, enable pin is tied to V_{IN} (LP38693-ADJ only), V_O = 1.25V, V_{IN} = 2.7V, I_L = 10mA.

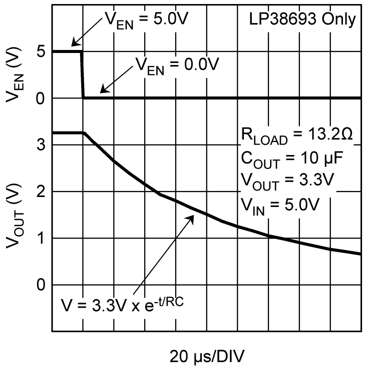
V_{OUT} vs V_{IN}, Power-Up



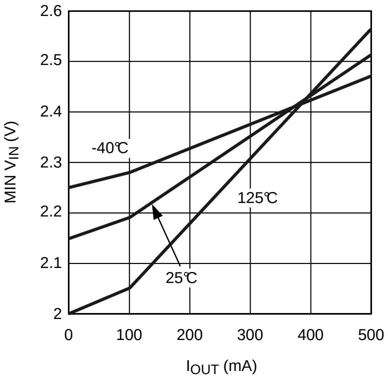
V_{OUT} vs V_{EN}, ON (LP38693 Only)



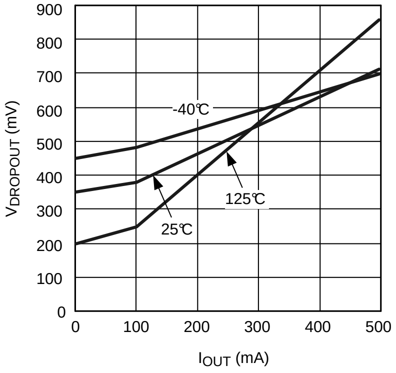
V_{OUT} vs V_{EN}, OFF (LP38693 Only)



MIN V_{IN} vs I_{OUT}



Dropout Voltage vs I_{OUT} (V_{OUT} = 1.8V)



Application Hints

EXTERNAL CAPACITORS

Like any low-dropout regulator, external capacitors are required to assure stability. These capacitors must be correctly selected for proper performance.

INPUT CAPACITOR: An input capacitor of at least 1µF is required (ceramic recommended). The capacitor must be located not more than one centimeter from the input pin and returned to a clean analog ground.

OUTPUT CAPACITOR: An output capacitor is required for loop stability. It must be located less than 1 centimeter from the device and connected directly to the output and ground pins using traces which have no other currents flowing through them.

The minimum amount of output capacitance that can be used for stable operation is 1µF. Ceramic capacitors are recommended (the LP38691/3-ADJ was designed for use with ultra low ESR capacitors). The LP38691/3-ADJ is stable with any output capacitor ESR between zero and 100 Ohms.

SETTING THE OUTPUT VOLTAGE: The output voltage is set using the external resistors R1 and R2 (see Typical Application Circuit). The output voltage will be given by the equation:

$$V_{OUT} = V_{ADJ} \times (1 + (R1 / R2)) \qquad (2)$$

Because the part has a minimum load current requirement of 100 µA, it is recommended that R2 always be 12k Ohms or less to provide adequate loading. Even if a minimum load is always provided by other means, it is not recommended that very high value resistors be used for R1 and R2 because it can make the ADJ node susceptible to noise pickup. A maximum Ohmic value of 100k is recommended for R2 to prevent this from occurring.

ENABLE PIN (LP38693-ADJ only): The LP38693–ADJ has an Enable pin (EN) which allows an external control signal to turn the regulator output On and Off. The Enable On/Off threshold has no hysteresis. The voltage signal must rise and fall cleanly, and promptly, through the ON and OFF voltage thresholds. The Enable pin has no internal pull-up or pull-down to establish a default condition and, as a result, this pin must be terminated either actively or passively. If the Enable pin is driven from a source that actively pulls high and low, the drive voltage should not be allowed to go below ground potential or higher than V_{IN}. If the application does not require the Enable function, the pin should be connected directly to the V_{IN} pin.

FOLDBACK CURRENT LIMITING: Foldback current limiting is built into the LP38691/3-ADJ which reduces the amount of output current the part can deliver as the output voltage is reduced. The amount of load current is dependent on the differential voltage between V_{IN} and V_{OUT}. Typically, when this differential voltage exceeds 5V, the load current will limit at about 350 mA. When the V_{IN} -V_{OUT} differential is reduced below 4V, load current is limited to about 850 mA.

SELECTING A CAPACITOR

It is important to note that capacitance tolerance and variation with temperature must be taken into consideration when selecting a capacitor so that the minimum required amount of capacitance is provided over the full operating temperature range.

Capacitor Characteristics

CERAMIC

For values of capacitance in the 10 to 100 µF range, ceramics are usually larger and more costly than tantalums but give superior AC performance for bypassing high frequency noise because of very low ESR (typically less than 10 mΩ). However, some dielectric types do not have good capacitance characteristics as a function of voltage and temperature.

Z5U and Y5V dielectric ceramics have capacitance that drops severely with applied voltage. A typical Z5U or Y5V capacitor can lose 60% of its rated capacitance with half of the rated voltage applied to it. The Z5U and Y5V also exhibit a severe temperature effect, losing more than 50% of nominal capacitance at high and low limits of the temperature range.

X7R and X5R dielectric ceramic capacitors are strongly recommended if ceramics are used, as they typically maintain a capacitance range within ±20% of nominal over full operating ratings of temperature and voltage. Of course, they are typically larger and more costly than Z5U/Y5U types for a given voltage and capacitance.

TANTALUM

Solid Tantalum capacitors have good temperature stability: a high quality Tantalum will typically show a capacitance value that varies less than 10-15% across the full temperature range of -40°C to 125°C. ESR will vary only about 2X going from the high to low temperature limits.

The increasing ESR at lower temperatures can cause oscillations when marginal quality capacitors are used (if the ESR of the capacitor is near the upper limit of the stability range at room temperature).

REVERSE VOLTAGE

A reverse voltage condition will exist when the voltage at the output pin is higher than the voltage at the input pin. Typically this will happen when V_{IN} is abruptly taken low and C_{OUT} continues to hold a sufficient charge such that the input to output voltage becomes reversed. A less common condition is when an alternate voltage source is connected to the output.

There are two possible paths for current to flow from the output pin back to the input during a reverse voltage condition.

1) While V_{IN} is high enough to keep the control circuity alive, and the Enable pin (LP38693-ADJ only) is above the $V_{EN(ON)}$ threshold, the control circuitry will attempt to regulate the output voltage. If the input voltage is less than the programmed output voltage, the control circuit will drive the gate of the pass element to the full ON condition. In this condition, reverse current will flow from the output pin to the input pin, limited only by the $R_{DS(ON)}$ of the pass element and the output to input voltage differential. Discharging an output capacitor up to 1000 µF in this manner will not damage the device as the current will rapidly decay. However, continuous reverse current should be avoided. When the Enable pin is low this condition will be prevented.

2) The internal PFET pass element has an inherent parasitic diode. During normal operation, the input voltage is higher than the output voltage and the parasitic diode is reverse biased. However, when V_{IN} is below the value where the control circuity is alive, or the Enable pin is low (LP38693-ADJ only), and the output voltage is more than 500 mV (typical) above the input voltage the parasitic diode becomes forward biased and current flows from the output pin to the input pin through the diode. The current in the parasitic diode should be limited to less than 1A continuous and 5A peak.

If used in a dual-supply system where the regulator output load is returned to a negative supply, the output pin must be diode clamped to ground to limit the negative voltage transition. A Schottky diode is recommended for this protective clamp.

PCB LAYOUT

Good PC layout practices must be used or instability can be induced because of ground loops and voltage drops. The input and output capacitors must be directly connected to the input, output, and ground pins of the regulator using traces which do not have other currents flowing in them (Kelvin connect).

The best way to do this is to lay out C_{IN} and C_{OUT} near the device with short traces to the V_{IN}, V_{OUT}, and ground pins. The regulator ground pin should be connected to the external circuit ground so that the regulator and its capacitors have a "single point ground".

It should be noted that stability problems have been seen in applications where "vias" to an internal ground plane were used at the ground points of the IC and the input and output capacitors. This was caused by varying ground potentials at these nodes resulting from current flowing through the ground plane. Using a single point ground technique for the regulator and it’s capacitors fixed the problem. Since high current flows through the traces going into V_{IN} and coming from V_{OUT}, Kelvin connect the capacitor leads to these pins so there is no voltage drop in series with the input and output capacitors.

LLP MOUNTING

The SDE06A (No Pullback) 6-Lead LLP package requires specific mounting techniques which are detailed in National Semiconductor Application Note # 1187. Referring to the section **PCB Design Recommendations** in AN-1187 (Page 5), it should be noted that the pad style which should be used with the LLP package is the NSMD (non-solder mask defined) type. Additionally, it is recommended the PCB terminal pads to be 0.2 mm longer than the package pads to create a solder fillet to improve reliability and inspection.

The thermal dissipation of the LLP package is directly related to the printed circuit board construction and the amount of additional copper area connected to the DAP.

The DAP (exposed pad) on the bottom of the LLP package is connected to the die substrate with a conductive die attach adhesive. The DAP has no direct electrical (wire) connection to any of the pins. There is a parasitic PN junction between the die substrate and the device ground. As such, it is strongly recommend that the DAP be connected directly to the ground at device lead 2 (i.e. GND). Alternately, but not recommended, the DAP may be left floating (i.e. no electrical connection). The DAP must not be connected to any potential other than ground.

For the LP38691SD-ADJ and LP38693SD-ADJ in the SDE06A 6-Lead LLP package, the junction-to-case thermal rating, θ_{JC}, is 10.4°C/W, where the case is the bottom of the package at the center of the DAP. The junction-to-ambient thermal performance for the LP38691SD-ADJ and LP38693SD-ADJ in the SDE06A 6-Lead LLP package, using the JEDEC JESD51 standards is summarized in the following table:

Board Type	Thermal Vias	θ_{JC}	θ_{JA}
JEDEC 2-Layer JESD 51-3	None	10.4°C/W	237°C/W
JEDEC 4-Layer JESD 51-7	1	10.4°C/W	74°C/W
	2	10.4°C/W	60°C/W
	4	10.4°C/W	49°C/W
	6	10.4°C/W	45°C/W

RFI/EMI SUSCEPTIBILITY

RFI (radio frequency interference) and EMI (electromagnetic interference) can degrade any integrated circuit’s performance because of the small dimensions of the geometries inside the device. In applications where circuit sources are present which generate signals with significant high frequency energy content (> 1 MHz), care must be taken to ensure that this does not affect the IC regulator.

If RFI/EMI noise is present on the input side of the regulator (such as applications where the input source comes from the output of a switching regulator), good ceramic bypass capacitors must be used at the input pin of the IC.

If a load is connected to the IC output which switches at high speed (such as a clock), the high-frequency current pulses required by the load must be supplied by the capacitors on the IC output. Since the bandwidth of the regulator loop is less than 100 kHz, the control circuitry cannot respond to load changes above that frequency. This means the effective output impedance of the IC at frequencies above 100 kHz is determined only by the output capacitor(s).

In applications where the load is switching at high speed, the output of the IC may need RF isolation from the load. It is recommended that some inductance be placed between the output capacitor and the load, and good RF bypass capacitors be placed directly across the load.

PCB layout is also critical in high noise environments, since RFI/EMI is easily radiated directly into PC traces. Noisy circuitry should be isolated from "clean" circuits where possible, and grounded through a separate path. At MHz frequencies, ground planes begin to look inductive and RFI/ EMI can cause ground bounce across the ground plane. In multi-layer PCB applications, care should be taken in layout so that noisy power and ground planes do not radiate directly into adjacent layers which carry analog power and ground.

OUTPUT NOISE

Noise is specified in two ways- **Spot Noise** or **Output Noise** density is the RMS sum of all noise sources, measured at the regulator output, at a specific frequency (measured with a 1Hz bandwidth). This type of noise is usually plotted on a curve as a function of frequency. **Total Output Noise** or **Broad-Band Noise** is the RMS sum of spot noise over a specified bandwidth, usually several decades of frequencies.

Attention should be paid to the units of measurement. Spot noise is measured in units µV/root-Hz or nV/root-Hz and total output noise is measured in µV(rms)

The primary source of noise in low-dropout regulators is the internal reference. Noise can be reduced in two ways: by increasing the transistor area or by increasing the current drawn by the internal reference. Increasing the area will decrease the chance of fitting the die into a smaller package. Increasing the current drawn by the internal reference increases the total supply current (ground pin current).

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
LP38691QSD-ADJ/NOPB	ACTIVE	WSON	NGG	6	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L251B	Samples
LP38691QSDX-ADJ/NOPB	ACTIVE	WSON	NGG	6	4500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L251B	Samples
LP38691SD-ADJ	ACTIVE	WSON	NGG	6	1000	TBD	CU SNPB	Level-1-260C-UNLIM	-40 to 125	L117B	Samples
LP38691SD-ADJ/NOPB	ACTIVE	WSON	NGG	6	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L117B	Samples
LP38691SDX-ADJ	ACTIVE	WSON	NGG	6	4500	TBD	CU SNPB	Level-1-260C-UNLIM	-40 to 125	L117B	Samples
LP38691SDX-ADJ/NOPB	ACTIVE	WSON	NGG	6	4500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L117B	Samples
LP38693MP-ADJ	ACTIVE	SOT-223	NDC	5	1000	TBD	CU SNPB	Level-1-260C-UNLIM	-40 to 125	LJUB	Samples
LP38693MP-ADJ/NOPB	ACTIVE	SOT-223	NDC	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LJUB	Samples
LP38693MPX-ADJ	ACTIVE	SOT-223	NDC	5	2000	TBD	CU SNPB	Level-1-260C-UNLIM	-40 to 125	LJUB	Samples
LP38693MPX-ADJ/NOPB	ACTIVE	SOT-223	NDC	5	2000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LJUB	Samples
LP38693QSD-ADJ/NOPB	ACTIVE	WSON	NGG	6	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LLRB	Samples
LP38693QSDX-ADJ/NOPB	ACTIVE	WSON	NGG	6	4500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LLRB	Samples
LP38693SD-ADJ	ACTIVE	WSON	NGG	6	1000	TBD	CU SNPB	Level-1-260C-UNLIM	-40 to 125	L127B	Samples
LP38693SD-ADJ/NOPB	ACTIVE	WSON	NGG	6	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L127B	Samples
LP38693SDX-ADJ	ACTIVE	WSON	NGG	6	4500	TBD	CU SNPB	Level-1-260C-UNLIM	-40 to 125	L127B	Samples
LP38693SDX-ADJ/NOPB	ACTIVE	WSON	NGG	6	4500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L127B	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[4] Only one of markings shown within the brackets will appear on the physical device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF LP38691-ADJ, LP38691-ADJ-Q1, LP38693-ADJ, LP38693-ADJ-Q1 :

- Catalog: LP38691-ADJ, LP38693-ADJ

- Automotive: LP38691-ADJ-Q1, LP38693-ADJ-Q1

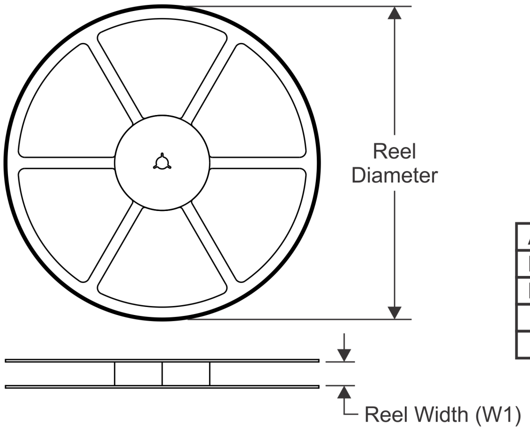
NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

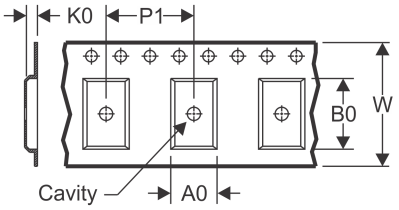
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

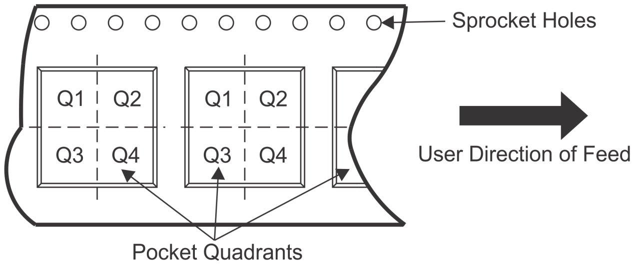


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

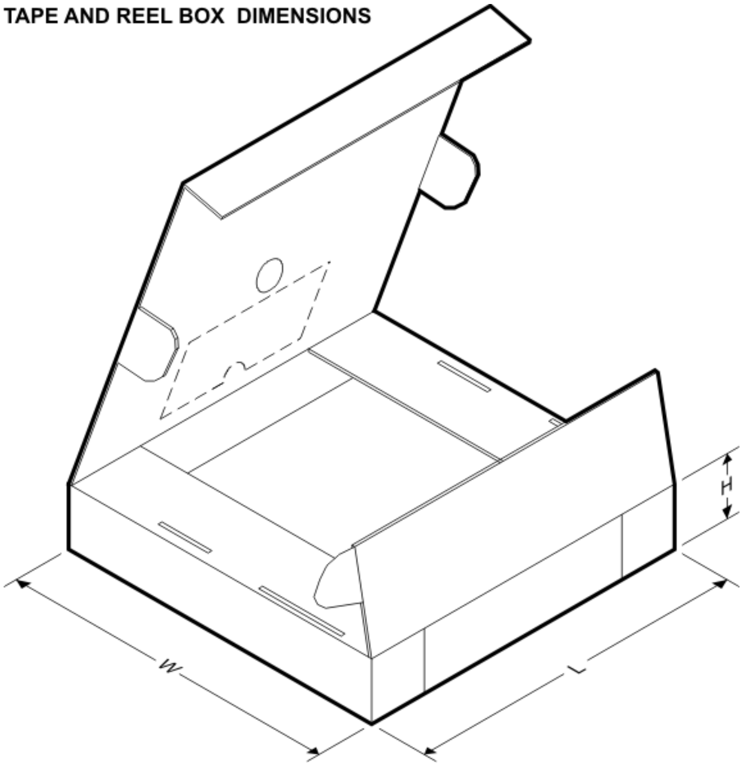
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP38691QSD-ADJ/NOPB	WSON	NGG	6	1000	178.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LP38691QSDX-ADJ/NOPB	WSON	NGG	6	4500	330.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LP38691SD-ADJ	WSON	NGG	6	1000	178.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LP38691SD-ADJ/NOPB	WSON	NGG	6	1000	178.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LP38691SDX-ADJ	WSON	NGG	6	4500	330.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LP38691SDX-ADJ/NOPB	WSON	NGG	6	4500	330.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LP38693MP-ADJ	SOT-223	NDC	5	1000	330.0	16.4	7.0	7.5	2.2	12.0	16.0	Q3
LP38693MP-ADJ/NOPB	SOT-223	NDC	5	1000	330.0	16.4	7.0	7.5	2.2	12.0	16.0	Q3
LP38693MPX-ADJ	SOT-223	NDC	5	2000	330.0	16.4	7.0	7.5	2.2	12.0	16.0	Q3
LP38693MPX-ADJ/NOPB	SOT-223	NDC	5	2000	330.0	16.4	7.0	7.5	2.2	12.0	16.0	Q3
LP38693QSD-ADJ/NOPB	WSON	NGG	6	1000	178.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LP38693QSDX-ADJ/NOPB	WSON	NGG	6	4500	330.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LP38693SD-ADJ	WSON	NGG	6	1000	178.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LP38693SD-ADJ/NOPB	WSON	NGG	6	1000	178.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LP38693SDX-ADJ	WSON	NGG	6	4500	330.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LP38693SDX-ADJ/NOPB	WSON	NGG	6	4500	330.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1

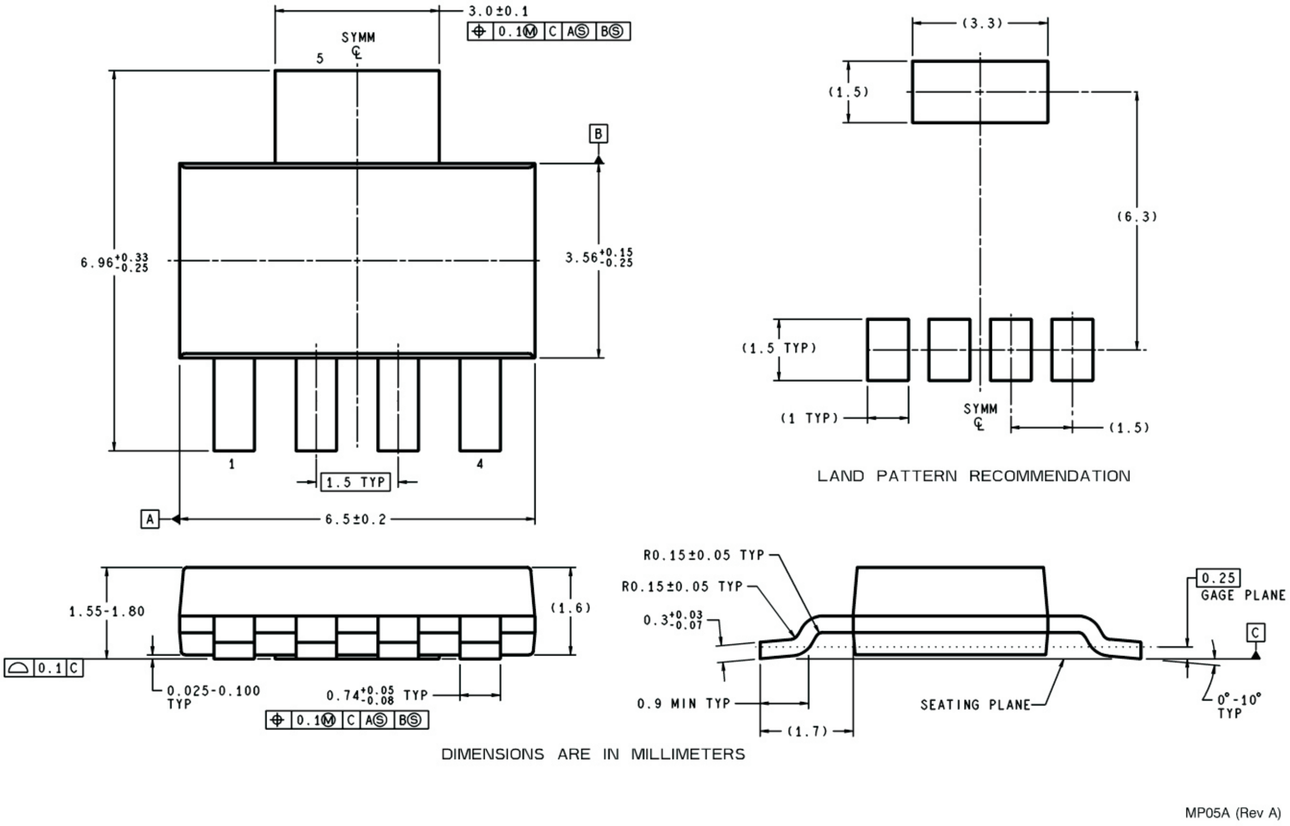
TAPE AND REEL BOX DIMENSIONS



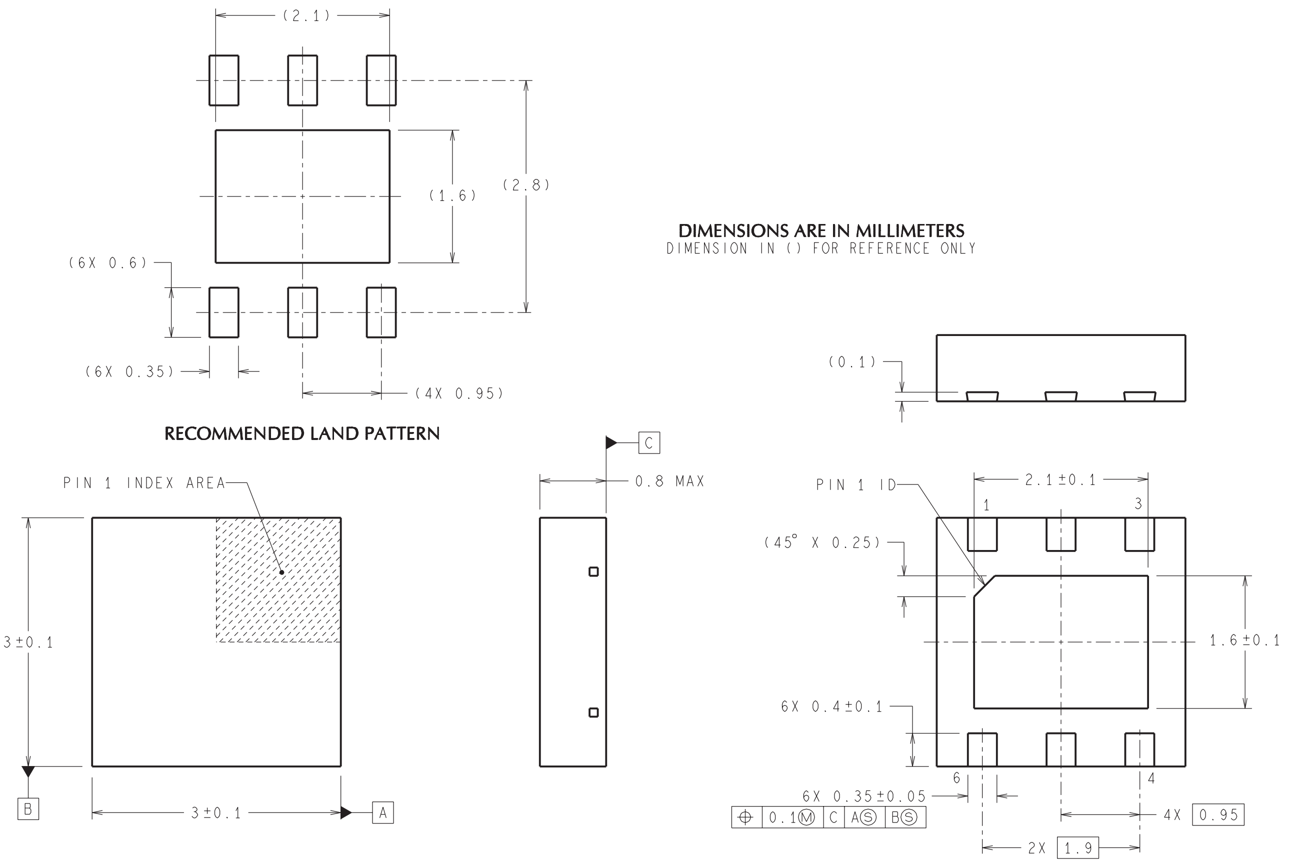
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP38691QSD-ADJ/NOPB	WSON	NGG	6	1000	203.0	190.0	41.0
LP38691QSDX-ADJ/NOPB	WSON	NGG	6	4500	349.0	337.0	45.0
LP38691SD-ADJ	WSON	NGG	6	1000	203.0	190.0	41.0
LP38691SD-ADJ/NOPB	WSON	NGG	6	1000	203.0	190.0	41.0
LP38691SDX-ADJ	WSON	NGG	6	4500	349.0	337.0	45.0
LP38691SDX-ADJ/NOPB	WSON	NGG	6	4500	349.0	337.0	45.0
LP38693MP-ADJ	SOT-223	NDC	5	1000	349.0	337.0	45.0
LP38693MP-ADJ/NOPB	SOT-223	NDC	5	1000	349.0	337.0	45.0
LP38693MPX-ADJ	SOT-223	NDC	5	2000	354.0	340.0	35.0
LP38693MPX-ADJ/NOPB	SOT-223	NDC	5	2000	354.0	340.0	35.0
LP38693QSD-ADJ/NOPB	WSON	NGG	6	1000	203.0	190.0	41.0
LP38693QSDX-ADJ/NOPB	WSON	NGG	6	4500	349.0	337.0	45.0
LP38693SD-ADJ	WSON	NGG	6	1000	203.0	190.0	41.0
LP38693SD-ADJ/NOPB	WSON	NGG	6	1000	203.0	190.0	41.0
LP38693SDX-ADJ	WSON	NGG	6	4500	349.0	337.0	45.0
LP38693SDX-ADJ/NOPB	WSON	NGG	6	4500	349.0	337.0	45.0

NDC0005A


3.0±0.1
⊕ 0.1Ⓜ C AⓈ BⓈ
SYMM
℄
5
B
6.96 +0.33 -0.25
3.56 +0.15 -0.25
1
4
1.5 TYP
A
6.5±0.2
1.55-1.80
(1.6)
⌓ 0.1 C
0.025-0.100 TYP
0.74 +0.05 -0.08 TYP
⊕ 0.1Ⓜ C AⓈ BⓈ
(3.3)
(1.5)
(6.3)
(1.5 TYP)
(1 TYP)
SYMM
℄
(1.5)
LAND PATTERN RECOMMENDATION
R0.15±0.05 TYP
R0.15±0.05 TYP
0.3 +0.03 -0.07
0.25
GAGE PLANE
C
0.9 MIN TYP
SEATING PLANE
0°-10° TYP
(1.7)
DIMENSIONS ARE IN MILLIMETERS
MP05A (Rev A)

NGG0006A



RECOMMENDED LAND PATTERN

DIMENSIONS ARE IN MILLIMETERS
DIMENSION IN ( ) FOR REFERENCE ONLY

SDE06A (Rev A)

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as “components”) are sold subject to TI’s terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI’s terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers’ products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers’ products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have ***not*** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products		**Applications**	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Applications Processors	www.ti.com/omap	**TI E2E Community**	e2e.ti.com
Wireless Connectivity	www.ti.com/wirelessconnectivity		

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265