ULTRA LOW NOISE, 250-mA LINEAR REGULATOR FOR RF AND ANALOG CIRCUITS - REQUIRES NO BYPASS CAPACITOR

Check for Samples: LP5907

FEATURES

- Stable with 1-µF Ceramic Input and Output Capacitors
- No Noise Bypass Capacitor Required
- Remote Output Capacitor Placement
- Thermal-overload and Short-circuit Protection
- –40°C to +125°C Junction Temperature Range for Operation

APPLICATIONS

- Cellular Phones
- PDA Handsets
- Wireless LAN Devices

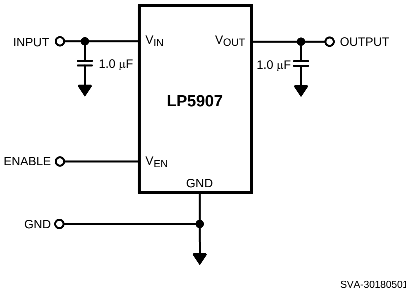
KEY SPECIFICATIONS

- Input Voltage Range: 2.2 V to 5.5 V
- Output Voltage Range: 1.2 V to 4.5 V
- Output Current: 250 mA
- Low Output Voltage Noise: <10 µV_{RMS}
- PSRR: 82 dB at 1 kHz
- Output Voltage Tolerance: ±2%
- Virtually Zero IQ (Disabled): <1 µA
- Very Low IQ (Enabled): 12 µA
- Startup Time: 80 µs
- Low Dropout: 120 mV Typical

PACKAGE

- 4-Bump Ultra-Thin Micro SMD (Lead Free): 0.35-mm Pitch, 0.65 mm × 0.65 mm × 0.40 mm
- 5-Pin SOT23 (Lead Free): 2.92 mm x 1.6 mm x 1 mm

Typical Application Circuit



DESCRIPTION

The LP5907 is a linear regulator capable of supplying 250-mA output current. Designed to meet the requirements of RF and analog circuits, the LP5907 device provides low noise, high PSRR, low quiescent current, and low line or load transient response figures. Using new innovative design techniques, the LP5907 offers class-leading noise performance without a noise bypass capacitor and the ability for remote output capacitor placement.

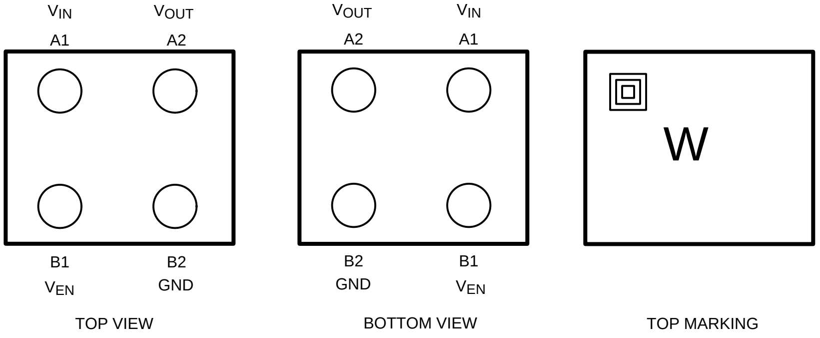
The device is designed to work with a 1-µF input and a 1-µF output ceramic capacitor (no bypass capacitor is required).

The device is available in an ultra-thin micro SMD package as well as a 5-pin SOT23 package. This device is available between 1.2 V and 4.5 V in 25-mV steps. Please contact Texas Instruments Sales for specific voltage option needs.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

CONNECTION DIAGRAMS

4-Bump Ultra-Thin micro SMD Package



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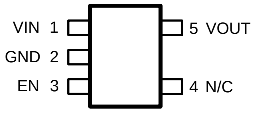
Note: The actual physical placement of the package marking will vary from part to part.

**5-Pin SOT23 Package
(Top View)**



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PIN DESCRIPTIONS

NAME	MICRO SMD PIN NO.	SOT23 PIN NO.	DESCRIPTION
VIN	A1	1	Input voltage supply. A 1-µF capacitor should be connected at this input.
VOUT	A2	5	Output voltage. A 1-µF Low ESR capacitor should be connected to this pin. Connect this output to the load circuit. An internal 280-Ω discharge resistor prevents a charge remaining on V_{OUT} when V_{EN} is low.
V_{EN}	B1	N/A	Enable input; disables the regulator when ≤0.4 V. Enables the regulator when ≥1.2 V. An internal 1-MΩ pulldown resistor connects this input to ground.
EN	N/A	3	
GND	B2	2	Common ground
N/C	N/A	4	No connect pin

ABSOLUTE MAXIMUM RATINGS(1)(2)(3)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{IN}	Input voltage		–0.3	6	V
V_{OUT}	Output voltage		–0.3 to (V_{IN} + 0.3 V)	6	V
V_{EN}	Enable input voltage		–0.3 to (V_{IN} + 0.3 V)	6	V
	Continuous power dissipation(3)		Internally Limited		
	Junction temperature (T_{JMAX})			150	°C
	Storage temperature range		–65	150	°C
	Maximum lead temperature (soldering, 10 seconds)			260	°C
	ESD rating(4)	Human body model		2	kV
		Machine model		200	V

(1) If Military or Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(2) Absolute Maximum Ratings indicate limits beyond which damage to the component may occur. Operating Ratings are conditions under which operation of the device is guaranteed. Operating Ratings do not imply guaranteed performance limits. For guaranteed performance limits and associated test conditions, see the Electrical Characteristics tables.
(3) Internal thermal shutdown circuitry protects the device from permanent damage.
(4) The Human body model is a 100 pF capacitor discharged through a 1.5 kΩ resistor into each pin. The machine model is a 200 pF capacitor discharged directly into each pin. MIL-STD-883 3015.7

OPERATING RATINGS(1)(2)

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage range	2.2		5.5	V
V_{EN}	Enable voltage range	0 to (V_{IN} + 0.3)		5.5	V
	Recommended load current(3)	0		250	mA
T_J	Junction temperature range	–40		+125	°C
T_A	Ambient temperature range(3)	–40		+85	°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the component may occur. Operating Ratings are conditions under which operation of the device is guaranteed. Operating Ratings do not imply guaranteed performance limits. For guaranteed performance limits and associated test conditions, see the Electrical Characteristics tables.
(2) All voltages are with respect to the potential at the GND pin.
(3) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature ($T_{A\text{-}MAX}$) is dependent on the maximum operating junction temperature ($T_{J\text{-}MAX\text{-}OP}$ = 125°C), the maximum power dissipation of the device in the application ($P_{D\text{-}MAX}$), and the junction-to ambient thermal resistance of the part/package in the application (θ_{JA}), as given by the following equation: $T_{A\text{-}MAX} = T_{J\text{-}MAX\text{-}OP} – (\theta_{JA} \times P_{D\text{-}MAX})$. See applications section.

THERMAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
θ_{JA}	Junction to ambient thermal resistance(1)	JEDEC board(2)	Micro SMD			119.6	°C/W
			SOT23			188.8	
		4L cellphone board (micro SMD)				186.5	

(1) Junction-to-ambient thermal resistance is highly application and board-layout dependent. In applications where high maximum power dissipation exists, special care must be paid to thermal dissipation issues in board design.
(2) Detailed description of the board can be found in JESD51-7

ELECTRICAL CHARACTERISTICS(1)(2)(3)

Limits in standard typeface are for T_A = 25°C. Limits in boldface type apply over the full operating junction temperature range (–40°C ≤ T_J ≤ +125°C). Unless otherwise noted, specifications apply to LP5907 (all packages) Typical Application Circuit (pg. 1) with:

$V_{IN} = V_{OUT\ (NOM)}$ + 1 V, V_{EN} = 1.2 V, C_{IN} = 1 µF, C_{OUT} = 1 µF, I_{OUT} = 1 mA.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IN}	Input voltage			2.2		5.5	V
ΔV_{OUT}	Output voltage tolerance	$V_{IN} = (V_{OUT(NOM)}$ + 1 V) to 5.5 V, I_{OUT} = 1 mA to 200 mA		**–2**		**2**	%
		$V_{IN} = (V_{OUT(NOM)}$ + 1 V) to 5.5 V, I_{OUT} = 1 mA to 200 mA (V_{OUT} < 1.8V, SOT23)		**-3**		**3**	
	Line regulation	$V_{IN} = (V_{OUT(NOM)}$ + 1 V) to 5.5 V, I_{OUT} = 1 mA			0.02		%/V
	Load regulation	I_{OUT} = 1 mA to 250 mA			0.001		%/mA
I_{LOAD}	Load current	See (4)					mA
	Maximum output current			**250**			
I_Q	Quiescent current(5)	V_{EN} = 1.2 V, I_{OUT} = 0 mA			12	**25**	µA
		V_{EN} = 1.2 V, I_{OUT} = 250 mA			250	**425**	
		V_{EN} = 0.3 V (Disabled)			0.2	**1**	
I_G	Ground current(6)	I_{OUT} = 0 mA (V_{EN} = 1.2 V)			14		µA
V_{DO}	Dropout voltage(7)	V_{OUT} = 2.8 V, I_{OUT} = 100 mA			50		mV
		V_{OUT} = 2.8 V, I_{OUT} = 250 mA			120	**200**	
		V_{OUT} = 2.8 V, I_{OUT} = 250 mA (SOT23 package)				**250**	
I_{SC}	Short circuit current limit	See (8)		250	500		mA
PSRR	Power supply rejection ratio(9)	f = 100 Hz, I_{OUT} = 20 mA			90		dB
		f = 1 kHz, I_{OUT} = 20 mA			82		
		f = 10 kHz, I_{OUT} = 20 mA			65		
		f = 100 kHz, I_{OUT} = 20 mA			60		
e_N	Output noise voltage(9)	BW = 10 Hz to 100 kHz	I_{OUT} = 1 mA		10		μV_{RMS}
			I_{OUT} = 250 mA		6.5		
$T_{SHUTDOWN}$	Thermal shutdown	Temperature			160		°C
		Hysteresis			15		
LOGIN INPUT THRESHOLDS							
V_{IL}	Low input threshold (V_{EN})	V_{IN} = 2.2 V to 5.5 V				**0.4**	V
V_{IH}	High input threshold (V_{EN})	V_{IN} = 2.2 V to 5.5 V		**1.2**			V
I_{EN}	Input current at V_{EN} Pin(10)	V_{EN} = 5.5 V and V_{IN} = 5.5 V			5.5		µA
		V_{EN} = 0 V and V_{IN} = 5.5 V			0.001		

(1) All voltages are with respect to the potential at the GND pin.

(2) Min and Max limits are ensured by design, test, or statistical analysis. Typical numbers are not guaranteed, but do represent the most likely norm.

(3) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature ($T_{A\text{-}MAX}$) is dependent on the maximum operating junction temperature ($T_{J\text{-}MAX\text{-}OP}$ = 125°C), the maximum power dissipation of the device in the application ($P_{D\text{-}MAX}$), and the junction-to ambient thermal resistance of the part/package in the application θ_{JA}), as given by the following equation: $T_{A\text{-}MAX} = T_{J\text{-}MAX\text{-}OP} - (\theta_{JA} \times P_{D\text{-}MAX})$. See applications section.

(4) The device maintains a stable, regulated output voltage without a load current.

(5) Quiescent current is defined here as the difference in current between the input voltage source and the load at V_{OUT}.

(6) Ground current is defined here as the total current flowing to ground as a result of all input voltages applied to the device.

(7) Dropout voltage is the voltage difference between the input and the output at which the output voltage drops to 100 mV below its nominal value.

(8) Short Circuit Current is measured with V_{OUT} pulled to 0 V and V_{IN} worst case = 6 V.

(9) This specification is ensured by design.

(10) There is a 1-MΩ resistor between V_{EN} and ground on the device.

ELECTRICAL CHARACTERISTICS[1][2][3] (continued)

Limits in standard typeface are for T_A = 25°C. Limits in boldface type apply over the full operating junction temperature range (–40°C ≤ T_J ≤ +125°C). Unless otherwise noted, specifications apply to LP5907 (all packages) Typical Application Circuit (pg. 1) with:
$V_{IN} = V_{OUT\ (NOM)} + 1$ V, $V_{EN} = 1.2$ V, $C_{IN} = 1$ µF, $C_{OUT} = 1$ µF, $I_{OUT} = 1$ mA.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
TRANSIENT CHARACTERISTICS						
ΔV_{OUT}	Line transient[11]	$V_{IN} = (V_{OUT(NOM)} + 1$ V) to $(V_{OUT(NOM)} + 1.6$ V) in 30 µs, $I_{OUT} = 1$ mA	**–1**			mV
		$V_{IN} = (V_{OUT(NOM)} + 1.6$ V) to $(V_{OUT(NOM)} + 1$ V) in 30 µs, IOUT = 1 mA			**1**	
	Load transient[11]	I_{OUT} = 1mA to 200 mA in 10 µs	**–40**			mV
		I_{OUT} = 200 mA to 1mA in 10 µs			**40**	
	Overshoot on startup[11]	Stated as a percentage of nominal VOUT			**5**	%
	Turn-on time	To 95% of $V_{OUT(NOM)}$		80	150	µs

(11) This specification is ensured by design.

OUTPUT AND INPUT CAPACITORS

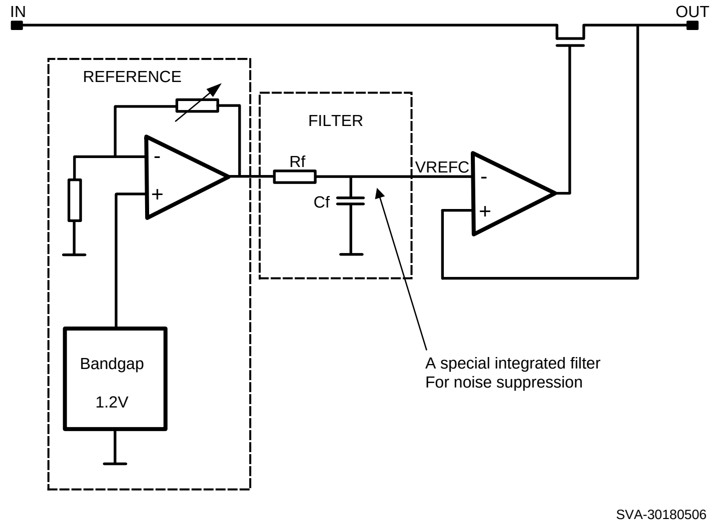
over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN[1]	TYP	MAX	UNIT
C_{IN}	Input capacitance[2]	Capacitance for stability	0.7	1		µF
C_{OUT}	Output capacitance[2]		0.7	1	10	
ESR	Output/Input capacitance[2]		5		500	mΩ

[1] Note: The minimum capacitance should be greater than 0.5 µF over the full range of operating conditions. The capacitor tolerance should be 30% or better over the full temperature range. The full range of operating conditions for the capacitor in the application should be considered during device selection to ensure this minimum capacitance specification is met. X7R capacitors are recommended however capacitor types X5R, Y5V and Z5U may be used with consideration of the application and conditions.

[2] This specification is guaranteed by design.

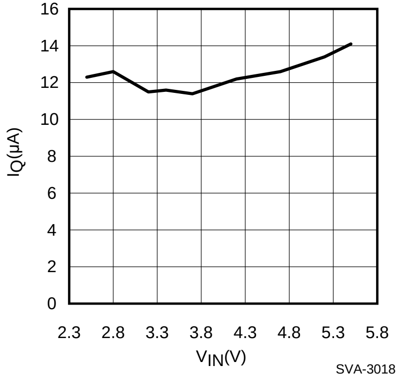
BLOCK DIAGRAM



TYPICAL CHARACTERISTICS

Unless otherwise noted, these curves apply to the micro SMD package only, V_{OUT} = 2.8 V, V_{IN} = 3.7 V, E_N = 1.2 V, C_{IN} = 1 µF, C_{OUT} = 1 µF, T_A = 25°C.

Quiescent Current vs Input Voltage



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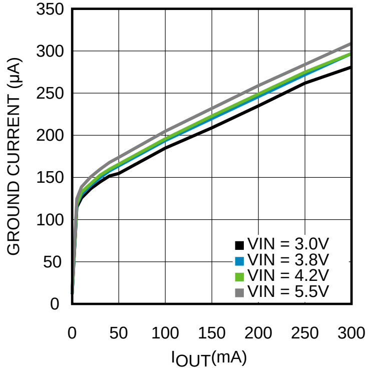
Ground Current vs Output Current



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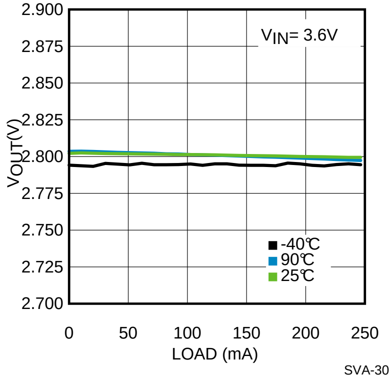
Load Regulation



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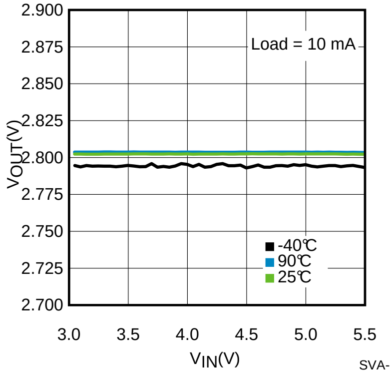
Line Regulation



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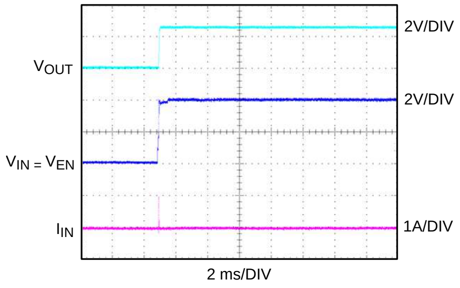
Inrush Current



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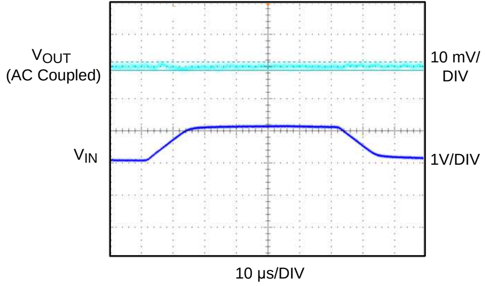
Line Transient

V_{IN} = 3.2 V ↔ 4.2 V, Load = 1 mA



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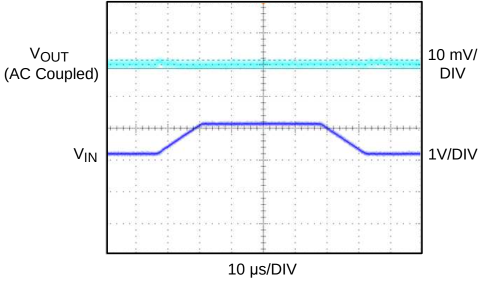
Line Transient

V_{IN} = 3.2 V ↔ 4.2 V, Load = 250 mA



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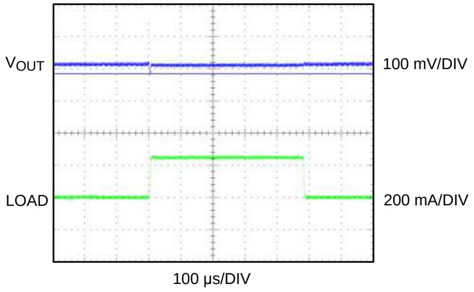
Load Transient,

Load = 0 mA ↔ 250 mA, -40°C



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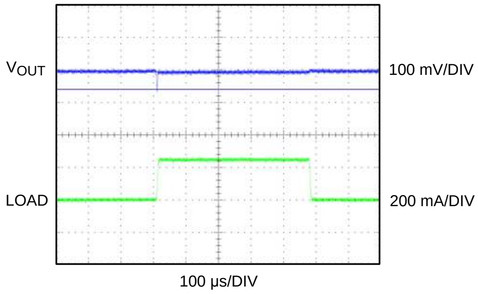
TYPICAL CHARACTERISTICS (continued)

Unless otherwise noted, these curves apply to the micro SMD package only, V_{OUT} = 2.8 V, V_{IN} = 3.7 V, E_N = 1.2 V, C_{IN} = 1 µF, C_{OUT} = 1 µF, T_A = 25°C.

Load Transient, Load = 0 mA ↔ 250 mA, 90°C



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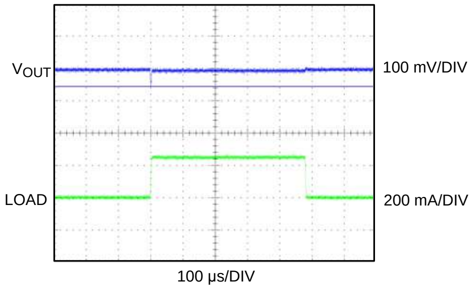
Load Transient, Load = 0 mA ↔ 250 mA, 25°C



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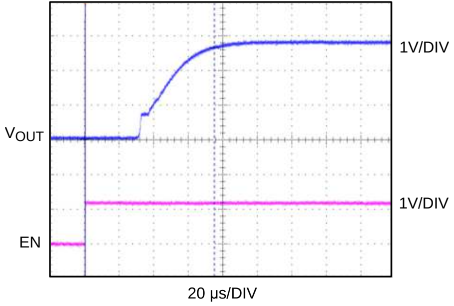
Startup 0 mA



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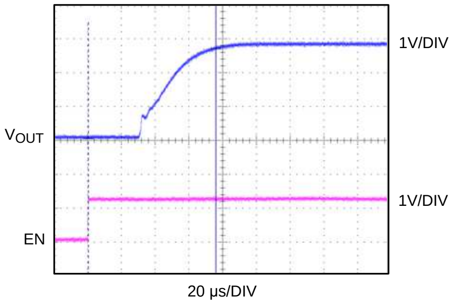
Startup 250 mA



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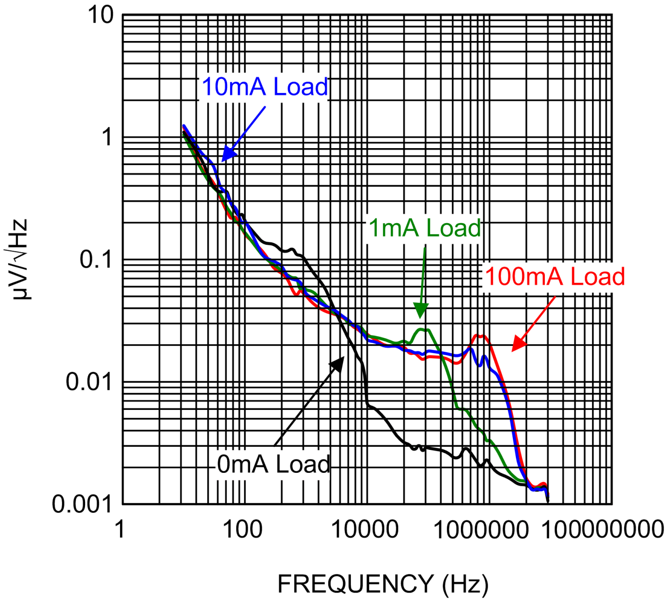
Noise Density Test



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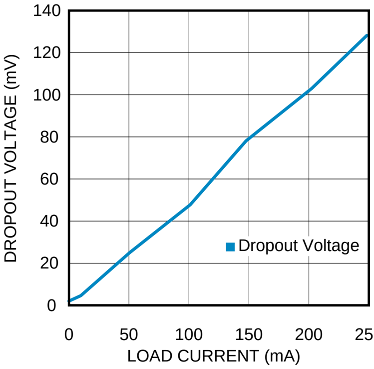
Dropout Voltage vs Load Current



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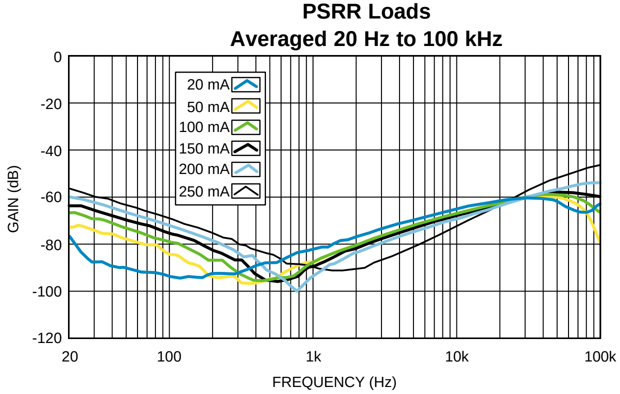
TYPICAL CHARACTERISTICS (continued)

Unless otherwise noted, these curves apply to the micro SMD package only, V_{OUT} = 2.8 V, V_{IN} = 3.7 V, E_N = 1.2 V, C_{IN} = 1 µF, C_{OUT} = 1 µF, T_A = 25°C.



PSRR Loads Averaged 20 Hz to 100 kHz

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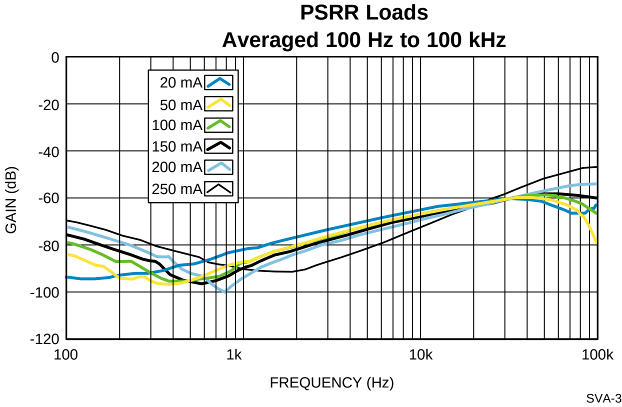

PSRR Loads Averaged 100 Hz to 100 kHz

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APPLICATION INFORMATION

POWER DISSIPATION AND DEVICE OPERATION

The permissible power dissipation for any package is a measure of the capability of the device to pass heat from the power source, the junctions of the IC, to the ultimate heat sink, the ambient environment. Thus the power dissipation is dependent on the ambient temperature and the thermal resistance across the various interfaces between the die and ambient air. As stated in Note (3) of the electrical characteristics, the allowable power dissipation for the device in a given package can be calculated using the equation:

$$P_D = \frac{(T_{JMAX} - T_A)}{\theta_{JA}} \tag{1}$$

The actual power dissipation across the device can be represented by the following equation:

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \tag{2}$$

This establishes the relationship between the power dissipation allowed due to thermal consideration, the voltage drop across the device, and the continuous current capability of the device. These two equations should be used to determine the optimum operating conditions for the device in the application.

EXTERNAL CAPACITORS

Like any low-dropout regulator, the LP5907 requires external capacitors for regulator stability. The LP5907 is specifically designed for portable applications requiring minimum board space and smallest components. These capacitors must be correctly selected for good performance.

INPUT CAPACITOR

An input capacitor is required for stability. The input capacitor should be at least equal to, or greater than, the output capacitor for good load transient performance. At least a 1-µF capacitor has to be connected between the LP5907 input pin and ground for stable operation over full load current range. Basically, it is ok to have more output capacitance than input, as long as the input is at least 1-µF.

This capacitor must be located a distance of not more than 1cm from the input pin and returned to a clean analog ground. Any good quality ceramic, tantalum, or film capacitor may be used at the input.

Important: To ensure stable operation it is essential that good PCB practices are employed to minimize ground impedance and keep input inductance low. If these conditions cannot be met, or if long leads are to be used to connect the battery or other power source to the LP5907, then it is recommended to increase the input capacitor to at least 10 µF. Also, tantalum capacitors can suffer catastrophic failures due to surge current when connected to a low-impedance source of power (like a battery or a very large capacitor). If a tantalum capacitor is used at the input, it must be guaranteed by the manufacturer to have a surge current rating sufficient for the application. There are no requirements for the ESR (Equivalent Series Resistance) on the input capacitor, but tolerance and temperature coefficient must be considered when selecting the capacitor to ensure the capacitance will remain 1 µF ±30% over the entire operating temperature range.

OUTPUT CAPACITOR

The LP5907 is designed specifically to work with a very small ceramic output capacitor, typically 1 µF. A ceramic capacitor (dielectric types X5R or X7R) in the 1 µF to 10 µF range, and with ESR between 5 mΩ to 500 mΩ, is suitable in the LP5907 application circuit. For this device the output capacitor should be connected between the V_{OUT} pin and a good ground connection.

It may also be possible to use tantalum or film capacitors at the device output, V_{OUT}, but these are not as attractive for reasons of size and cost (see *CAPACITOR CHARACTERISTICS* below).

The output capacitor must meet the requirement for the minimum value of capacitance and have an ESR value that is within the range 5 mΩ to 500 mΩ for stability.

CAPACITOR CHARACTERISTICS

The LP5907 is designed to work with ceramic capacitors on the input and output to take advantage of the benefits they offer. For capacitance values in the range of 1 µF to 10 µF, ceramic capacitors are the smallest, least expensive and have the lowest ESR values, thus making them best for eliminating high frequency noise. The ESR of a typical 1 µF ceramic capacitor is in the range of 20 mΩ to 40 mΩ, which easily meets the ESR requirement for stability for the LP5907.

The temperature performance of ceramic capacitors varies by type and manufacturer. Most large value ceramic capacitors (≥2.2 µF) are manufactured with Z5U or Y5V temperature characteristics, which results in the capacitance dropping by more than 50% as the temperature goes from 25°C to 85°C.

A better choice for temperature coefficient in a ceramic capacitor is X7R. This type of capacitor is the most stable and holds the capacitance within ±15% over the temperature range. Tantalum capacitors are less desirable than ceramic for use as output capacitors because they are more expensive when comparing equivalent capacitance and voltage ratings in the 1 µF to 10 µF range.

Another important consideration is that tantalum capacitors have higher ESR values than equivalent size ceramics. This means that while it may be possible to find a tantalum capacitor with an ESR value within the stable range, it would have to be larger in capacitance (which means bigger and more costly) than a ceramic capacitor with the same ESR value. It should also be noted that the ESR of a typical tantalum will increase about 2:1 as the temperature goes from 25°C down to –40°C, so some guard band must be allowed.

REMOTE CAPACITOR OPERATION

The LP5907 requires at least a 1-µF capacitor at output pin, but there is no strict requirements about the location of the capacitor in regards the LDO output pin. In practical designs the output capacitor may be located some 5-10 cm away from the LDO. This means that there is no need to have a special capacitor close to the output pin if there is already respective capacitors in the system (like a capacitor at the input of supplied part). The remote capacitor feature helps user to minimize the number of capacitors in the system.

As a good design practice, it is good to keep the wiring parasitic inductance at a minimum, which means to use as wide as possible traces from the LDO output to the capacitors, keeping the LDO trace layer as close as possible to ground layer and avoiding vias on the path. If there is a need to use vias, implement as many as possible vias between the connection layers. The recommendation is to keep parasitic wiring inductance less than 35 nH. For the applications with fast load transients, it is recommended to use an input capacitor equal to or larger to the sum of the capacitance at the output node for the best load transient performance.

NO-LOAD STABILITY

The LP5907 will remain stable and in regulation with no external load.

ENABLE CONTROL

The LP5907 may be switched ON or OFF by a logic input at the ENABLE pin. A high voltage at this pin will turn the device on. When the enable pin is low, the regulator output is off and the device typically consumes 3 nA. However if the application does not require the shutdown feature, the V_{EN} pin can be tied to V_{IN} to keep the regulator output permanently on.

A 1-MΩ pulldown resistor ties the V_{EN} input to ground, this ensures that the device will remain off when the enable pin is left open circuit. To ensure proper operation, the signal source used to drive the V_{EN} input must be able to swing above and below the specified turn-on/off voltage thresholds listed in the Electrical Characteristics section under V_{IL} and V_{IH}.

MICRO SMD MOUNTING

The micro SMD package requires specific mounting techniques, which are detailed in Texas Instruments Application Note AN-1112.

For best results during assembly, alignment ordinals on the PC board may be used to facilitate placement of the micro SMD device.

MICRO SMD LIGHT SENSITIVITY

Exposing the micro SMD device to direct light may cause incorrect operation of the device. Light sources such as halogen lamps can affect electrical performance if they are situated in proximity to the device.

Light with wavelengths in the red and infrared part of the spectrum have the most detrimental effect; thus, the fluorescent lighting used inside most buildings has very little effect on performance.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
LP5907MFX-1.2	ACTIVE					TBD	Call TI	Call TI	-40 to 85		Samples
LP5907MFX-1.2/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85		Samples
LP5907MFX-1.8	ACTIVE			5		TBD	Call TI	Call TI	-40 to 85		Samples
LP5907MFX-1.8/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-55 to 150		Samples
LP5907MFX-2.8/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85		Samples
LP5907MFX-2.85/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85		Samples
LP5907MFX-3.0/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85		Samples
LP5907MFX-3.1/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85		Samples
LP5907MFX-3.2/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85		Samples
LP5907MFX-3.3/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85		Samples
LP5907MFX-4.5/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85		Samples
LP5907SNE-1.2/NOPB	PREVIEW	X2SON	DQN	4	1	TBD	Call TI	Call TI	-40 to 85		
LP5907SNE-2.8/NOPB	PREVIEW	X2SON	DQN	4	1	TBD	Call TI	Call TI	-40 to 85		
LP5907SNE-2.85/NOPB	PREVIEW	X2SON	DQN	4		TBD	Call TI	Call TI	-40 to 85		
LP5907SNE-3.1/NOPB	PREVIEW	X2SON	DQN	4	1	TBD	Call TI	Call TI	-40 to 85		
LP5907SNE-4.5/NOPB	PREVIEW	X2SON	DQN	4		TBD	Call TI	Call TI	-40 to 85		
LP5907SNX-1.2	PREVIEW	X2SON	DQN	4		TBD	Call TI	Call TI	-40 to 125		
LP5907SNX-1.2/NOPB	PREVIEW	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85		
LP5907SNX-1.8	PREVIEW	X2SON	DQN	4		TBD	Call TI	Call TI	-40 to 125		
LP5907SNX-2.7	PREVIEW	X2SON	DQN	4		TBD	Call TI	Call TI	-40 to 125		
LP5907SNX-2.8	PREVIEW	X2SON	DQN	4		TBD	Call TI	Call TI	-40 to 125		

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
LP5907SNX-2.8/NOPB	PREVIEW	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125		
LP5907SNX-2.85	PREVIEW	X2SON	DQN	4		TBD	Call TI	Call TI	-40 to 125		
LP5907SNX-2.85/NOPB	PREVIEW	X2SON	DQN	4		Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125		
LP5907SNX-3.0	PREVIEW	X2SON	DQN	4		TBD	Call TI	Call TI	-40 to 125		
LP5907SNX-3.1	PREVIEW	X2SON	DQN	4		TBD	Call TI	Call TI	-40 to 125		
LP5907SNX-3.1/NOPB	PREVIEW	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125		
LP5907SNX-3.2	PREVIEW	X2SON	DQN	4		TBD	Call TI	Call TI	-40 to 125		
LP5907SNX-3.3	PREVIEW	X2SON	DQN	4		TBD	Call TI	Call TI	-40 to 125		
LP5907SNX-4.5	PREVIEW	X2SON	DQN	4		TBD	Call TI	Call TI	-40 to 125		
LP5907SNX-4.5/NOPB	PREVIEW	X2SON	DQN	4		Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125		
LP5907UVE-1.2/NOPB	ACTIVE	DSBGA	YKE	4	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	R	Samples
LP5907UVE-1.8/NOPB	ACTIVE	DSBGA	YKE	4	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	S	Samples
LP5907UVE-2.8/NOPB	ACTIVE	DSBGA	YKE	4	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	U	Samples
LP5907UVE-2.85/NOPB	ACTIVE	DSBGA	YKE	4	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	V	Samples
LP5907UVE-3.0/NOPB	ACTIVE	DSBGA	YKE	4	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	B	Samples
LP5907UVE-3.1/NOPB	ACTIVE	DSBGA	YKE	4	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	X	Samples
LP5907UVE-3.3/NOPB	ACTIVE	DSBGA	YKE	4	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	D	Samples
LP5907UVE-4.5/NOPB	ACTIVE	DSBGA	YKE	4	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	Z	Samples
LP5907UVX-1.2/NOPB	ACTIVE	DSBGA	YKE	4	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	R	Samples
LP5907UVX-1.8/NOPB	ACTIVE	DSBGA	YKE	4	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	S	Samples
LP5907UVX-1.9/NOPB	PREVIEW	DSBGA	YKE	4		TBD	Call TI	Call TI	-40 to 85		

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
LP5907UVX-2.8/NOPB	ACTIVE	DSBGA	YKE	4	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	U	Samples
LP5907UVX-2.85/NOPB	ACTIVE	DSBGA	YKE	4	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	V	Samples
LP5907UVX-3.0/NOPB	ACTIVE	DSBGA	YKE	4	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	B	Samples
LP5907UVX-3.1/NOPB	ACTIVE	DSBGA	YKE	4	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	X	Samples
LP5907UVX-3.3/NOPB	ACTIVE	DSBGA	YKE	4	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	D	Samples
LP5907UVX-4.5/NOPB	ACTIVE	DSBGA	YKE	4	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	Z	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Only one of markings shown within the brackets will appear on the physical device.

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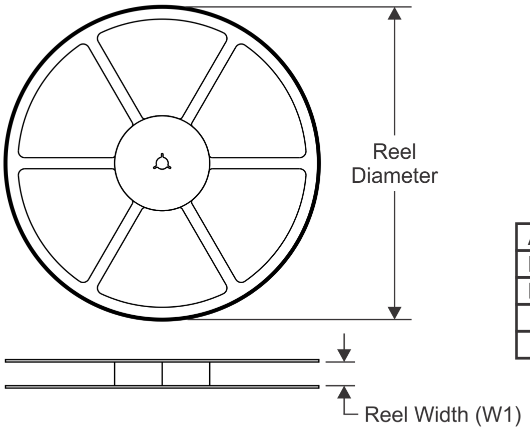
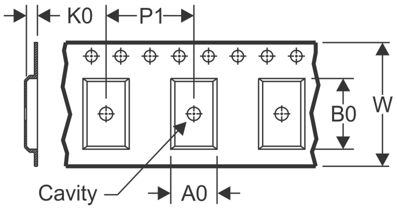
TAPE AND REEL INFORMATION

REEL DIMENSIONS

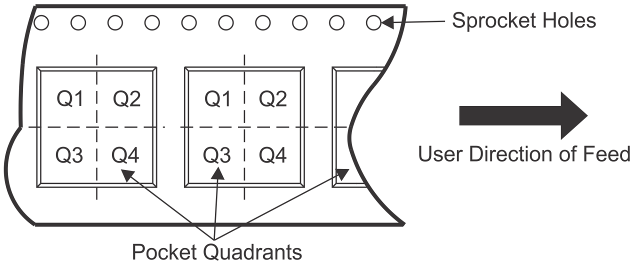


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

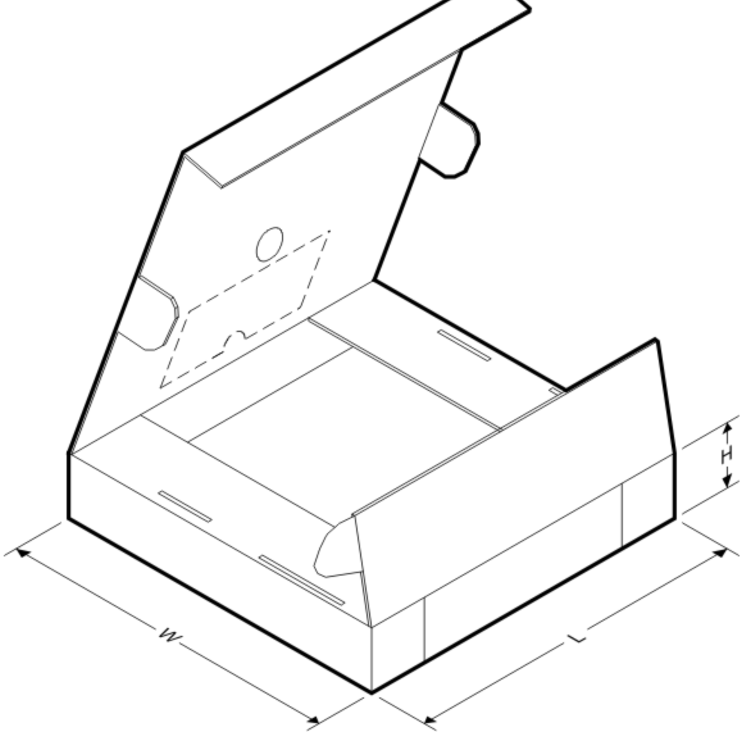


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP5907MFX-1.2/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP5907MFX-1.8/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP5907MFX-2.8/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP5907MFX-2.85/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP5907MFX-3.0/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP5907MFX-3.1/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP5907MFX-3.2/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP5907MFX-3.3/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP5907MFX-4.5/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP5907UVE-1.2/NOPB	DSBGA	YKE	4	250	178.0	8.4	0.71	0.71	0.51	4.0	8.0	Q1
LP5907UVE-1.8/NOPB	DSBGA	YKE	4	250	178.0	8.4	0.71	0.71	0.51	4.0	8.0	Q1
LP5907UVE-2.8/NOPB	DSBGA	YKE	4	250	178.0	8.4	0.71	0.71	0.51	4.0	8.0	Q1
LP5907UVE-2.85/NOPB	DSBGA	YKE	4	250	178.0	8.4	0.71	0.71	0.51	4.0	8.0	Q1
LP5907UVE-3.0/NOPB	DSBGA	YKE	4	250	178.0	8.4	0.71	0.71	0.51	4.0	8.0	Q1
LP5907UVE-3.1/NOPB	DSBGA	YKE	4	250	178.0	8.4	0.71	0.71	0.51	4.0	8.0	Q1
LP5907UVE-3.3/NOPB	DSBGA	YKE	4	250	178.0	8.4	0.71	0.71	0.51	4.0	8.0	Q1
LP5907UVE-4.5/NOPB	DSBGA	YKE	4	250	178.0	8.4	0.71	0.71	0.51	4.0	8.0	Q1
LP5907UVX-1.2/NOPB	DSBGA	YKE	4	3000	178.0	8.4	0.71	0.71	0.51	4.0	8.0	Q1

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP5907UVX-1.8/NOPB	DSBGA	YKE	4	3000	178.0	8.4	0.71	0.71	0.51	4.0	8.0	Q1
LP5907UVX-2.8/NOPB	DSBGA	YKE	4	3000	178.0	8.4	0.71	0.71	0.51	4.0	8.0	Q1
LP5907UVX-2.85/NOPB	DSBGA	YKE	4	3000	178.0	8.4	0.71	0.71	0.51	4.0	8.0	Q1
LP5907UVX-3.0/NOPB	DSBGA	YKE	4	3000	178.0	8.4	0.71	0.71	0.51	4.0	8.0	Q1
LP5907UVX-3.1/NOPB	DSBGA	YKE	4	3000	178.0	8.4	0.71	0.71	0.51	4.0	8.0	Q1
LP5907UVX-3.3/NOPB	DSBGA	YKE	4	3000	178.0	8.4	0.71	0.71	0.51	4.0	8.0	Q1
LP5907UVX-4.5/NOPB	DSBGA	YKE	4	3000	178.0	8.4	0.71	0.71	0.51	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS

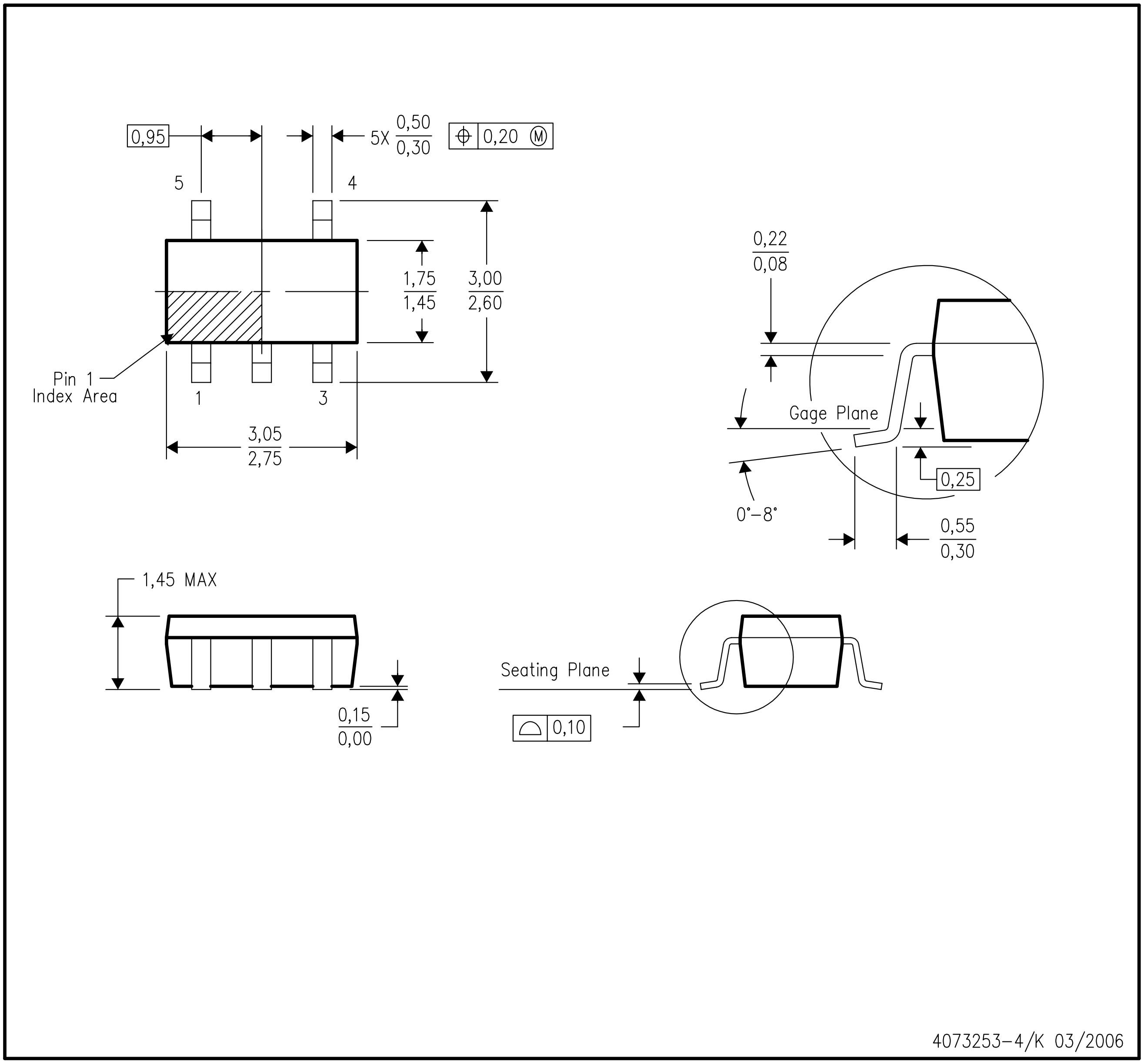


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP5907MFX-1.2/NOPB	SOT-23	DBV	5	3000	206.0	191.0	90.0
LP5907MFX-1.8/NOPB	SOT-23	DBV	5	3000	206.0	191.0	90.0
LP5907MFX-2.8/NOPB	SOT-23	DBV	5	3000	206.0	191.0	90.0
LP5907MFX-2.85/NOPB	SOT-23	DBV	5	3000	206.0	191.0	90.0
LP5907MFX-3.0/NOPB	SOT-23	DBV	5	3000	206.0	191.0	90.0
LP5907MFX-3.1/NOPB	SOT-23	DBV	5	3000	206.0	191.0	90.0
LP5907MFX-3.2/NOPB	SOT-23	DBV	5	3000	206.0	191.0	90.0
LP5907MFX-3.3/NOPB	SOT-23	DBV	5	3000	206.0	191.0	90.0
LP5907MFX-4.5/NOPB	SOT-23	DBV	5	3000	206.0	191.0	90.0
LP5907UVE-1.2/NOPB	DSBGA	YKE	4	250	203.0	190.0	41.0

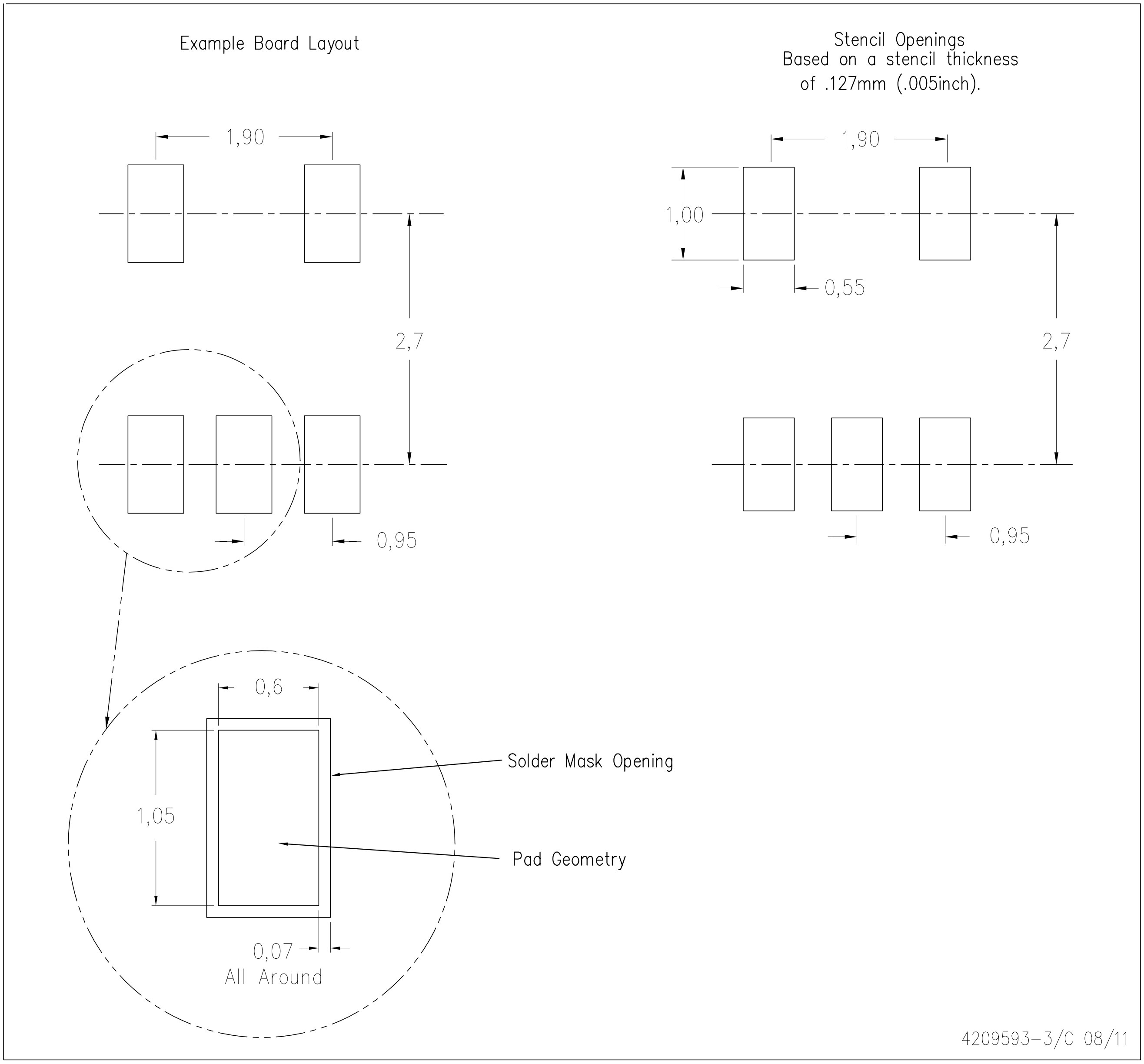
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP5907UVE-1.8/NOPB	DSBGA	YKE	4	250	203.0	190.0	41.0
LP5907UVE-2.8/NOPB	DSBGA	YKE	4	250	203.0	190.0	41.0
LP5907UVE-2.85/NOPB	DSBGA	YKE	4	250	203.0	190.0	41.0
LP5907UVE-3.0/NOPB	DSBGA	YKE	4	250	203.0	190.0	41.0
LP5907UVE-3.1/NOPB	DSBGA	YKE	4	250	203.0	190.0	41.0
LP5907UVE-3.3/NOPB	DSBGA	YKE	4	250	203.0	190.0	41.0
LP5907UVE-4.5/NOPB	DSBGA	YKE	4	250	203.0	190.0	41.0
LP5907UVX-1.2/NOPB	DSBGA	YKE	4	3000	206.0	191.0	90.0
LP5907UVX-1.8/NOPB	DSBGA	YKE	4	3000	206.0	191.0	90.0
LP5907UVX-2.8/NOPB	DSBGA	YKE	4	3000	206.0	191.0	90.0
LP5907UVX-2.85/NOPB	DSBGA	YKE	4	3000	206.0	191.0	90.0
LP5907UVX-3.0/NOPB	DSBGA	YKE	4	3000	206.0	191.0	90.0
LP5907UVX-3.1/NOPB	DSBGA	YKE	4	3000	206.0	191.0	90.0
LP5907UVX-3.3/NOPB	DSBGA	YKE	4	3000	206.0	191.0	90.0
LP5907UVX-4.5/NOPB	DSBGA	YKE	4	3000	206.0	191.0	90.0

DBV (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
- D. Falls within JEDEC MO–178 Variation AA.

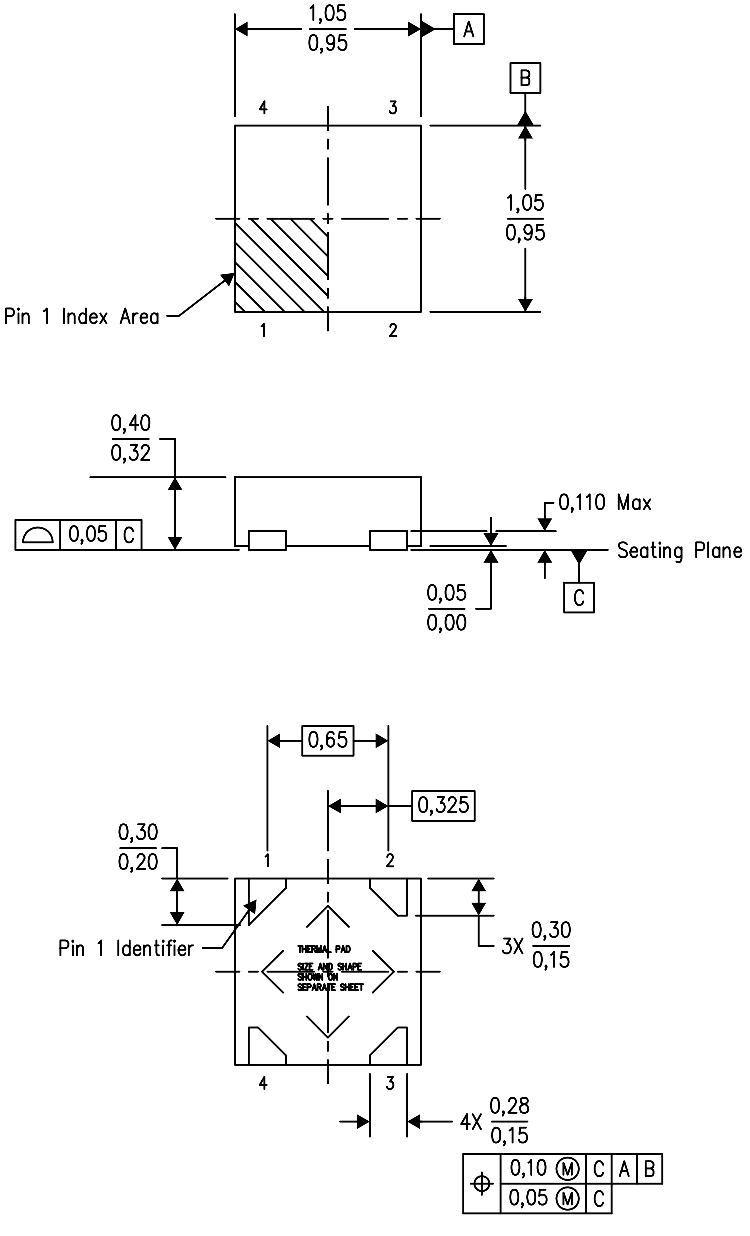
DBV (R–PDSO–G5) PLASTIC SMALL OUTLINE



4209593–3/C 08/11

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
- D. Publication IPC–7351 is recommended for alternate designs.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

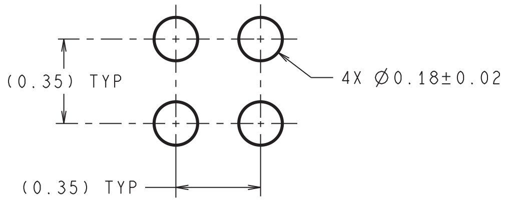
DQN (S–PX2SON–N4) PLASTIC SMALL OUTLINE NO–LEAD



Bottom View

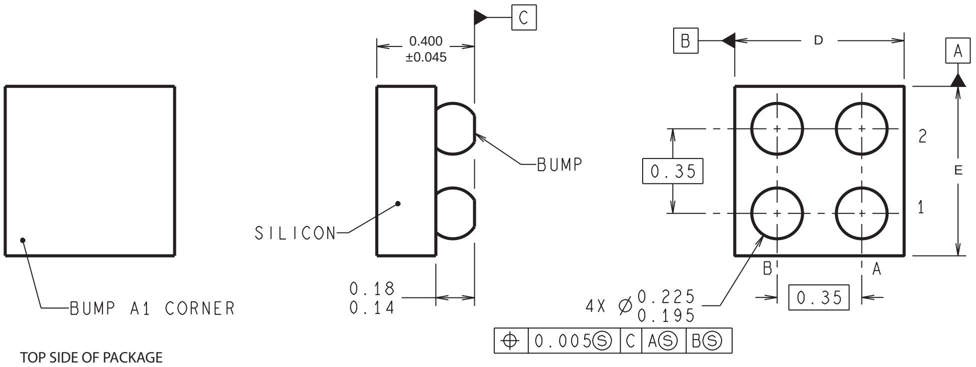
4210367/D 09/2012

NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
- B. This drawing is subject to change without notice.
- C. SON (Small Outline No–Lead) package configuration.
- D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
- E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.



DIMENSIONS ARE IN MILLIMETERS
DIMENSIONS IN ( ) FOR REFERENCE ONLY

LAND PATTERN RECOMMENDATION



TOP SIDE OF PACKAGE

BOTTOM SIDE OF PACKAGE

TLE04XXX (Rev A)

D: Max = 0.695 mm, Min =0.595 mm

E: Max = 0.695 mm, Min =0.595 mm

4215149/A 12/12

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.

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