LPV521 Nanopower, 1.8V, RRIO, CMOS Input, Operational Amplifier

Check for Samples: LPV521

FEATURES

- **(For V_S = 5V, Typical unless otherwise noted)**
- **Supply current at V_{CM} = 0.3V 400 nA (max)**
- **Operating voltage range 1.6V to 5.5V**
- **Low TCV_{OS} 3.5 µV/°C (max)**
- **V_{OS} 1 mV (max)**
- **Input bias current 40 fA**
- **PSRR 109 dB**
- **CMRR 102 dB**
- **Open loop gain 132 dB**
- **Gain bandwidth product 6.2 kHz**
- **Slew rate 2.4 V/ms**
- **Input voltage noise at f = 100 Hz 255 nV/√Hz**
- **Temperature range −40°C to 125°C**

APPLICATIONS

- **Wireless remote sensors**
- **Powerline monitoring**
- **Power meters**
- **Battery powered industrial sensors**
- **Micropower oxygen sensor and gas sensor**
- **Active RFID readers**
- **Zigbee based sensors for HVAC control**
- **Sensor network powered by energy scavenging**

DESCRIPTION

The LPV521 is a single nanopower 552 nW amplifier designed for ultra long life battery applications. The operating voltage range of 1.6V to 5.5V coupled with typically 351 nA of supply current make it well suited for RFID readers and remote sensor nanopower applications. The device has input common mode voltage 0.1V over the rails, guaranteed TCV_{OS} and voltage swing to the rail output performance. The LPV521 has a carefully designed CMOS input stage that outperforms competitors with typically 40 fA I_{BIAS} currents. This low input current significantly reduces I_{BIAS} and I_{OS} errors introduced in megohm resistance, high impedance photodiode, and charge sense situations. The LPV521 is a member of the PowerWise® family and has an exceptional power-to-performance ratio.

The wide input common mode voltage range, guaranteed 1 mV V_{OS} and 3.5 µV/°C TCV_{OS} enables accurate and stable measurement for both high side and low side current sensing.

EMI protection was designed into the device to reduce sensitivity to unwanted RF signals from cell phones or other RFID readers.

The LPV521 is offered in the 5-pin SC70 package.

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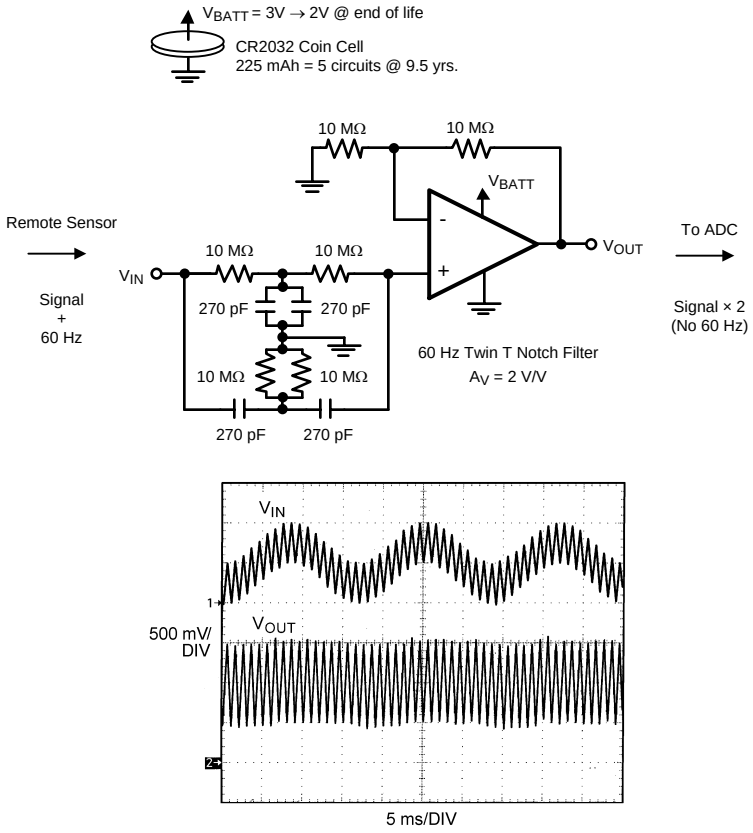
Typical Application



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1)(2)

ESD Tolerance (3)	
Human Body Model	2000V
Machine Model	200V
Charge-Device Model	1000V
Any pin relative to V^-	6V, −0.3V
IN+, IN-, OUT Pins	V^+ + 0.3V, V^- – 0.3V
V^+, V^-, OUT Pins	40mA
Differential Input Voltage (V_{IN+} - V_{IN-})	±300 mV
Storage Temperature Range	−65°C to 150°C
Junction Temperature (4)	150°C
Mounting Temperature	
Infrared or Convection (30 sec.)	260°C
Wave Soldering Lead Temp. (4 sec.)	260°C

(1) Absolute Maximum Ratings indicate limits beyond which damage may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and test conditions, see the Electrical Characteristics.

(2) **If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office / Distributors for availability and specifications.**

(3) Human Body Model, applicable std. MIL-STD-883, Method 3015.7. Machine Model, applicable std. JESD22-A115-A (ESD MM std. of JEDEC)Field-Induced Charge-Device Model, applicable std. JESD22-C101-C (ESD FICDM std. of JEDEC).

(4) The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA}. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} – T_A)/ \theta_{JA}$. All numbers apply for packages soldered directly onto a PC Board.

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Operating Ratings (1)

Temperature Range (2)	−40°C to 125°C
Supply Voltage ($V_S = V^+ - V^-$)	1.6V to 5.5V
Package Thermal Resistance (θ_{JA}) (2)	
5-Pin SC70	456 °C/W

(1) Absolute Maximum Ratings indicate limits beyond which damage may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and test conditions, see the Electrical Characteristics.
(2) The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA}. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} – T_A)/ \theta_{JA}$. All numbers apply for packages soldered directly onto a PC Board.

1.8V DC Electrical Characteristics(1)

Unless otherwise specified, all limits guaranteed for T_A = 25°C, V^+ = 1.8V, V^- = 0V, $V_{CM} = V_O = V^+/2$, and R_L > 1 MΩ. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (2)	Typ (3)	Max (2)	Units
V_{OS}	Input Offset Voltage	V_{CM} = 0.3V		0.1	±1.0 **±1.23**	mV
		V_{CM} = 1.5V		0.1	±1.0 **±1.23**	
TCV_{OS}	Input Offset Voltage Drift (4)			±0.4	**±3**	µV/°C
I_{BIAS}	Input Bias Current			0.01	±1 **±50**	pA
I_{OS}	Input Offset Current			10		fA
CMRR	Common Mode Rejection Ratio	0V ≤ V_{CM} ≤ 1.8V	66 **60**	92		dB
		0V ≤ V_{CM} ≤ 0.7V	75 **74**	101		
		1.2V ≤ V_{CM} ≤ 1.8V	75 **53**	120		
PSRR	Power Supply Rejection Ratio	1.6V ≤ V^+ ≤ 5.5V V_{CM} = 0.3V	85 **76**	109		dB
CMVR	Common Mode Voltage Range	CMRR ≥ 67 dB CMRR ≥ 60 dB	0 **0**		1.8 **1.8**	V
A_{VOL}	Large Signal Voltage Gain	V_O = 0.5V to 1.3V R_L = 100 kΩ to $V^+/2$	74 **73**	125		dB
V_O	Output Swing High	R_L = 100 kΩ to $V^+/2$ V_{IN}(diff) = 100 mV		2	50 **50**	mV from either rail
	Output Swing Low	R_L = 100 kΩ to $V^+/2$ V_{IN}(diff) = −100 mV		2	50 **50**	
I_O	Output Current (5)	Sourcing, V_O to V^- V_{IN}(diff) = 100 mV	1 **0.5**	3		mA
		Sinking, V_O to V^+ V_{IN}(diff) = −100 mV	1 **0.5**	3		

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that $T_J = T_A$. No guarantee of parametric performance is indicated in the electrical tables under conditions of internal self-heating where $T_J > T_A$. Absolute Maximum Ratings indicate junction temperature limits beyond which the device may be permanently degraded, either mechanically or electrically.
(2) All limits are guaranteed by testing, statistical analysis or design.
(3) Typical values represent the most likely parametric norm at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not guaranteed on shipped production material.
(4) The offset voltage average drift is determined by dividing the change in V_{OS} at the temperature extremes by the total temperature change.
(5) The short circuit test is a momentary open loop test.

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1.8V DC Electrical Characteristics[1] (continued)

Unless otherwise specified, all limits guaranteed for T_A = 25°C, V^+ = 1.8V, V^- = 0V, V_{CM} = V_O = V^+/2, and R_L > 1 MΩ. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min [2]	Typ [3]	Max [2]	Units
I_S	Supply Current	V_{CM} = 0.3V		345	400 **580**	nA
		V_{CM} = 1.5V		472	600 **850**	

1.8V AC Electrical Characteristics[1]

Unless otherwise specified, all limits guaranteed for T_A = 25°C, V^+ = 1.8V, V^- = 0V, V_{CM} = V_O = V^+/2, and R_L > 1 MΩ. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions		Min [2]	Typ [3]	Max [2]	Units
GBW	Gain-Bandwidth Product	C_L = 20 pF, R_L = 100 kΩ			6.1		kHz
SR	Slew Rate	A_V = +1, V_{IN} = 0V to 1.8V	Falling Edge		2.9		V/ms
			Rising Edge		2.3		
θ_m	Phase Margin	C_L = 20 pF, R_L = 100 kΩ			72		deg
G_m	Gain Margin	C_L = 20 pF, R_L = 100 kΩ			19		dB
e_n	Input-Referred Voltage Noise Density	f = 100 Hz			265		nV/√Hz
	Input-Referred Voltage Noise	0.1 Hz to 10 Hz			24		μV_{PP}
i_n	Input-Referred Current Noise	f = 100 Hz			100		fA/√Hz

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that T_J = T_A. No guarantee of parametric performance is indicated in the electrical tables under conditions of internal self-heating where T_J > T_A. Absolute Maximum Ratings indicate junction temperature limits beyond which the device may be permanently degraded, either mechanically or electrically.
(2) All limits are guaranteed by testing, statistical analysis or design.
(3) Typical values represent the most likely parametric norm at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not guaranteed on shipped production material.

3.3V DC Electrical Characteristics[1]

Unless otherwise specified, all limits guaranteed for T_A = 25°C, V^+ = 3.3V, V^- = 0V, V_{CM} = V_O = V^+/2, and R_L > 1 MΩ. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min [2]	Typ [3]	Max [2]	Units
V_{OS}	Input Offset Voltage	V_{CM} = 0.3V		0.1	±1.0 **±1.23**	mV
		V_{CM} = 3V		0.1	±1.0 **±1.23**	
TCV_{OS}	Input Offset Voltage Drift [4]			±0.4	**±3**	µV/°C
I_{BIAS}	Input Bias Current			0.01	±1 **±50**	pA
I_{OS}	Input Offset Current			20		fA

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that T_J = T_A. No guarantee of parametric performance is indicated in the electrical tables under conditions of internal self-heating where T_J > T_A. Absolute Maximum Ratings indicate junction temperature limits beyond which the device may be permanently degraded, either mechanically or electrically.
(2) All limits are guaranteed by testing, statistical analysis or design.
(3) Typical values represent the most likely parametric norm at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not guaranteed on shipped production material.
(4) The offset voltage average drift is determined by dividing the change in V_{OS} at the temperature extremes by the total temperature change.

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3.3V DC Electrical Characteristics[1] (continued)

Unless otherwise specified, all limits guaranteed for T_A = 25°C, V^+ = 3.3V, V^- = 0V, $V_{CM} = V_O = V^+/2$, and R_L > 1 MΩ. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min [2]	Typ [3]	Max [2]	Units
CMRR	Common Mode Rejection Ratio	0V ≤ V_{CM} ≤ 3.3V	72 **70**	97		dB
		0V ≤ V_{CM} ≤ 2.2V	78 **75**	106		
		2.7V ≤ V_{CM} ≤ 3.3V	77 **76**	121		
PSRR	Power Supply Rejection Ratio	1.6V ≤ V^+ ≤ 5.5V V_{CM} = 0.3V	85 **76**	109		dB
CMVR	Common Mode Voltage Range	CMRR ≥ 72 dB CMRR ≥ 70 dB	−0.1 **0**		3.4 **3.3**	V
A_{VOL}	Large Signal Voltage Gain	V_O = 0.5V to 2.8V R_L = 100 kΩ to $V^+/2$	82 **76**	120		dB
V_O	Output Swing High	R_L = 100 kΩ to $V^+/2$ V_{IN}(diff) = 100 mV		3	50 **50**	mV from either rail
	Output Swing Low	R_L = 100 kΩ to $V^+/2$ V_{IN}(diff) = −100 mV		2	50 **50**	
I_O	Output Current [5]	Sourcing, V_O to V^- V_{IN}(diff) = 100 mV	5 **4**	11		mA
		Sinking, V_O to V^+ V_{IN}(diff) = −100 mV	5 **4**	12		
I_S	Supply Current	V_{CM} = 0.3V		346	400 **600**	nA
		V_{CM} = 3V		471	600 **860**	

(5) The short circuit test is a momentary open loop test.

3.3V AC Electrical Characteristics[1]

Unless otherwise is specified, all limits guaranteed for T_A = 25°C, V^+ = 3.3V, V^- = 0V, $V_{CM} = V_O = V^+/2$, and R_L > 1 MΩ. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions		Min [2]	Typ [3]	Max [2]	Units
GBW	Gain-Bandwidth Product	C_L = 20 pF, R_L = 100 kΩ			6.2		kHz
SR	Slew Rate	A_V = +1, V_{IN} = 0V to 3.3V	Falling Edge		2.9		V/ms
			Rising Edge		2.5		
θ_m	Phase Margin	C_L = 20 pF, R_L = 10 kΩ			73		deg
G_m	Gain Margin	C_L = 20 pF, R_L = 10 kΩ			19		dB
e_n	Input-Referred Voltage Noise Density	f = 100 Hz			259		$nV/\sqrt{Hz}$
	Input-Referred Voltage Noise	0.1 Hz to 10 Hz			22		μV_{PP}
i_n	Input-Referred Current Noise	f = 100 Hz			100		$fA/\sqrt{Hz}$

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that $T_J = T_A$. No guarantee of parametric performance is indicated in the electrical tables under conditions of internal self-heating where $T_J > T_A$. Absolute Maximum Ratings indicate junction temperature limits beyond which the device may be permanently degraded, either mechanically or electrically.
(2) All limits are guaranteed by testing, statistical analysis or design.
(3) Typical values represent the most likely parametric norm at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not guaranteed on shipped production material.

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5V DC Electrical Characteristics(1)

Unless otherwise specified, all limits guaranteed for T_A = 25°C, V^+ = 5V, V^- = 0V, V_{CM} = V_O = $V^+/2$, and R_L > 1MΩ. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (2)	Typ (3)	Max (2)	Units
V_{OS}	Input Offset Voltage	V_{CM} = 0.3V		0.1	±1.0 **±1.23**	mV
		V_{CM} = 4.7V		0.1	±1.0 **±1.23**	
TCV_{OS}	Input Offset Voltage Drift (4)			±0.4	**±3.5**	µV/°C
I_{BIAS}	Input Bias Current			0.04	±1 **±50**	pA
I_{OS}	Input Offset Current			60		fA
CMRR	Common Mode Rejection Ratio	0V ≤ V_{CM} ≤ 5.0V	75 **74**	102		dB
		0V ≤ V_{CM} ≤ 3.9V	84 **80**	108		
		4.4V ≤ V_{CM} ≤ 5.0V	77 **76**	115		
PSRR	Power Supply Rejection Ratio	1.6V ≤ V^+ ≤ 5.5V V_{CM} = 0.3V	85 **76**	109		dB
CMVR	Common Mode Voltage Range	CMRR ≥ 75 dB CMRR ≥ 74 dB	−0.1 **0**		5.1 **5**	V
A_{VOL}	Large Signal Voltage Gain	V_O = 0.5V to 4.5V R_L = 100 kΩ to $V^+/2$	84 **76**	132		dB
V_O	Output Swing High	R_L = 100 kΩ to $V^+/2$ V_{IN}(diff) = 100 mV		3	50 **50**	mV from either rail
	Output Swing Low	R_L = 100 kΩ to $V^+/2$ V_{IN} (diff) = −100 mV		3	50 **50**	
I_O	Output Current (5)	Sourcing, V_O to V^- V_{IN}(diff) = 100 mV	15 **8**	23		mA
		Sinking, V_O to V^+ V_{IN}(diff) = −100 mV	15 **8**	22		
I_S	Supply Current	V_{CM} = 0.3V		351	400 **620**	nA
		V_{CM} = 4.7V		475	600 **870**	

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that T_J = T_A. No guarantee of parametric performance is indicated in the electrical tables under conditions of internal self-heating where T_J > T_A. Absolute Maximum Ratings indicate junction temperature limits beyond which the device may be permanently degraded, either mechanically or electrically.
(2) All limits are guaranteed by testing, statistical analysis or design.
(3) Typical values represent the most likely parametric norm at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not guaranteed on shipped production material.
(4) The offset voltage average drift is determined by dividing the change in V_{OS} at the temperature extremes by the total temperature change.
(5) The short circuit test is a momentary open loop test.

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5V AC Electrical Characteristics[1]

Unless otherwise specified, all limits guaranteed for T_A = 25°C, V^+ = 5V, V^- = 0V, V_{CM} = V_O = V^+/2, and R_L > 1MΩ. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions		Min [2]	Typ [3]	Max [2]	Units
GBW	Gain-Bandwidth Product	C_L = 20 pF, R_L = 100 kΩ			6.2		kHz
SR	Slew Rate	A_V = +1, V_{IN} = 0V to 5V	Falling Edge	1.1 **1.2**	2.7		V/ms
			Rising Edge	1.1 **1.2**	2.4		
θ_m	Phase Margin	C_L = 20 pF, R_L = 100 kΩ			73		deg
G_m	Gain Margin	C_L = 20 pF, R_L = 100 kΩ			20		dB
e_n	Input-Referred Voltage Noise Density	f = 100 Hz			255		$nV/\sqrt{Hz}$
	Input-Referred Voltage Noise	0.1 Hz to 10 Hz			22		μV_{PP}
i_n	Input-Referred Current Noise	f = 100 Hz			100		$fA/\sqrt{Hz}$
EMIRR	EMI Rejection Ratio, IN+ and IN− [4]	V_{RF_PEAK} = 100 mV_P (−20 dB_P), f = 400 MHz			121		dB
		V_{RF_PEAK} = 100 mV_P (−20 dB_P), f = 900 MHz			121		
		V_{RF_PEAK} = 100 mV_P (−20 dB_P), f = 1800 MHz			124		
		V_{RF_PEAK} = 100 mV_P (−20 dB_P), f = 2400 MHz			142		

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that T_J = T_A. No guarantee of parametric performance is indicated in the electrical tables under conditions of internal self-heating where T_J > T_A. Absolute Maximum Ratings indicate junction temperature limits beyond which the device may be permanently degraded, either mechanically or electrically.
(2) All limits are guaranteed by testing, statistical analysis or design.
(3) Typical values represent the most likely parametric norm at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not guaranteed on shipped production material.
(4) The EMI Rejection Ratio is defined as EMIRR = 20log ($V_{RF\_PEAK}/\Delta V_{OS}$).

CONNECTION DIAGRAM

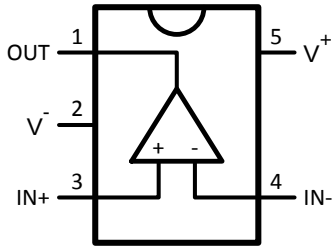

Figure 1. 5-Pin SC70
Top View

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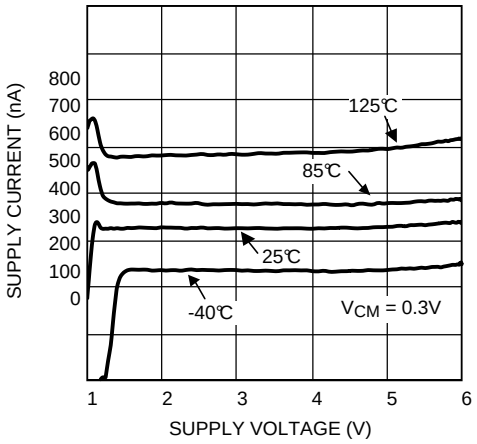
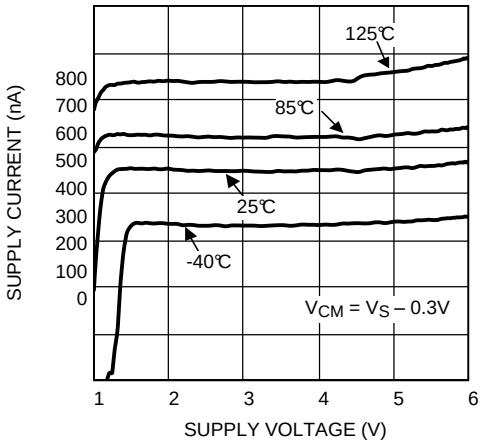
TYPICAL PERFORMANCE CHARACTERISTICS

At T_J = 25°C, unless otherwise specified.

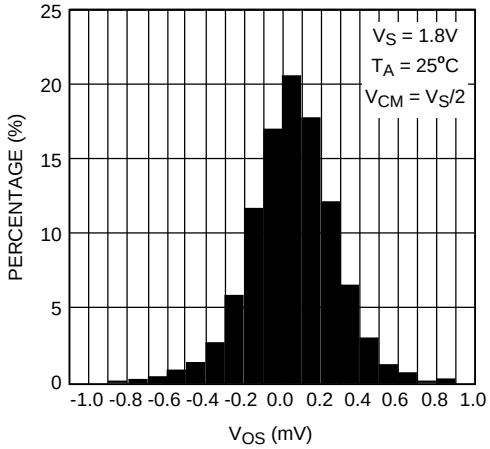
Supply Current vs. Supply Voltage



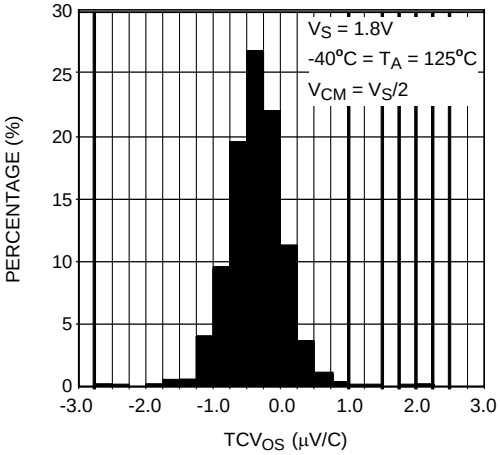
Supply Current vs. Supply Voltage



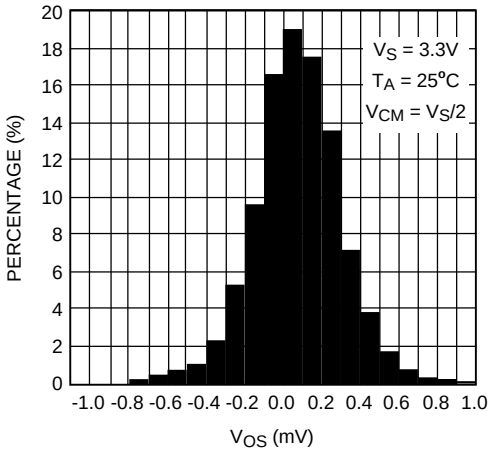
Offset Voltage Distribution



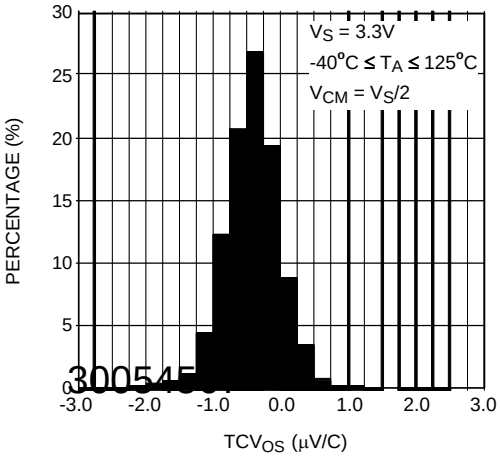
TCV_{OS} Distribution



Offset Voltage Distribution



TCV_{OS} Distribution



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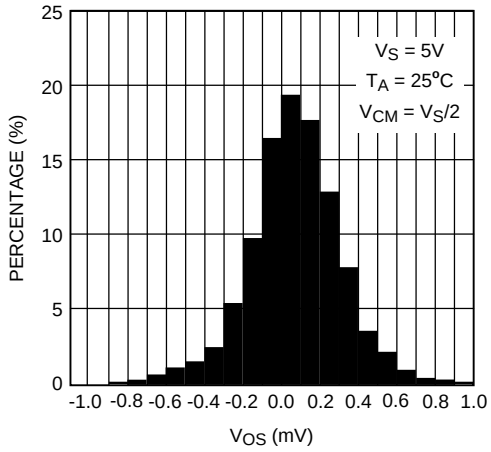
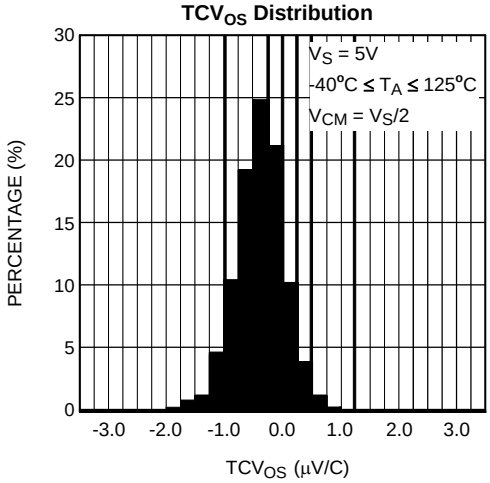
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

At T_J = 25°C, unless otherwise specified.

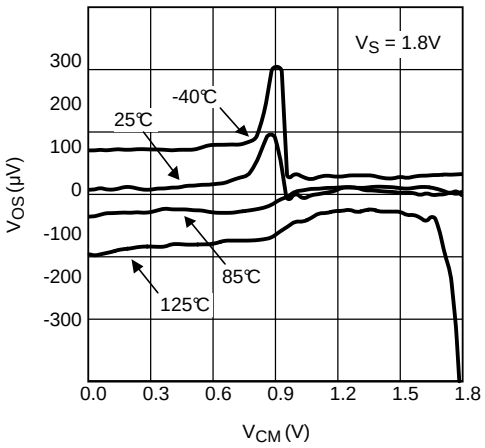
Offset Voltage Distribution



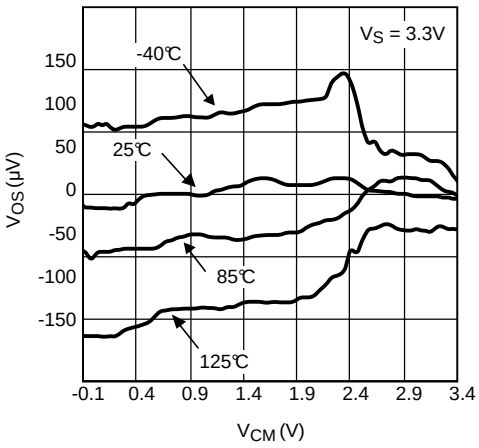
TCV_{OS} Distribution



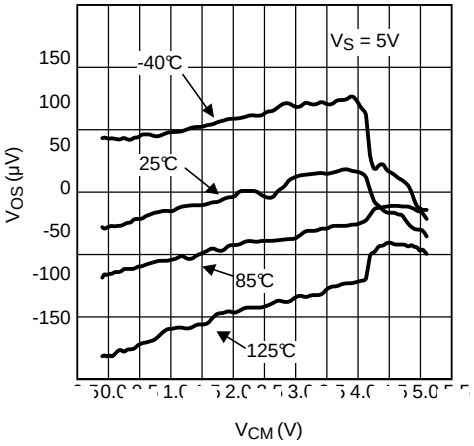
Input Offset Voltage vs. Input Common Mode



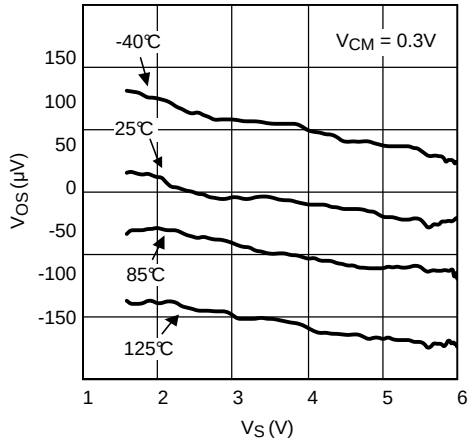
Input Offset Voltage vs. Input Common Mode



Input Offset Voltage vs. Input Common Mode



Input Offset Voltage vs. Supply Voltage



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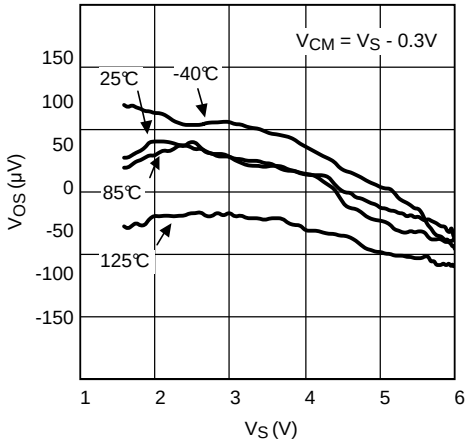
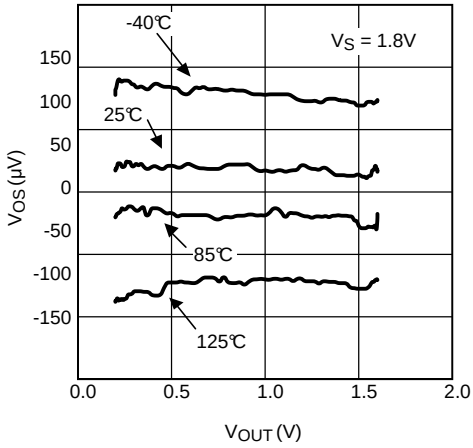
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

At T_J = 25°C, unless otherwise specified.

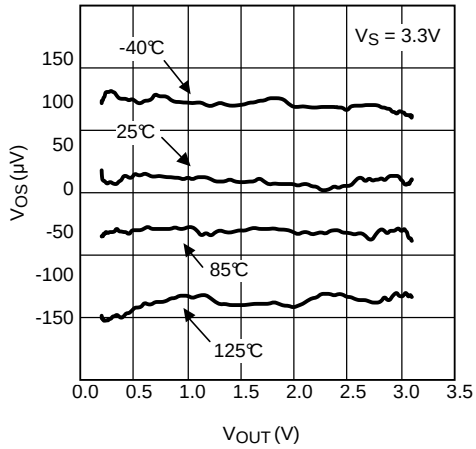
Input Offset Voltage vs. Supply Voltage



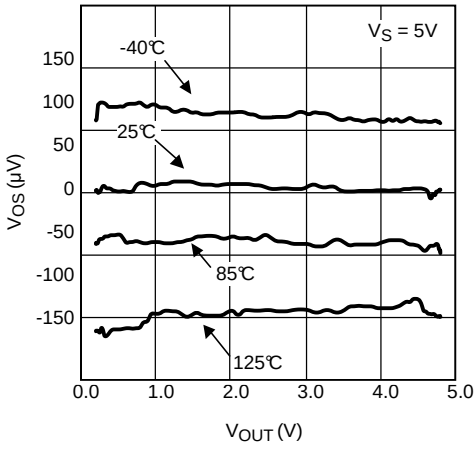
Input Offset Voltage vs. Output Voltage



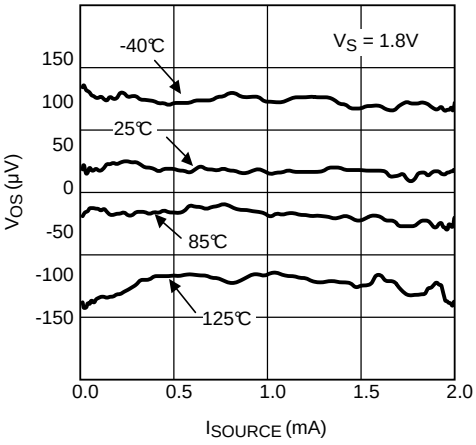
Input Offset Voltage vs. Output Voltage



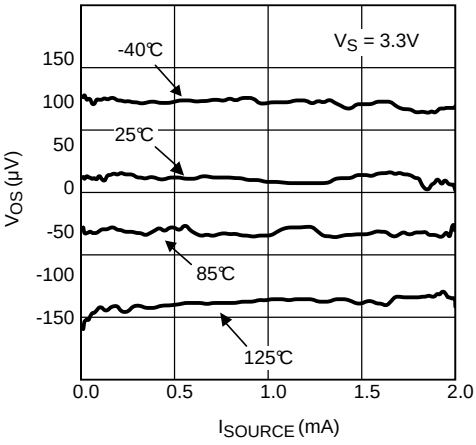
Input Offset Voltage vs. Output Voltage



Input Offset Voltage vs. Sourcing Current



Input Offset Voltage vs. Sourcing Current



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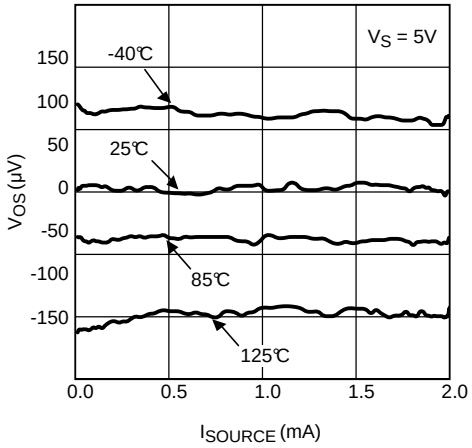
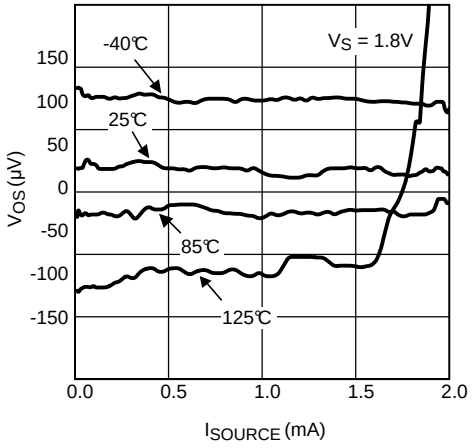
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

At T_J = 25°C, unless otherwise specified.

Input Offset Voltage vs. Sourcing Current



Input Offset Voltage vs. Sinking Current



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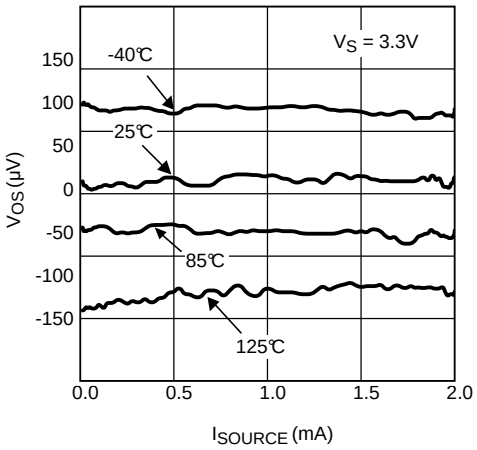

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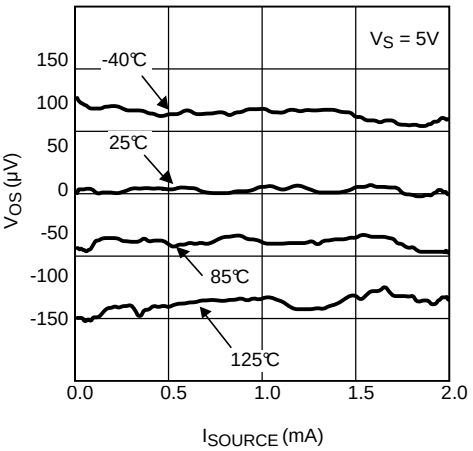
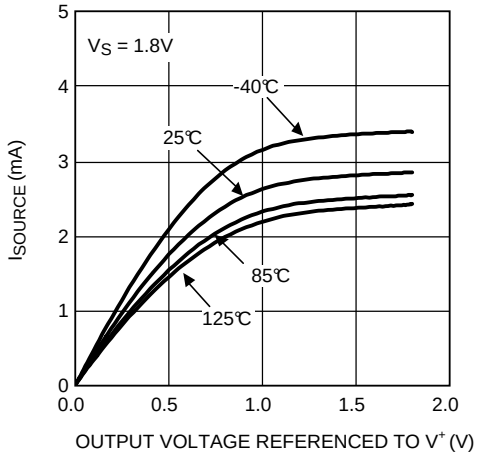
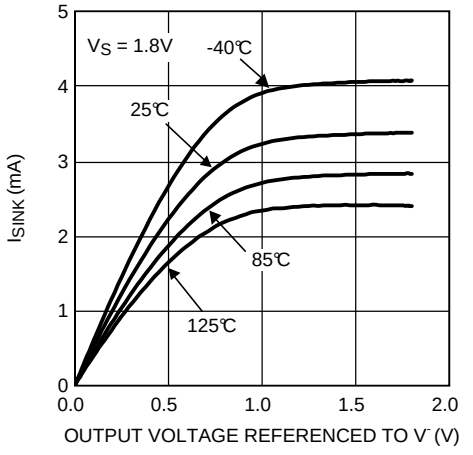


Sourcing Current vs. Output Voltage



Sinking Current vs. Output Voltage



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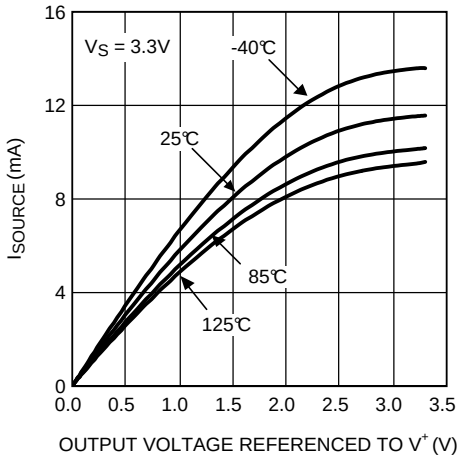
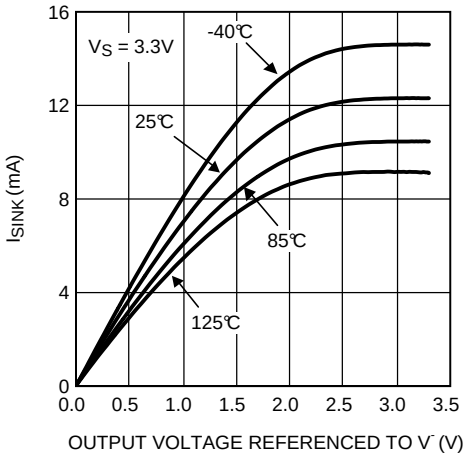
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

At T_J = 25°C, unless otherwise specified.

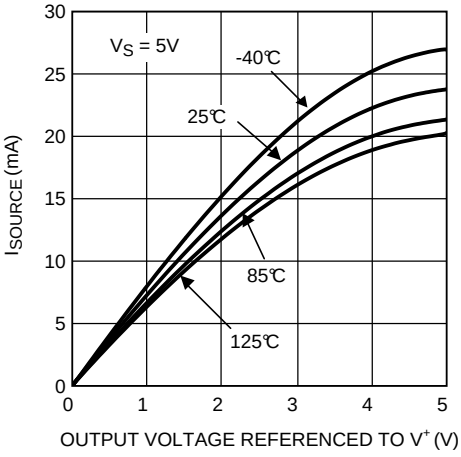
Sourcing Current vs. Output Voltage



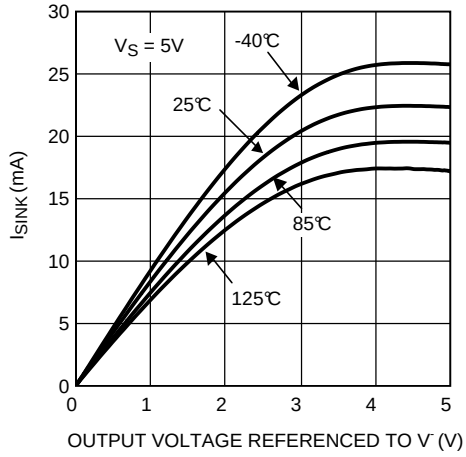
Sinking Current vs. Output Voltage



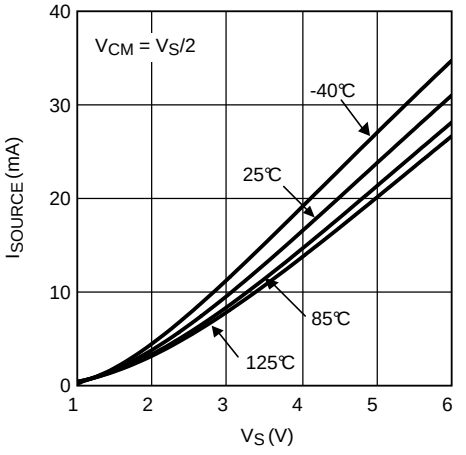
Sourcing Current vs. Output Voltage



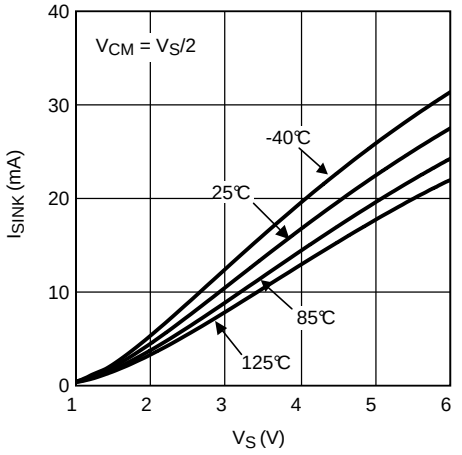
Sinking Current vs. Output Voltage



Sourcing Current vs. Supply Voltage



Sinking Current vs. Supply Voltage



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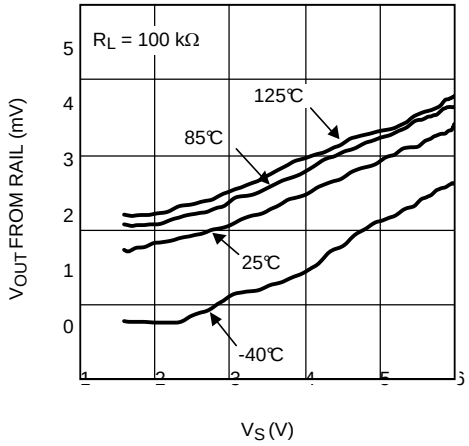
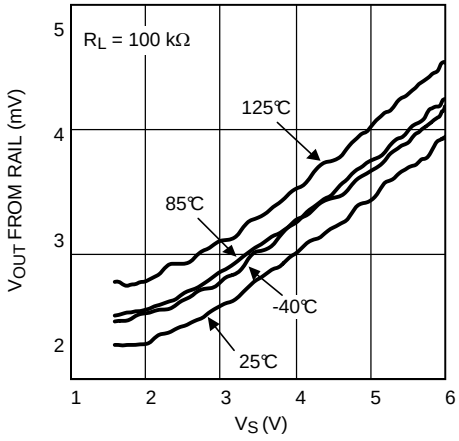
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

At T_J = 25°C, unless otherwise specified.

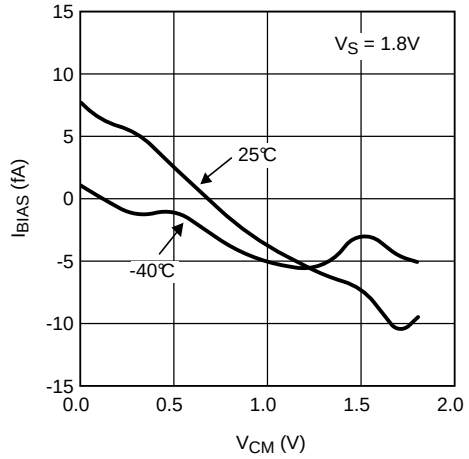
Output Swing High vs. Supply Voltage



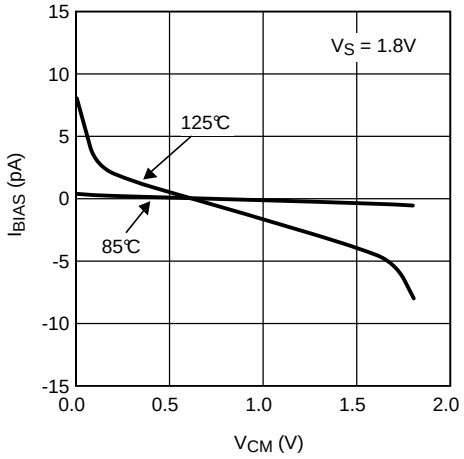
Output Swing Low vs. Supply Voltage



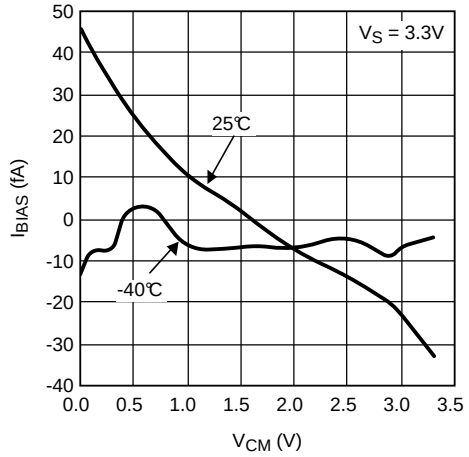
Input Bias Current vs. Common Mode Voltage



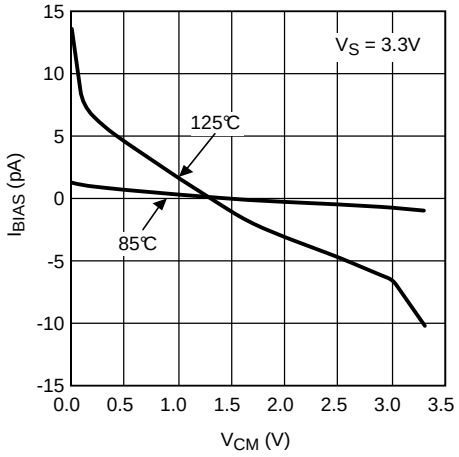
Input Bias Current vs. Common Mode Voltage



Input Bias Current vs. Common Mode Voltage



Input Bias Current vs. Common Mode Voltage



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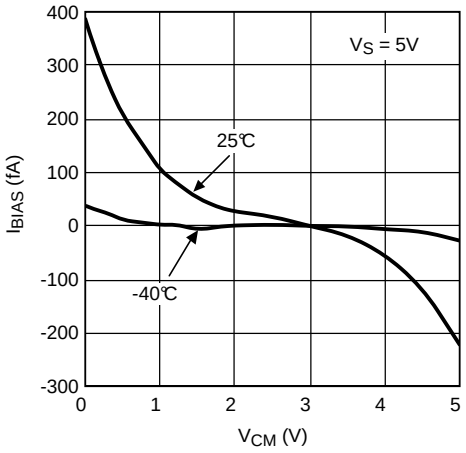
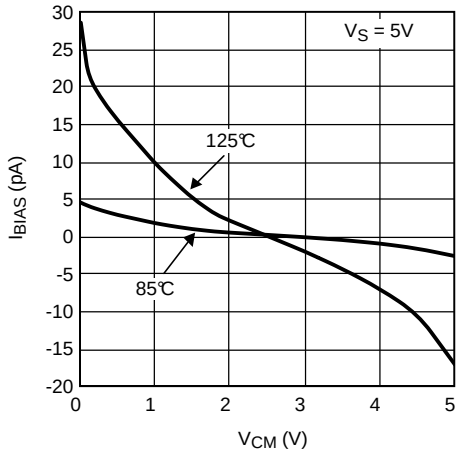
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

At T_J = 25°C, unless otherwise specified.

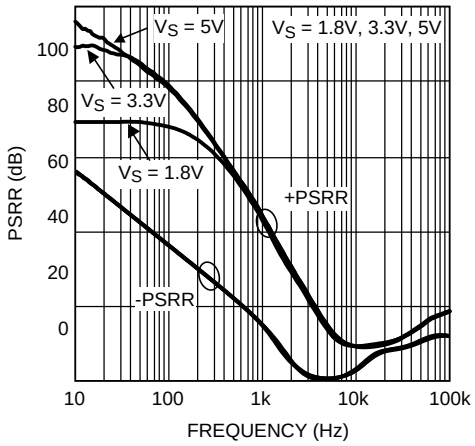
Input Bias Current vs. Common Mode Voltage



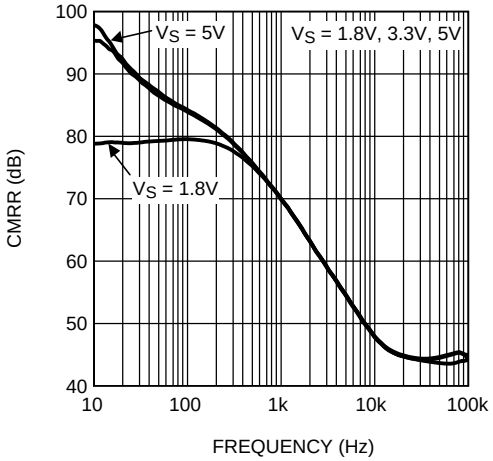
Input Bias Current vs. Common Mode Voltage



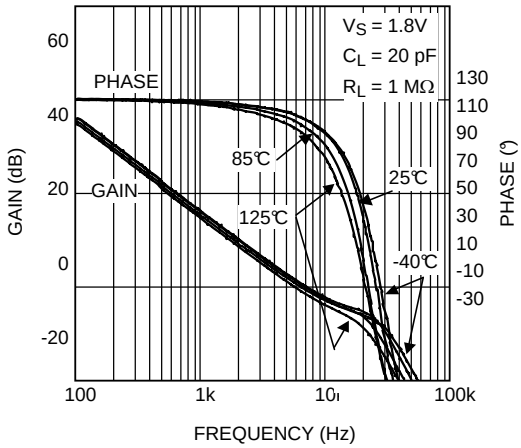
PSRR vs. Frequency



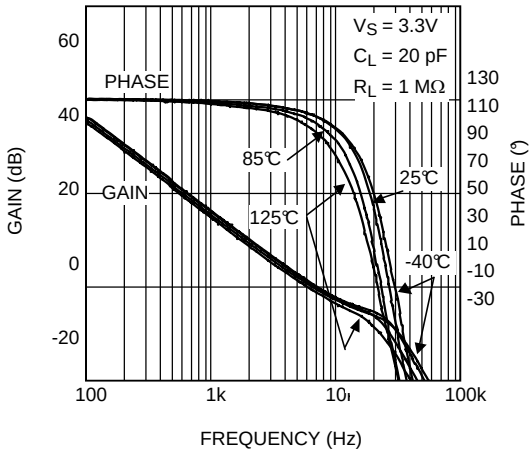
CMRR vs. Frequency



Frequency Response vs. Temperature



Frequency Response vs. Temperature



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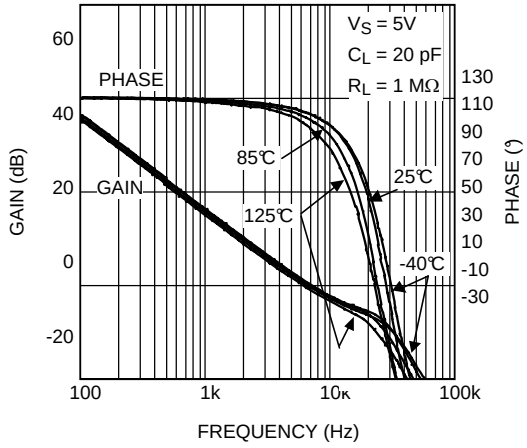
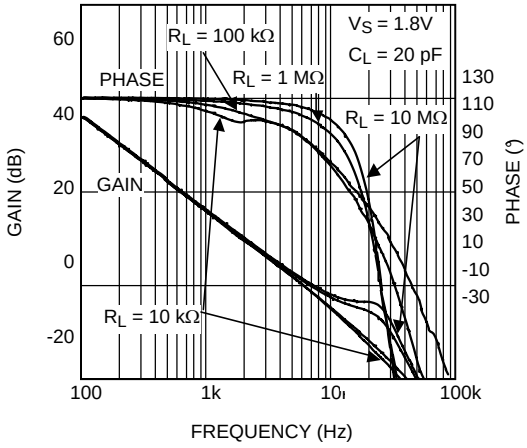
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

At T_J = 25°C, unless otherwise specified.

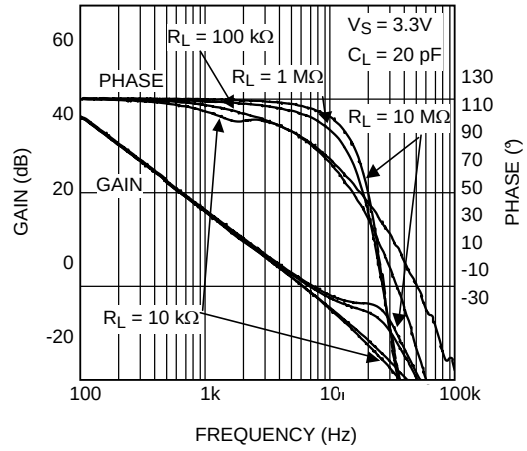
Frequency Response vs. Temperature



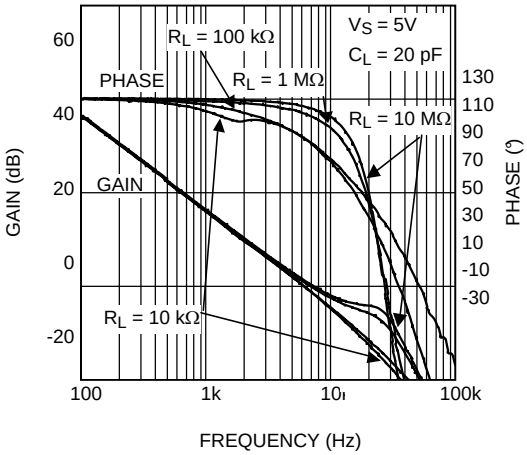
Frequency Response vs. R_L



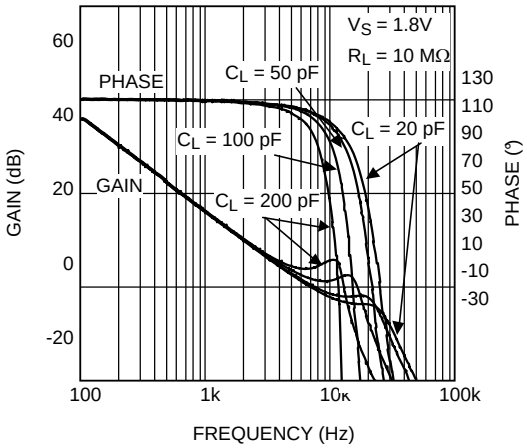
Frequency Response vs. R_L



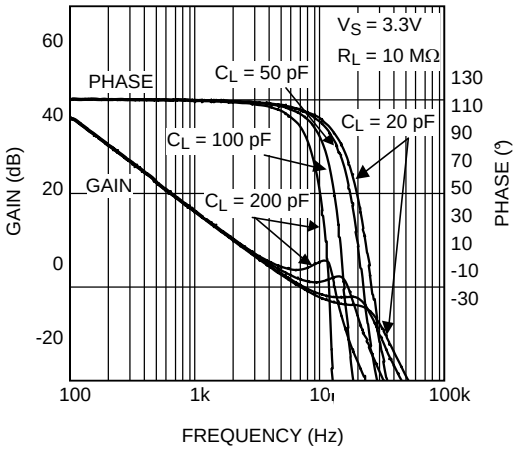
Frequency Response vs. R_L



Frequency Response vs. C_L



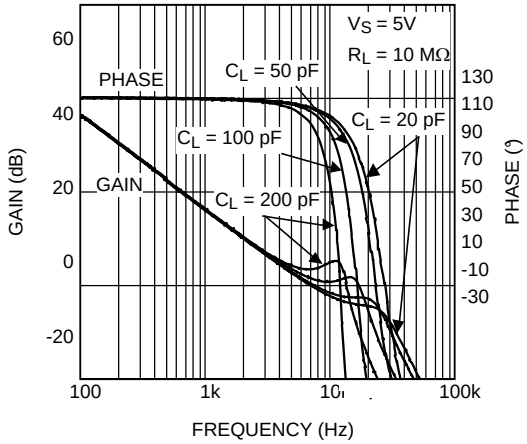
Frequency Response vs. C_L



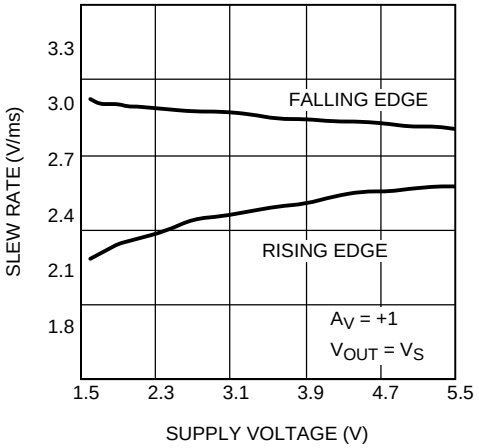
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

At T_J = 25°C, unless otherwise specified.

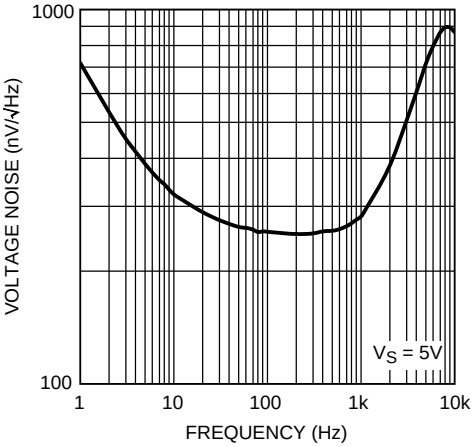
Frequency Response vs. C_L



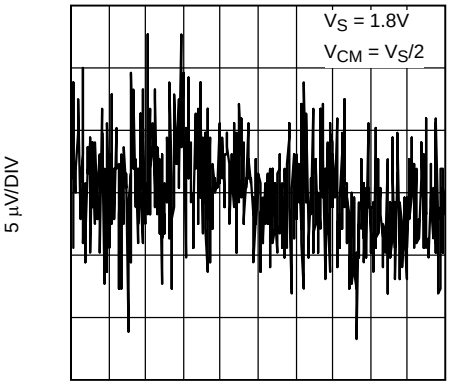
Slew Rate vs. Supply Voltage



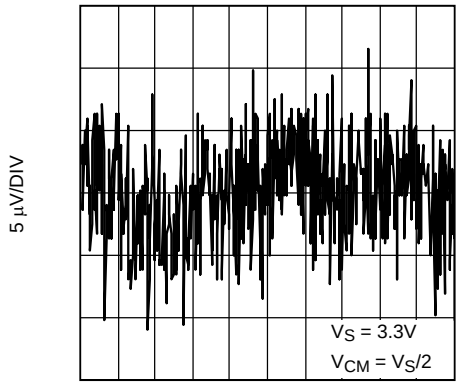
Voltage Noise vs. Frequency



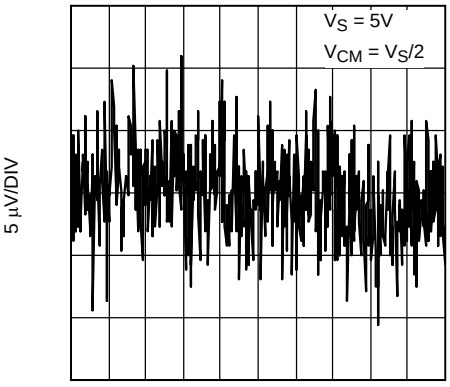
0.1 to 10 Hz Time Domain Voltage Noise



0.1 to 10 Hz Time Domain Voltage Noise



0.1 to 10 Hz Time Domain Voltage Noise



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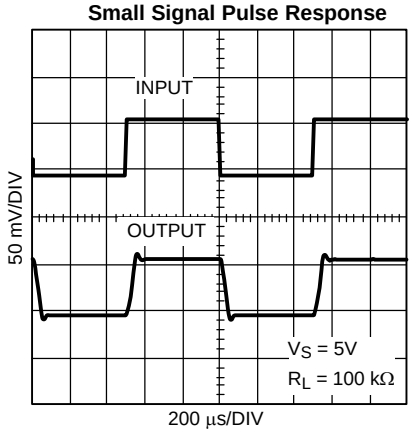
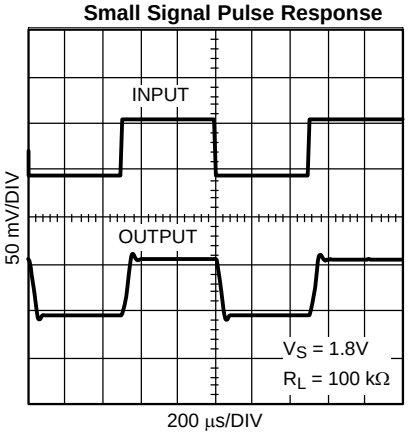
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

At T_J = 25°C, unless otherwise specified.

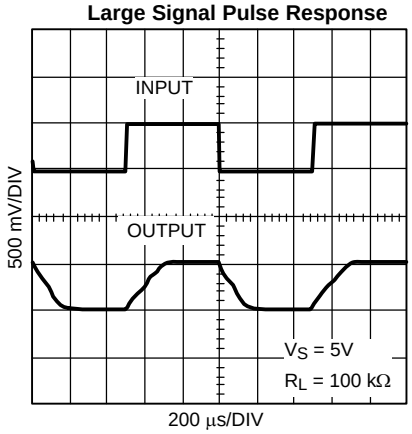
Small Signal Pulse Response



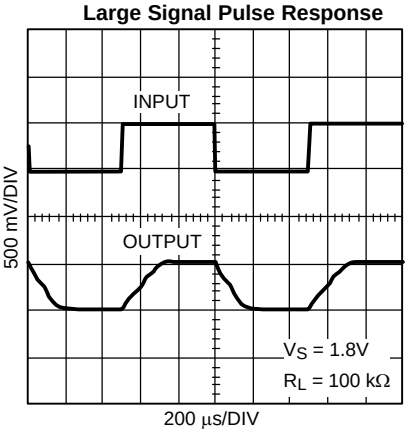
Small Signal Pulse Response



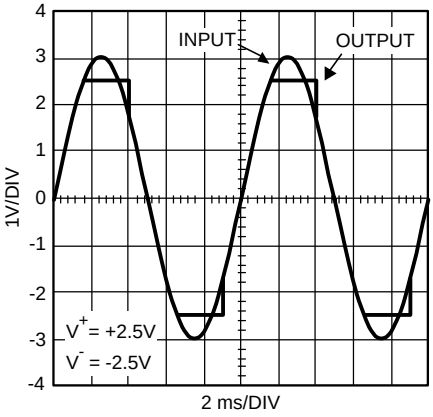
Large Signal Pulse Response



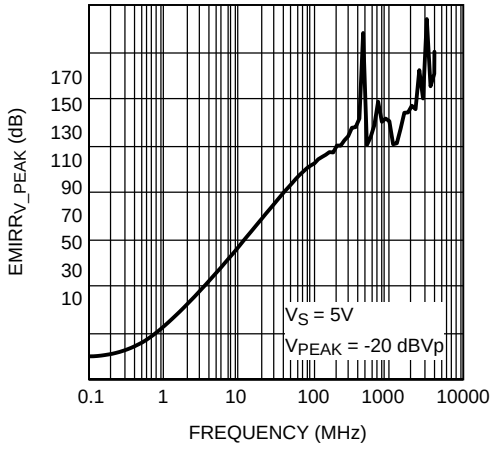
Large Signal Pulse Response



Overload Recovery Waveform



EMIRR vs. Frequency



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APPLICATION INFORMATION

The LPV521 is fabricated with National Semiconductor's state-of-the-art VIP50 process. This proprietary process dramatically improves the performance of National Semiconductor's low-power and low-voltage operational amplifiers. The following sections showcase the advantages of the VIP50 process and highlight circuits which enable ultra-low power consumption.

60 HZ TWIN T NOTCH FILTER

Small signals from transducers in remote and distributed sensing applications commonly suffer strong 60 Hz interference from AC power lines. The circuit of Figure 2 notches out the 60 Hz and provides a gain A_V = 2 for the sensor signal represented by a 1 kHz sine wave. Similar stages may be cascaded to remove 2nd and 3rd harmonics of 60 Hz. Thanks to the nA power consumption of the LPV521, even 5 such circuits can run for 9.5 years from a small CR2032 lithium cell. These batteries have a nominal voltage of 3V and an end of life voltage of 2V. With an operating voltage from 1.6V to 5.5V the LPV521 can function over this voltage range.

The notch frequency is set by $F_0 = 1/2\pi RC$. To achieve a 60 Hz notch use R = 10 MΩ and C = 270 pF. If eliminating 50 Hz noise, which is common in European systems, use R = 11.8 MΩ and C = 270 pF.

The Twin T Notch Filter works by having two separate paths from V_{IN} to the amplifier's input. A low frequency path through the resistors R - R and another separate high frequency path through the capacitors C - C. However, at frequencies around the notch frequency, the two paths have opposing phase angles and the two signals will tend to cancel at the amplifier's input.

To ensure that the target center frequency is achieved and to maximize the notch depth (Q factor) the filter needs to be as balanced as possible. To obtain circuit balance, while overcoming limitations of available standard resistor and capacitor values, use passives in parallel to achieve the 2C and R/2 circuit requirements for the filter components that connect to ground.

To make sure passive component values stay as expected clean board with alcohol, rinse with deionized water, and air dry. Make sure board remains in a relatively low humidity environment to minimize moisture which may increase the conductivity of board components. Also large resistors come with considerable parasitic stray capacitance which effects can be reduced by cutting out the ground plane below components of concern.

Large resistors are used in the feedback network to minimize battery drain. When designing with large resistors, resistor thermal noise, op amp current noise, as well as op amp voltage noise, must be considered in the noise analysis of the circuit. The noise analysis for the circuit in Figure 2 can be done over a bandwidth of 5 kHz, which takes the conservative approach of overestimating the bandwidth (LPV521 typical GBW/A_V is lower). The total noise at the output is approximately 800 µVpp, which is excellent considering the total consumption of the circuit is only 540 nA. The dominant noise terms are op amp voltage noise (550 µVpp), current noise through the feedback network (430 µVpp), and current noise through the notch filter network (280 µVpp). Thus the total circuit's noise is below 1/2 LSB of a 10 bit system with a 2 V reference, which is 1 mV.

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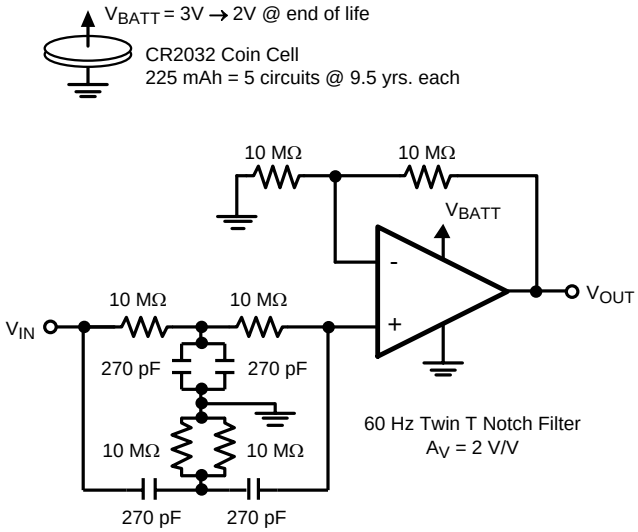

Figure 2. 60 Hz Notch Filter

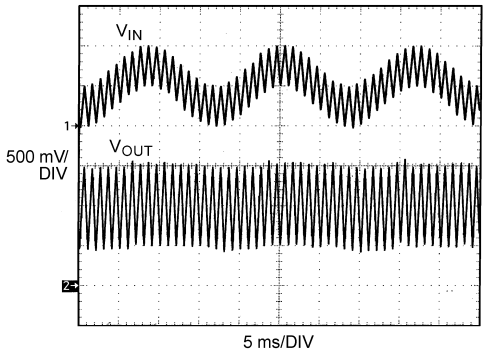

Figure 3. 60 Hz Notch Filter Waveform

BATTERY CURRENT SENSING

The rail-to-rail common mode input range and the very low quiescent current make the LPV521 ideal to use in high side and low side battery current sensing applications. The high side current sensing circuit in Figure 4 is commonly used in a battery charger to monitor the charging current in order to prevent over charging. A sense resistor R_{SENSE} is connected in series with the battery. The theoretical output voltage of the circuit is V_{OUT} = [(R_{SENSE} × R_3) / R_1] × I_{CHARGE}. In reality, however, due to the finite Current Gain, β, of the transistor the current that travels through R_3 will not be I_{CHARGE}, but instead, will be α × I_{CHARGE} or β/(β+1) × I_{CHARGE}. A Darlington pair can be used to increase the β and performance of the measuring circuit. Using the components shown in Figure 4 will result in V_{OUT} ≈ 4000 Ω × I_{CHARGE}. This is ideal to amplify a 1 mA I_{CHARGE} to near full scale of an ADC with V_{REF} at 4.1V. A resistor, R2 is used at the non-inverting input of the amplifier, with the same value as R1 to minimize offset voltage. Selecting values per Figure 4 will limit the current traveling through the R_1 – Q1 – R_3 leg of the circuit to under 1 µA which is on the same order as the LPV521 supply current. Increasing resistors R_1 , R_2 , and R_3 will decrease the measuring circuit supply current and extend battery life. Decreasing R_{SENSE} will minimize error due to resistor tolerance, however, this will also decrease V_{SENSE} = I_{CHARGE} × R_{SENSE}, and in turn the amplifier offset voltage will have a more significant contribution to the total error of the circuit. With the components shown in Figure 4 the measurement circuit supply current can be kept below 1.5 µA and measure 100 µA to 1 mA..

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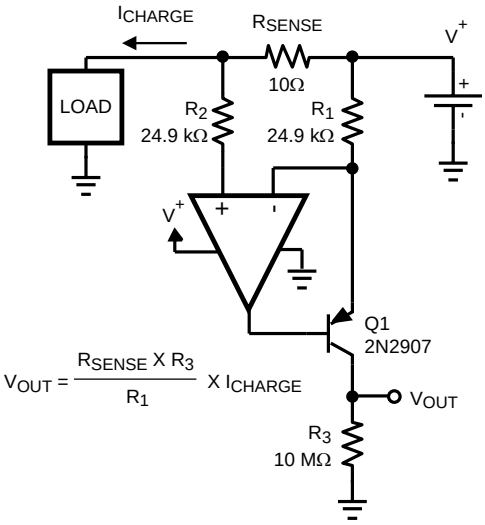

Figure 4. High Side Current Sensing

PORTABLE GAS DETECTION SENSOR

Gas sensors are used in many different industrial and medical applications. They generate a current which is proportional to the percentage of a particular gas sensed in an air sample. This current goes through a load resistor and the resulting voltage drop is measured. Depending on the sensed gas and sensitivity of the sensor, the output current can be in the order of tens of microamperes to a few milliamperes. Gas sensor datasheets often specify a recommended load resistor value or they suggest a range of load resistors to choose from.

Oxygen sensors are used when air quality or oxygen delivered to a patient needs to be monitored. Fresh air contains 20.9% oxygen. Air samples containing less than 18% oxygen are considered dangerous. Oxygen sensors are also used in industrial applications where the environment must lack oxygen. An example is when food is vacuum packed. There are two main categories of oxygen sensors, those which sense oxygen when it is abundantly present (i.e. in air or near an oxygen tank) and those which detect traces of oxygen in ppm.

Figure 5 shows a typical circuit used to amplify the output of an oxygen detector. The LPV521 makes an excellent choice for this application as it only draws 345 nA of current and operates on supply voltages down to 1.6V. This application detects oxygen in air. The oxygen sensor outputs a known current through the load resistor. This value changes with the amount of oxygen present in the air sample. Oxygen sensors usually recommend a particular load resistor value or specify a range of acceptable values for the load resistor. Oxygen sensors typically have a life of one to two years. The use of the nanopower LPV521 means minimal power usage by the op amp and it enhances the battery life. With the components shown in Figure 5 the circuit can consume less than 0.5 µA of current ensuring that even batteries used in compact portable electronics, with low mAh charge ratings, could last beyond the life of the oxygen sensor. The precision specifications of the LPV521, such as its very low offset voltage, low TCV_{OS} , low input bias current, high CMRR, and high PSRR are other factors which make the LPV521 a great choice for this application.

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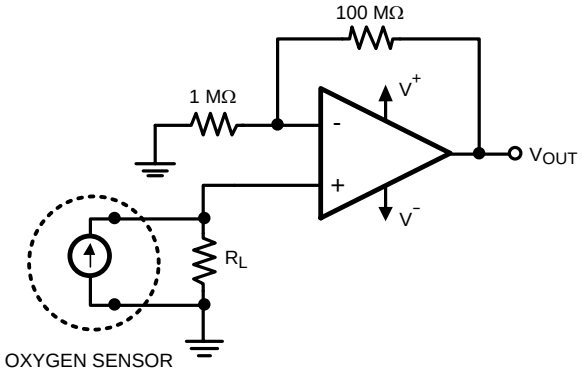

Figure 5. Precision Oxygen Sensor

INPUT STAGE

The LPV521 has a rail-to-rail input which provides more flexibility for the system designer. Rail-to-rail input is achieved by using in parallel, one PMOS differential pair and one NMOS differential pair. When the common mode input voltage (V_{CM}) is near V+, the NMOS pair is on and the PMOS pair is off. When V_{CM} is near V−, the NMOS pair is off and the PMOS pair is on. When V_{CM} is between V+ and V−, internal logic decides how much current each differential pair will get. This special logic ensures stable and low distortion amplifier operation within the entire common mode voltage range.

Because both input stages have their own offset voltage (V_{OS}) characteristic, the offset voltage of the LPV521 becomes a function of V_{CM}. V_{OS} has a crossover point at 1.0V below V+. Refer to the 'V_{OS} vs. V_{CM}' curve in the Typical Performance Characteristics section. Caution should be taken in situations where the input signal amplitude is comparable to the V_{OS} value and/or the design requires high accuracy. In these situations, it is necessary for the input signal to avoid the crossover point. In addition, parameters such as PSRR and CMRR which involve the input offset voltage will also be affected by changes in V_{CM} across the differential pair transition region.

OUTPUT STAGE

The LPV521 output voltage swings 3 mV from rails at 3.3V supply, which provides the maximum possible dynamic range at the output. This is particularly important when operating on low supply voltages.

The LPV521 Maximum Output Voltage Swing defines the maximum swing possible under a particular output load. The LPV521 output swings 50 mV from the rail at 5V supply with an output load of 100 kΩ.

DRIVING CAPACITIVE LOAD

The LPV521 is internally compensated for stable unity gain operation, with a 6.2 kHz typical gain bandwidth. However, the unity gain follower is the most sensitive configuration to capacitive load. The combination of a capacitive load placed at the output of an amplifier along with the amplifier's output impedance creates a phase lag, which reduces the phase margin of the amplifier. If the phase margin is significantly reduced, the response will be under damped which causes peaking in the transfer and, when there is too much peaking, the op amp might start oscillating.

In order to drive heavy capacitive loads, an isolation resistor, R_{ISO}, should be used, as shown in Figure 6. By using this isolation resistor, the capacitive load is isolated from the amplifier's output. The larger the value of R_{ISO}, the more stable the amplifier will be. If the value of R_{ISO} is sufficiently large, the feedback loop will be stable, independent of the value of C_L. However, larger values of R_{ISO} result in reduced output swing and reduced output current drive.

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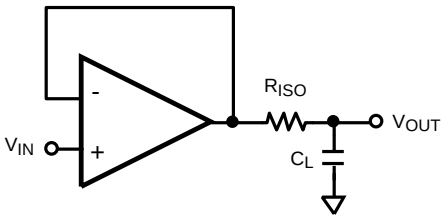

Figure 6. Resistive Isolation of Capacitive Load

Recommended minimum values for R_{ISO} are given in the following table, for 5V supply. Figure 7 shows the typical response obtained with the C_L = 50 pF and R_{ISO} = 154 kΩ. The other values of R_{ISO} in the table were chosen to achieve similar dampening at their respective capacitive loads. Notice that for the LPV521 with larger C_L a smaller R_{ISO} can be used for stability. However, for a given C_L a larger R_{ISO} will provide a more damped response. For capacitive loads of 20 pF and below no isolation resistor is needed.

C_L	R_{ISO}
0 – 20 pF	not needed
50 pF	154 kΩ
100 pF	118 kΩ
500 pF	52.3 kΩ
1 nF	33.2 kΩ
5 nF	17.4 kΩ
10 nF	13.3 kΩ

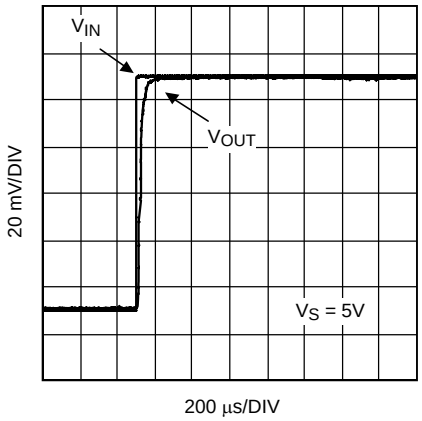

Figure 7. Step Response

EMI SUPPRESSION

The near-ubiquity of cellular, bluetooth, and Wi-Fi signals and the rapid rise of sensing systems incorporating wireless radios make electromagnetic interference (EMI) an evermore important design consideration for precision signal paths. Though RF signals lie outside the op amp band, RF carrier switching can modulate the DC offset of the op amp. Also some common RF modulation schemes can induce down-converted components. The added DC offset and the induced signals are amplified with the signal of interest and thus corrupt the measurement. The LPV521 uses on chip filters to reject these unwanted RF signals at the inputs and power supply pins; thereby preserving the integrity of the precision signal path.

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Twisted pair cabling and the active front-end's common-mode rejection provide immunity against low frequency noise (i.e. 60 Hz or 50 Hz mains) but are ineffective against RF interference. Even a few centimeters of PCB trace and wiring for sensors located close to the amplifier can pick up significant 1 GHz RF. The integrated EMI filters of the LPV521 reduce or eliminate external shielding and filtering requirements, thereby increasing system robustness. A larger EMIRR means more rejection of the RF interference. For more information on EMIRR, please refer to AN-1698.

POWER SUPPLIES AND LAYOUT

The LPV521 operates from a single 1.6V to 5.5V power supply. It is recommended to bypass the power supplies with a 0.1 µF ceramic capacitor placed close to the V^+ and V^- pins.

Ground layout improves performance by decreasing the amount of stray capacitance and noise at the op amp's inputs and outputs. To decrease stray capacitance, minimize PC board trace lengths and resistor leads, and place external components close to the op amps' pins.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
LPV521MG/NOPB	ACTIVE	SC70	DCK	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	AHA	Samples
LPV521MGE/NOPB	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	AHA	Samples
LPV521MGX/NOPB	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	AHA	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
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Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Only one of markings shown within the brackets will appear on the physical device.

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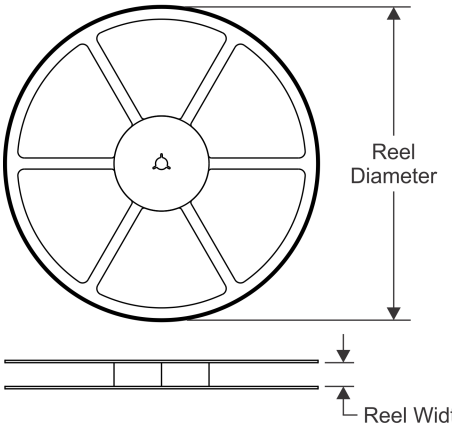
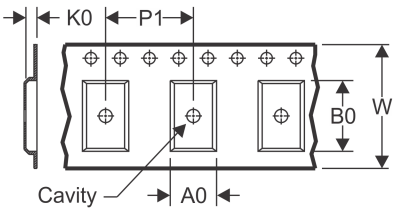
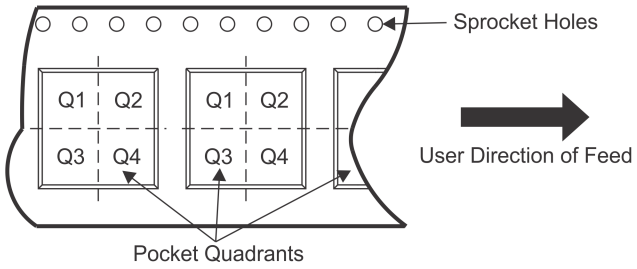


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

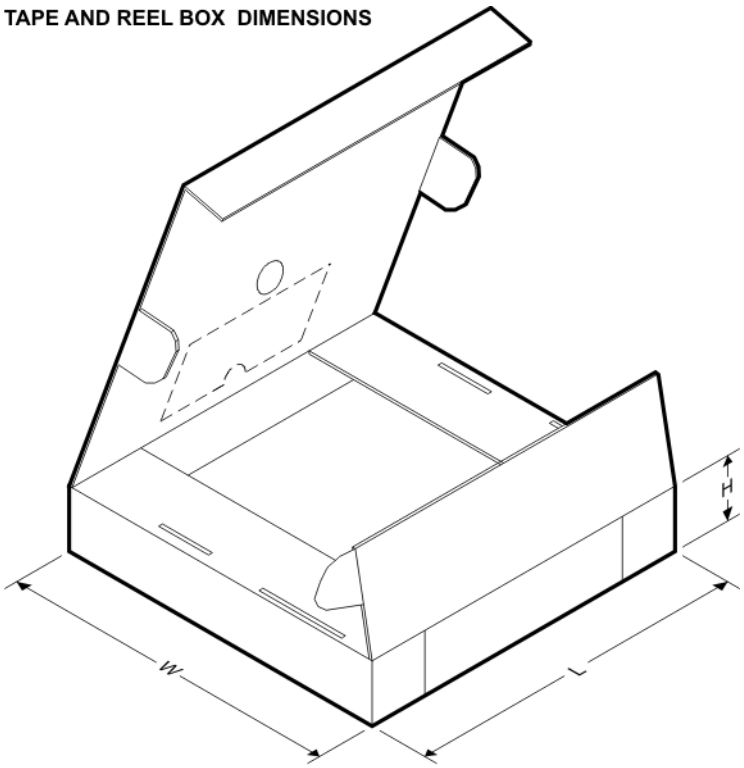
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LPV521MG/NOPB	SC70	DCK	5	1000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
LPV521MGE/NOPB	SC70	DCK	5	250	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
LPV521MGX/NOPB	SC70	DCK	5	3000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3

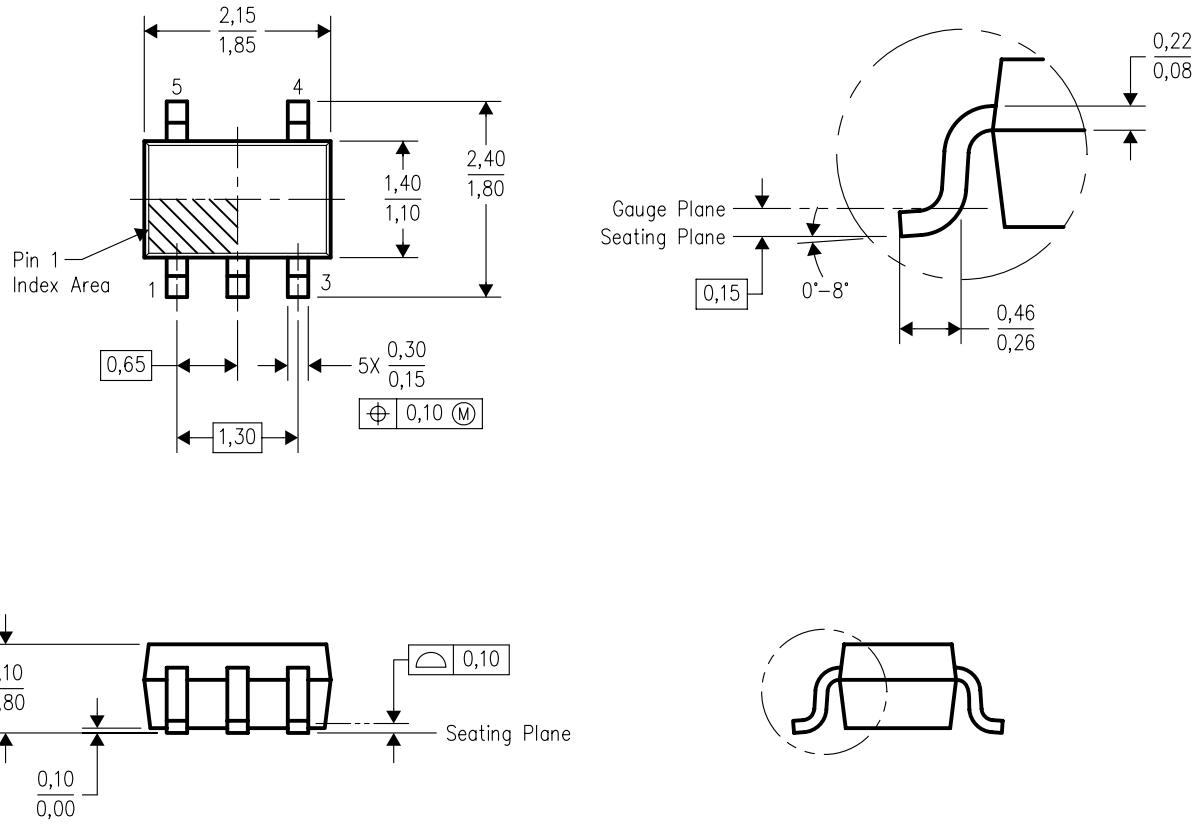
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LPV521MG/NOPB	SC70	DCK	5	1000	203.0	190.0	41.0
LPV521MGE/NOPB	SC70	DCK	5	250	203.0	190.0	41.0
LPV521MGX/NOPB	SC70	DCK	5	3000	206.0	191.0	90.0

DCK (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE



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NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–203 variation AA.

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