

## LPV821, 650nA, Precision, Nanopower, Zero-Drift Amplifier

### 1 Features

- Quiescent Current: 650 nA
- Low Offset Voltage:  $\pm 10 \mu\text{V}$  (Maximum)
- Offset Voltage Drift:  $\pm 0.096 \mu\text{V}/^\circ\text{C}$  (Maximum)
- 0.1-Hz to 10-Hz Noise:  $3.9 \mu\text{V}_{\text{PP}}$
- Input Bias Current:  $\pm 7 \text{ pA}$
- Gain Bandwidth: 8 kHz
- Supply Voltage: 1.7 V to 3.6 V
- Rail-to-Rail Input/Output
- Industry Standard Package
  - Single in 5-pin SOT-23
- EMI Hardened

### 2 Applications

- Battery-Powered Instruments
- Gas Detection
- Process Analytics
- Fault Monitoring
- Current Sensing
  - Shunt Resistor
  - Current Transformer
- Temperature Measurements
  - High Impedance Thermistors
  - RTD's, Thermocouples
- Strain Gauges
  - Electronic Scales
  - Pressure Sensors

### 3 Description

The LPV821 is a single-channel, nanopower, zero-drift operational amplifier for “Always ON” sensing applications in wireless and wired equipment where low input offset is required. With the combination of low initial offset, low offset drift, and 8 kHz of bandwidth from 650 nA of quiescent current, the LPV821 is the industry's lowest power zero-drift amplifier that can be used for end equipment that monitor current consumption, temperature, gas, or strain gauges.

The LPV821 zero-drift operational amplifier uses a proprietary auto-calibration technique to simultaneously provide low offset voltage ( $10 \mu\text{V}$ , maximum) and minimal drift over time and temperature. In addition to having low offset and ultra-low quiescent current, the LPV821 amplifier has pico-amp bias currents which reduce errors commonly introduced in applications monitoring sensors with high output impedance and amplifier configurations with megaohm feedback resistors.

#### Device Information<sup>(1)</sup>

PART NUMBER	CHAN COUNT	PACKAGE	BODY SIZE (NOM)
LPV821	1	SOT-23 (5)	2.90 mm x 1.60 mm
LPV822 <sup>(2)</sup>	2	WSON (8)	2.00 mm x 2.00 mm

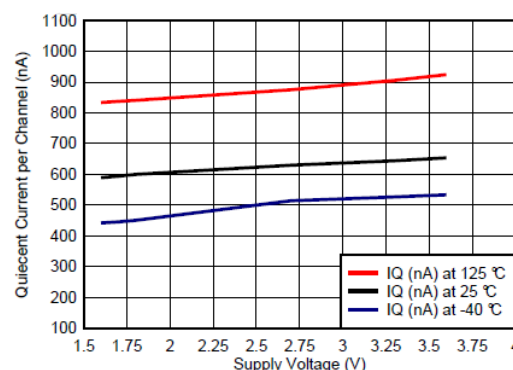
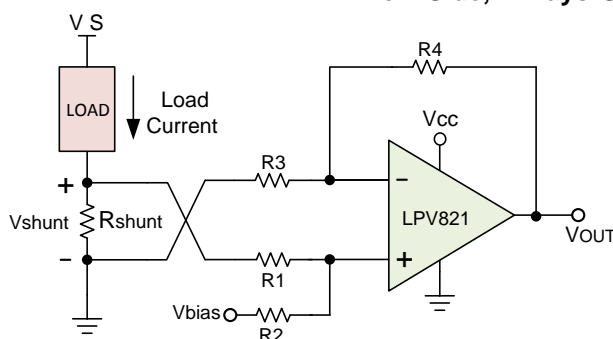
#### Precision Nano-Power Amplifier Family

FAMILY	CHAN COUNT	I <sub>Q</sub> PER CHAN	V <sub>OS</sub> (MAX)	V <sub>SUPPLY</sub>
LPV821	1	650 nA	10 $\mu\text{V}$	1.7 to 3.6 V
LPV811	1	450 nA	370 $\mu\text{V}$	1.6 to 5.5 V
LPV812	2	425 nA	300 $\mu\text{V}$	1.6 to 5.5 V
OPA369	1,2	800 nA	750 $\mu\text{V}$	1.8 to 5.5 V

(1) For all available packages, see the orderable addendum at the end of the data sheet.

(2) Planned for near-future release

#### Low-Side, Always-On Current Sense



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## 4 Revision History

### Changes from Original (August 2017) to Revision A

Page

- Changed Advanced Information to Production Data Release..... **1**

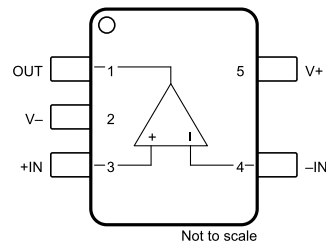
## 5 Description (continued)

The LPV821 amplifier also features an input stage with rail-to-rail input common mode range and an output stage that swings within 12 mV of the rails, maintaining the widest dynamic range possible. The device is EMI hardened to reduce system sensitivity to unwanted RF signals from mobile phones, WiFi, radio transmitters, and tag readers.

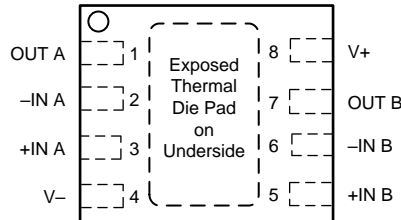
The LPV821 zero-drift amplifier operates with a single supply voltage as low as 1.7V, ensuring continuous performance in low battery situations over the extended temperature range of -40°C to 125°C. The LPV821 (single) is available in industry standard 5-pin SOT-23.

## 6 Pin Configuration and Functions

**LPV821 5-Pin SOT-23  
DBV Package  
Top View**



**LPV822 8-Pin WSON  
DSG Package  
Top View**



**Pin Functions: LPV821 DBV**

PIN		I/O	DESCRIPTION
NAME	NUMBER		
OUT	1	O	Output
V-	2	P	Negative (lowest) power supply
+IN	3	I	Non-Inverting Input
-IN	4	I	Inverting Input
V+	5	P	Positive (highest) power supply

**Pin Functions: LPV822 DSG (Preview)**

PIN		I/O	DESCRIPTION
NAME	NUMBER		
OUT A	1	O	Channel A Output
-IN A	2	I	Channel A Inverting Input
+IN A	3	I	Channel A Non-Inverting Input
V-	4	P	Negative (lowest) power supply
+IN B	5	I	Channel B Non-Inverting Input
-IN B	6	I	Channel B Inverting Input
OUT B	7	O	Channel B Output
V+	8	P	Positive (highest) power supply

## 7 Specifications

### 7.1 Absolute Maximum Ratings

See <sup>(1)</sup>

		MIN	MAX	UNIT
Voltage	Supply, $V_S = (V+) - (V-)$	-0.3	4	V
	Input/Output Pin Voltage <sup>(2)</sup> <sup>(3)</sup>	(V-) - 0.3	(V+) + 0.3	
	Differential Input Voltage +IN - (-IN) <sup>(2)</sup>	- 0.3	+ 0.3	
Current	Signal input terminals <sup>(2)</sup>	-10	10	mA
	Output short-circuit <sup>(4)</sup>	Continuous	Continuous	
Junction temperature			150	°C
Operating ambient temperature		-40	125	
Storage temperature, $T_{stg}$		-65	150	

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under . Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.3 V beyond the supply rails should be current limited to 10 mA or less.
- (3) Not to exceed -0.3V or +4.0V on ANY pin, referred to V-
- (4) Short-circuit to ground, one amplifier per package.

### 7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	±750	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Supply voltage	$V_S = (V+) - (V-)$	1.7		3.6	V
Specified temperature		-40		125	°C

### 7.4 Thermal Information

THERMAL METRIC		LPV821	UNIT
		DBV (SOT)	
		5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	218.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	101.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	52.9	°C/W
$\Psi_{JT}$	Junction-to-top characterization parameter	18.9	°C/W
$\Psi_{JB}$	Junction-to-board characterization parameter	52.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

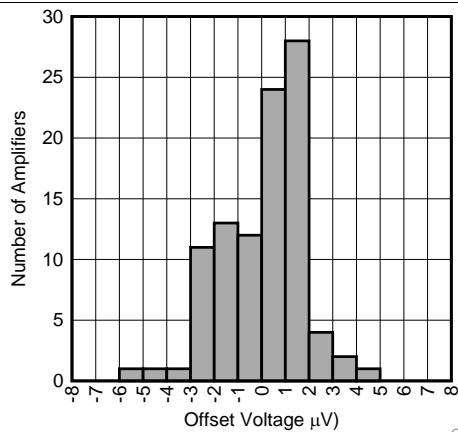
## 7.5 Electrical Characteristics

$T_A = 25^\circ\text{C}$ ,  $V_S = 1.8\text{ V to }3.3\text{ V}$ ,  $V_{CM} = V_{OUT} = V_S/2$ , and  $R_L \geq 10\text{ M}\Omega$  to  $V_S/2$ , unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>OFFSET VOLTAGE</b>						
$V_{OS}$	Input offset voltage	$V_S = 3.3\text{ V}$		$\pm 1.5$	$\pm 10$	$\mu\text{V}$
$dV_{OS}/dT$	Input offset voltage drift	$T_A = -40^\circ\text{C to }125^\circ\text{C}$ , $V_S = 3.3\text{ V}$		$\pm 0.02$	$\pm 0.096$	$\mu\text{V}/^\circ\text{C}$
PSRR	Power-supply rejection ratio	$V_S = 1.8\text{ V to }3.3\text{ V}$		0.4	4.5	$\mu\text{V/V}$
<b>INPUT</b>						
<b>BIAS CURRENT</b>						
$I_B$	Input bias current	+IN	$T_A = 25^\circ\text{C}$	7		$\text{pA}$
			$T_A = 125^\circ\text{C}$	7		
	-IN		$T_A = 25^\circ\text{C}$	-7		
			$T_A = 125^\circ\text{C}$	-250		
$I_{OS}$	Input offset current			14		$\text{pA}$
<b>NOISE</b>						
$E_n$	Input voltage noise	$f = 0.1\text{ Hz to }10\text{ Hz}$		3.9		$\mu\text{V}_{PP}$
$e_n$	Input voltage noise density	$f = 100\text{ Hz}$		215		$\text{nV}/\sqrt{\text{Hz}}$
$i_n$	Input current noise density	$f = 100\text{ Hz}$		1		$\text{fA}/\sqrt{\text{Hz}}$
<b>INPUT VOLTAGE</b>						
$V_{CM}$	Common-mode voltage range		(V-)		(V+)	V
CMRR	Common-mode rejection ratio	$(V-) \leq V_{CM} \leq (V+)$ , $V_S = 3.3\text{ V}$	100	125		dB
<b>INPUT CAPACITANCE</b>						
	Differential			3.3		pF
	Common-mode			3.7		pF
<b>OPEN-LOOP GAIN</b>						
$A_{OL}$	Open-loop voltage gain	$(V-) + 0.1\text{ V} \leq V_O \leq (V+) - 0.1\text{ V}$ , $R_L = 100\text{ k}\Omega$ to $V_S/2$		135		dB
<b>FREQUENCY RESPONSE</b>						
GBW	Gain-bandwidth product	$C_L = 20\text{ pF}$ , $R_L = 10\text{ M}\Omega$		8		kHz
SR	Slew rate	$G = +1$ , $C_L = 20\text{ pF}$		3.3		V/ms
<b>OUTPUT</b>						
$V_{OH}$	Voltage output swing from positive rail	$R_L = 100\text{ k}\Omega$ to $V^+/2$ , $V_S = 3.3\text{ V}$			12	mV
$V_{OL}$	Voltage output swing from negative rail	$R_L = 100\text{ k}\Omega$ to $V^+/2$ , $V_S = 3.3\text{ V}$			12	
$I_{SC}$	Short-circuit current	Sourcing, $V_O$ to $V_-$ , $V_{IN(diff)} = 100\text{ mV}$ , $V_S = 3.3\text{ V}$		21		mA
		Sinking, $V_O$ to $V_+$ , $V_{IN(diff)} = -100\text{ mV}$ , $V_S = 3.3\text{ V}$		50		
$C_L$	Capacitive load drive			See Table 1		
$Z_O$	Open-loop output impedance	$f = 100\text{ Hz}$ , $I_O = 0\text{ A}$		80		k $\Omega$
<b>POWER SUPPLY</b>						
$I_Q$	Quiescent current per channel	$V_{CM} = V_S/2$ , $I_O = 0$ , $V_S = 3.3\text{ V}$		650	790	nA

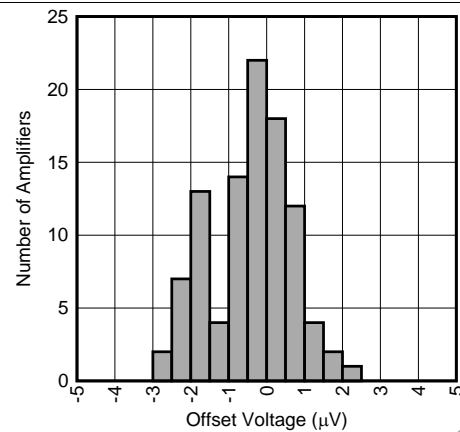
## 7.6 Typical Characteristics

At  $T_A = 25^\circ\text{C}$ ,  $V_S = 3.3\text{ V}$ ,  $V_{CM} = V_{OUT} = V_S/2$ ,  $C_L = 20\text{ pF}$ , and  $R_L \geq 10\text{ M}\Omega$ , unless otherwise noted.



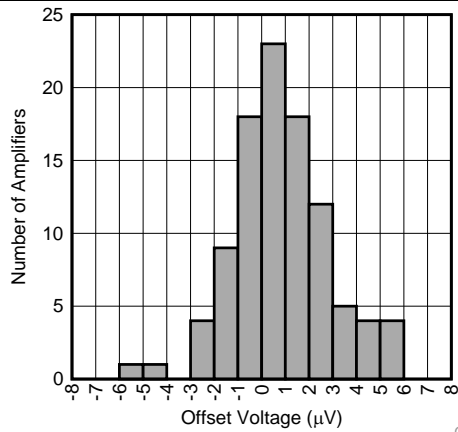
$V_S = 1.8\text{ V}$   $N = 98\text{ units}$   $T_A = -40^\circ\text{C}$

**Figure 1. Offset Voltage Distribution,  $V_S = 1.8\text{ V}$**



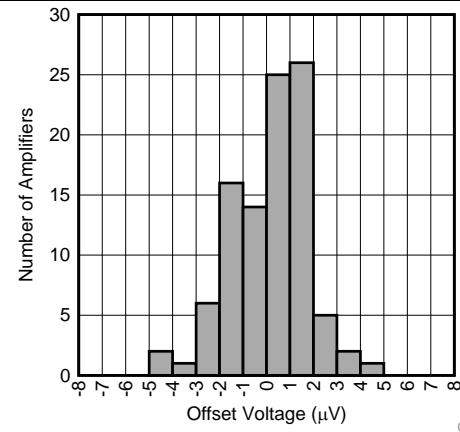
$V_S = 1.8\text{ V}$   $N = 98\text{ units}$   $T_A = 25^\circ\text{C}$

**Figure 2. Offset Voltage Distribution,  $V_S = 1.8\text{ V}$**



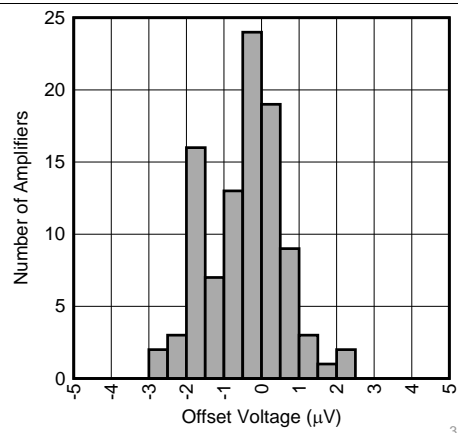
$V_S = 1.8\text{ V}$   $N = 98\text{ units}$   $T_A = 125^\circ\text{C}$

**Figure 3. Offset Voltage Distribution,  $V_S = 1.8\text{ V}$**



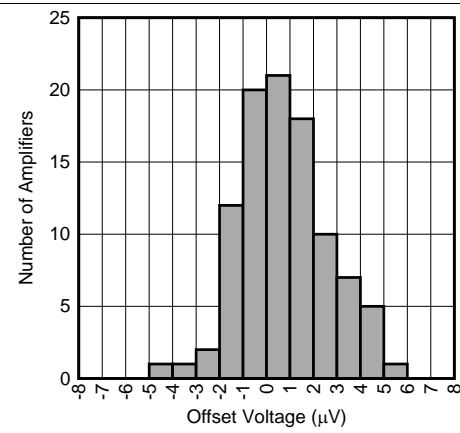
$V_S = 3.3\text{ V}$   $N = 98\text{ units}$   $T_A = -40^\circ\text{C}$

**Figure 4. Offset Voltage Distribution,  $V_S = 3.3\text{ V}$**



$V_S = 3.3\text{ V}$   $N = 98\text{ units}$   $T_A = 25^\circ\text{C}$

**Figure 5. Offset Voltage Distribution,  $V_S = 3.3\text{ V}$**



$V_S = 3.3\text{ V}$   $N = 98\text{ units}$   $T_A = 125^\circ\text{C}$

**Figure 6. Offset Voltage Distribution,  $V_S = 3.3\text{ V}$**

## Typical Characteristics (continued)

At  $T_A = 25^\circ\text{C}$ ,  $V_S = 3.3\text{ V}$ ,  $V_{CM} = V_{OUT} = V_S/2$ ,  $C_L = 20\text{ pF}$ , and  $R_L \geq 10\text{ M}\Omega$ , unless otherwise noted.

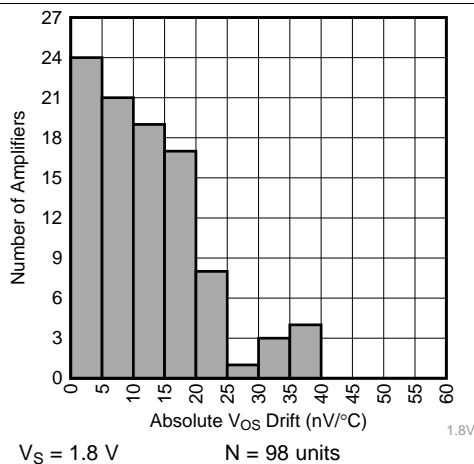


Figure 7. Offset Voltage Drift Distribution,  $V_S = 1.8\text{ V}$

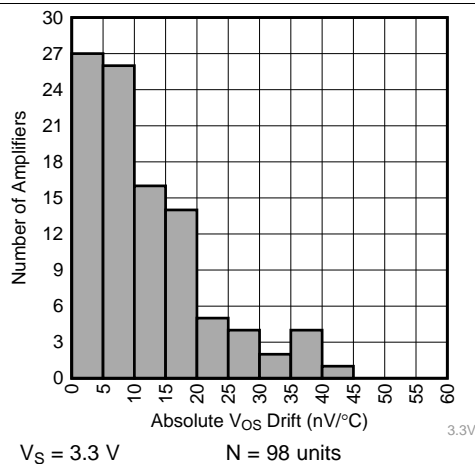


Figure 8. Offset Voltage Drift Distribution,  $V_S = 3.3\text{ V}$

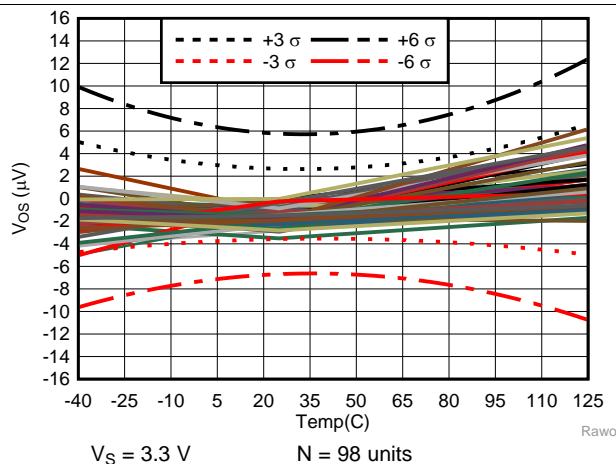


Figure 9. Offset Voltage vs Temperature,  $V_S = 3.3\text{ V}$

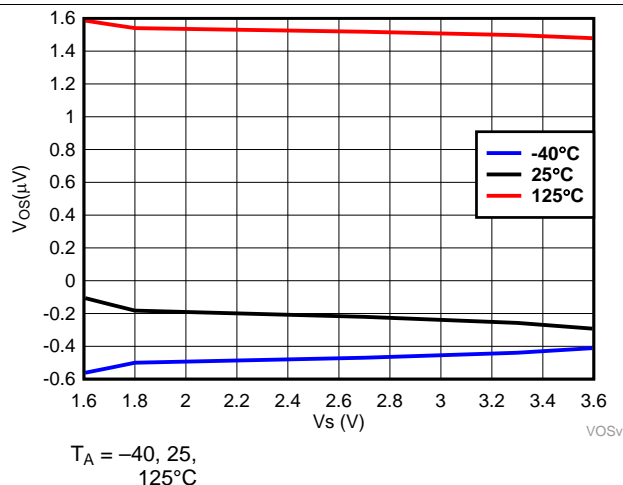


Figure 10. Offset Voltage vs Supply Voltage

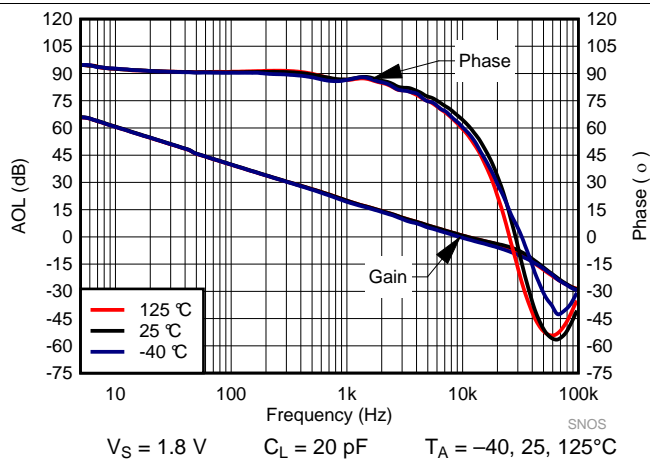


Figure 11. Open-Loop Gain and Phase vs Frequency

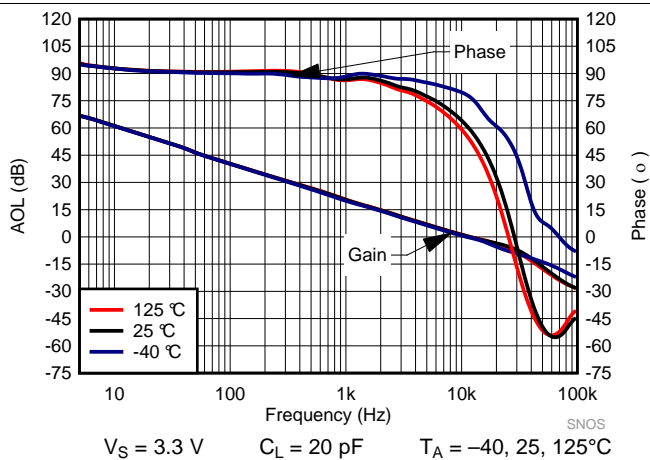


Figure 12. Open-Loop Gain and Phase vs Frequency

## Typical Characteristics (continued)

At  $T_A = 25^\circ\text{C}$ ,  $V_S = 3.3\text{ V}$ ,  $V_{CM} = V_{OUT} = V_S/2$ ,  $C_L = 20\text{ pF}$ , and  $R_L \geq 10\text{ M}\Omega$ , unless otherwise noted.

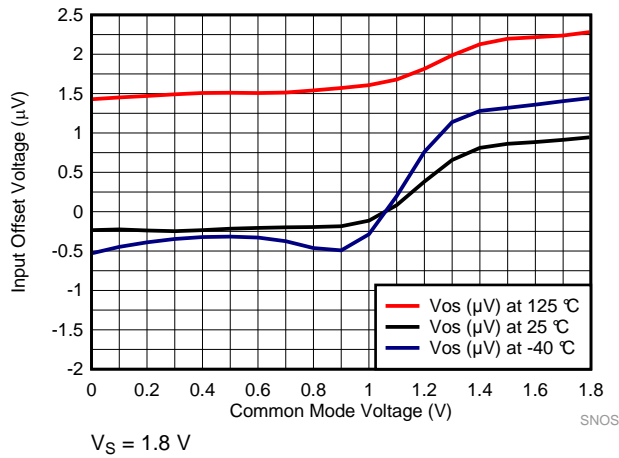


Figure 13. Input Offset Voltage vs Input Common Mode Voltage

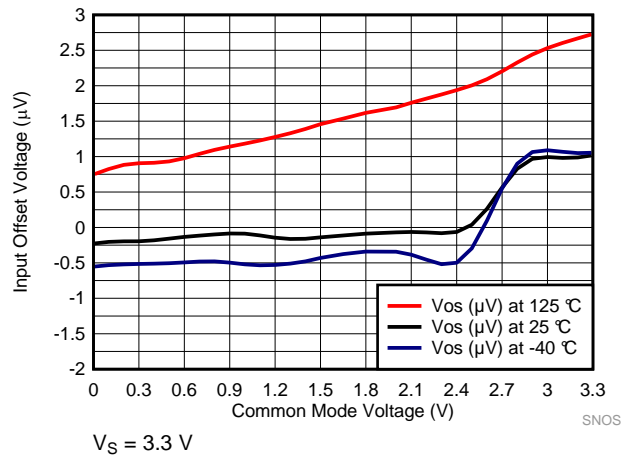


Figure 14. Input Offset Voltage vs Input Common Mode Voltage

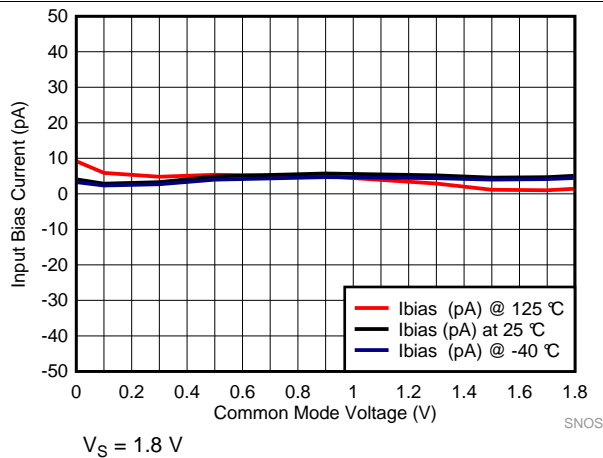


Figure 15. Input Bias Current on +IN Input Pin vs Common Mode Voltage

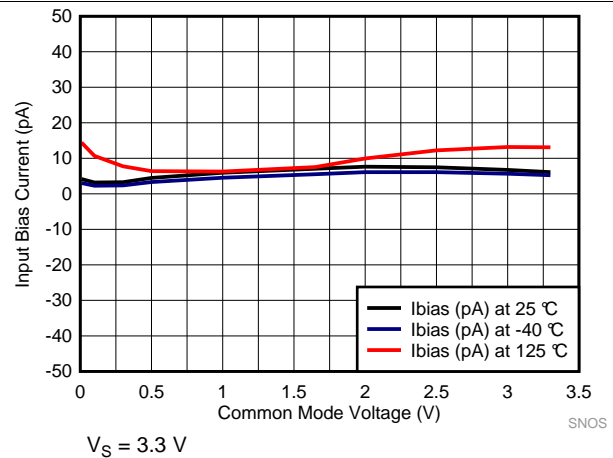


Figure 16. Input Bias Current on +IN Input Pin vs Common Mode Voltage

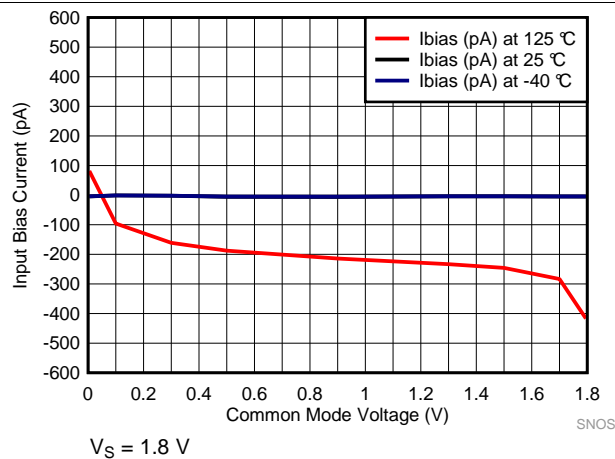


Figure 17. Input Bias Current on -IN Pin vs Common Mode Voltage

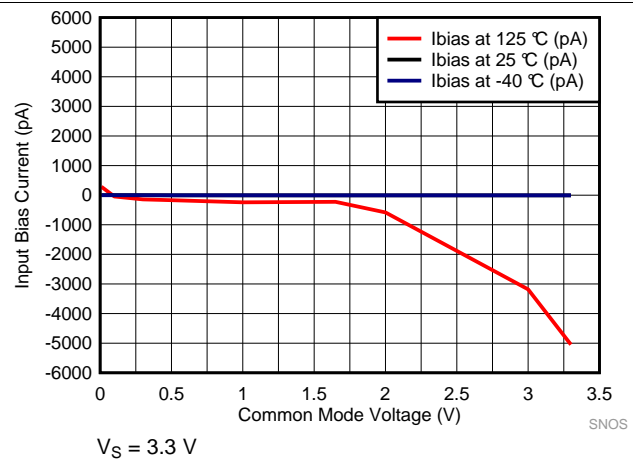
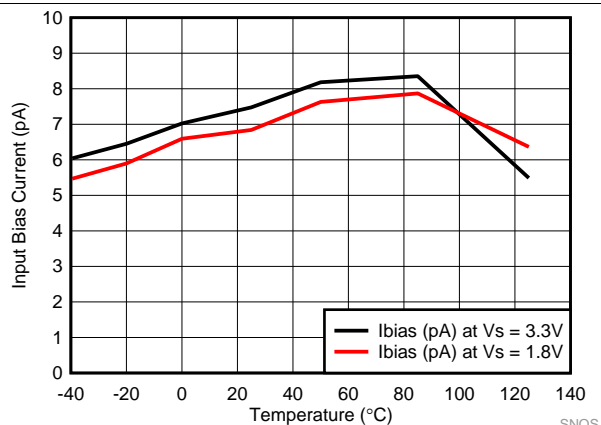


Figure 18. Input Bias Current on -IN Input Pin vs Common Mode Voltage



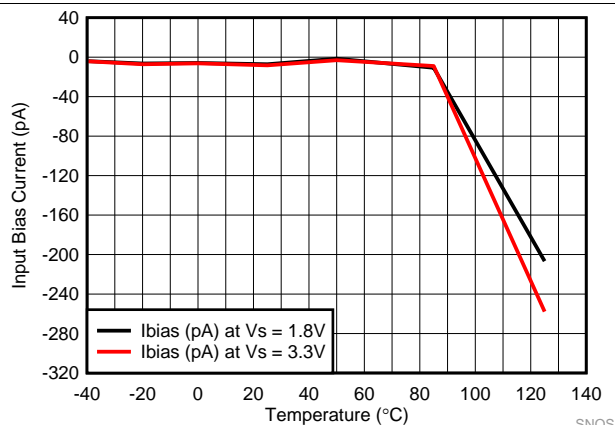
## Typical Characteristics (continued)

At  $T_A = 25^\circ\text{C}$ ,  $V_S = 3.3\text{ V}$ ,  $V_{CM} = V_{OUT} = V_S/2$ ,  $C_L = 20\text{ pF}$ , and  $R_L \geq 10\text{ M}\Omega$ , unless otherwise noted.



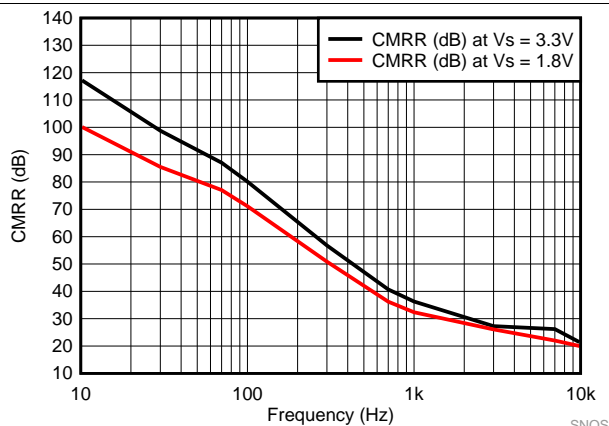
$V_S = 3.3\text{ V}$  and  $1.8\text{ V}$

**Figure 19. Input Bias Current ON +IN Input vs Temperature**



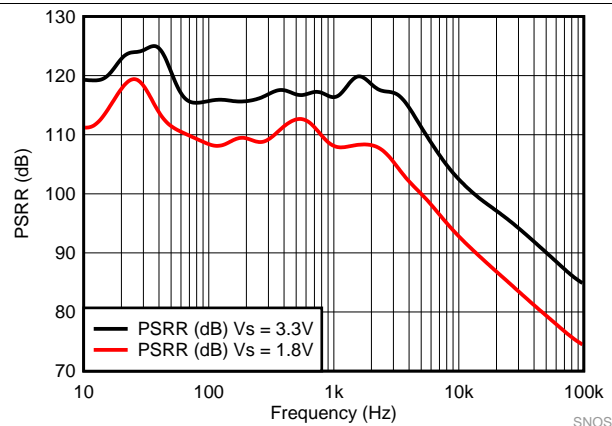
$V_S = 3.3\text{ V}$  and  $1.8\text{ V}$

**Figure 20. Input Bias Current on -IN Input Pin vs Temperature**



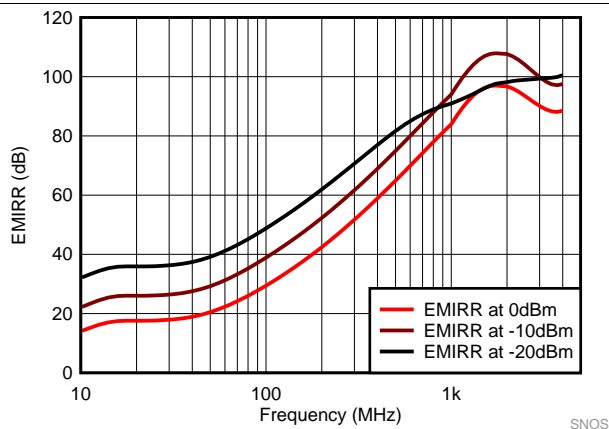
$V_S = 3.3\text{ V}$  and  $1.8\text{ V}$

**Figure 21. CMRR vs Frequency**

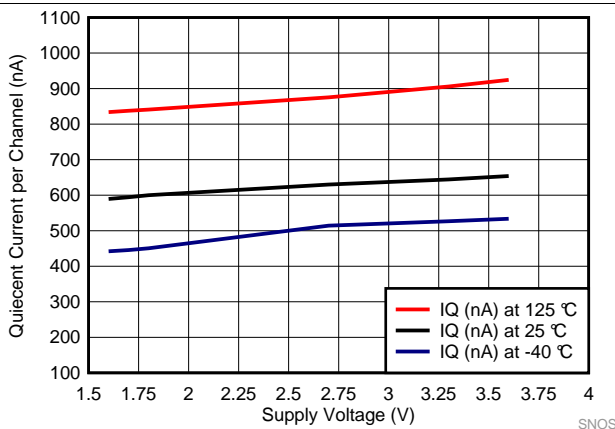


$V_S = 3.3\text{ V}$  and  $1.8\text{ V}$

**Figure 22. PSRR vs Frequency**



**Figure 23. EMIRR Performance**



$T_A = -40, 25, 125^\circ\text{C}$

**Figure 24. Per Channel Quiescent Current vs Supply Voltage**

## Typical Characteristics (continued)

At  $T_A = 25^\circ\text{C}$ ,  $V_S = 3.3\text{ V}$ ,  $V_{CM} = V_{OUT} = V_S/2$ ,  $C_L = 20\text{ pF}$ , and  $R_L \geq 10\text{ M}\Omega$ , unless otherwise noted.

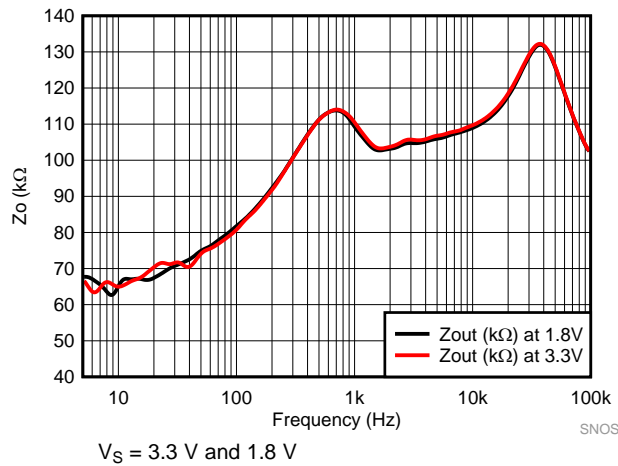


Figure 25. Open Loop Output Impedance

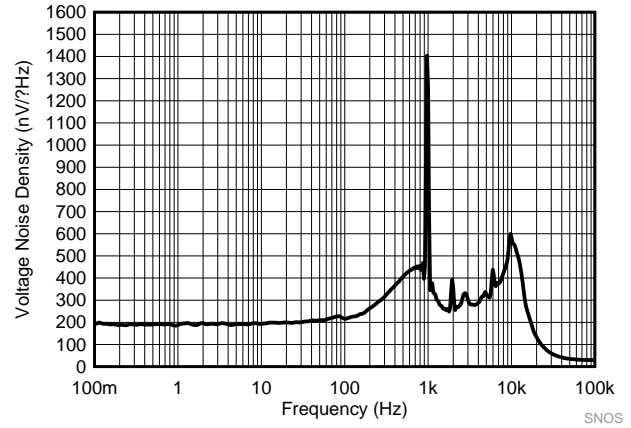


Figure 26. Voltage Noise Spectral Density vs Frequency

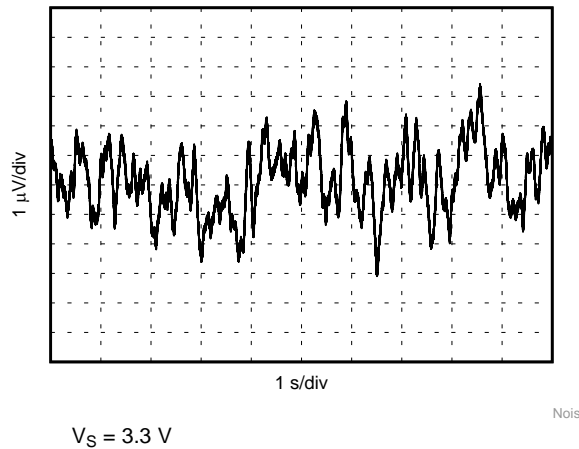


Figure 27. 0.1-Hz to 10-Hz Noise,  $V_S = 3.3\text{ V}$

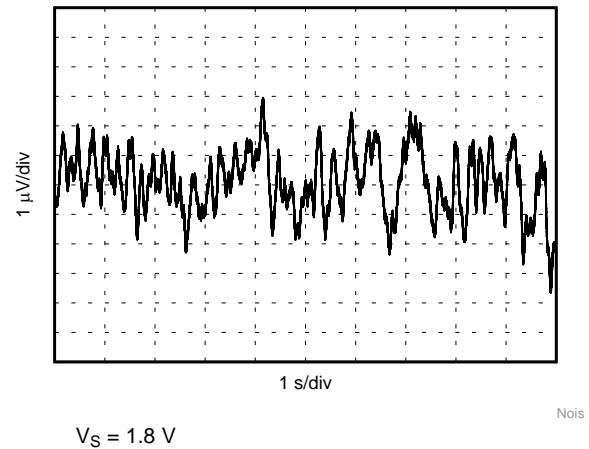


Figure 28. 0.1-Hz to 10-Hz Noise,  $V_S = 1.8\text{ V}$

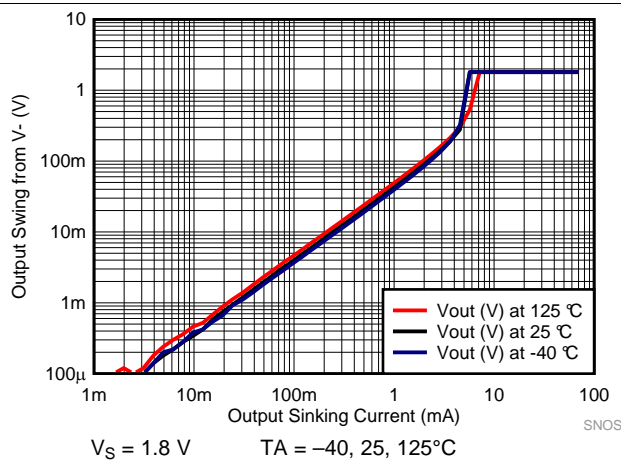


Figure 29. Output Swing vs. Sinking Current,  $1.8\text{ V}$

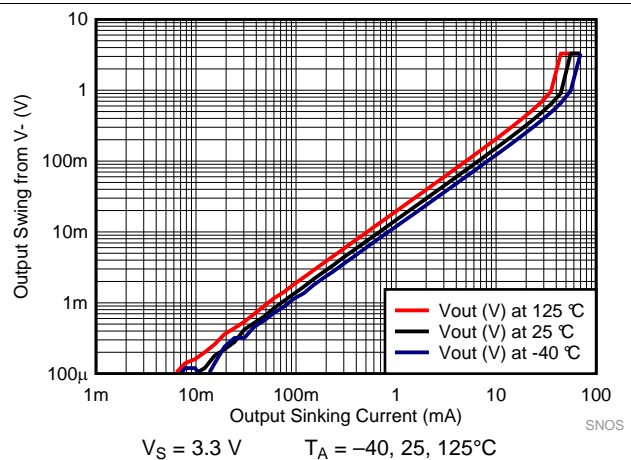
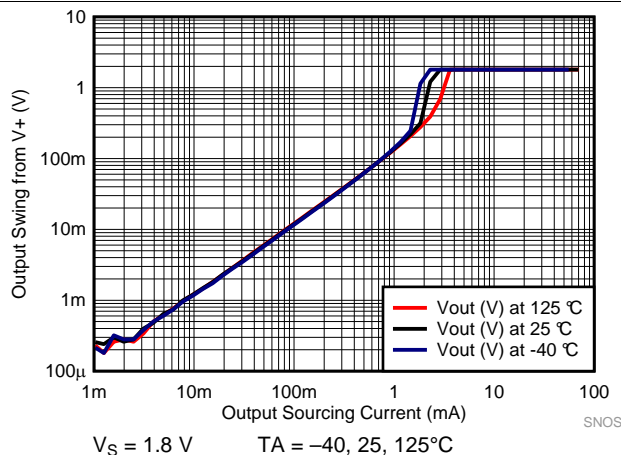


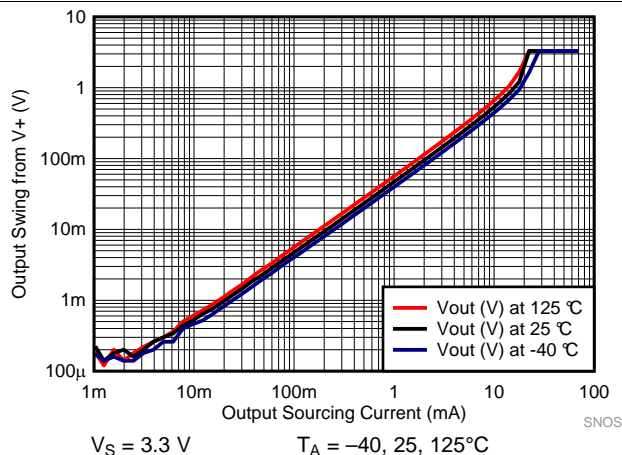
Figure 30. Output Swing vs. Sinking Current,  $3.3\text{ V}$

## Typical Characteristics (continued)

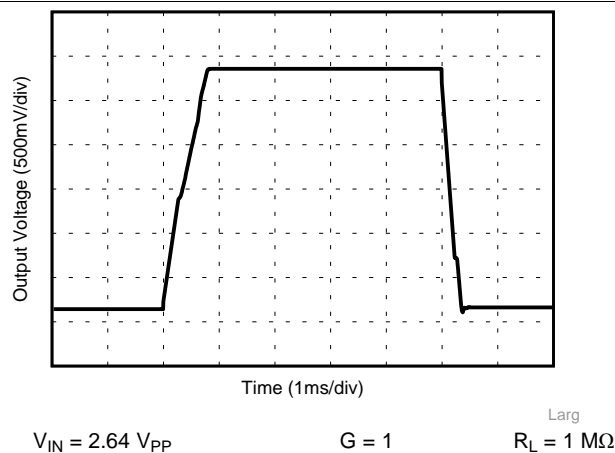
At  $T_A = 25^\circ\text{C}$ ,  $V_S = 3.3\text{ V}$ ,  $V_{CM} = V_{OUT} = V_S/2$ ,  $C_L = 20\text{ pF}$ , and  $R_L \geq 10\text{ M}\Omega$ , unless otherwise noted.



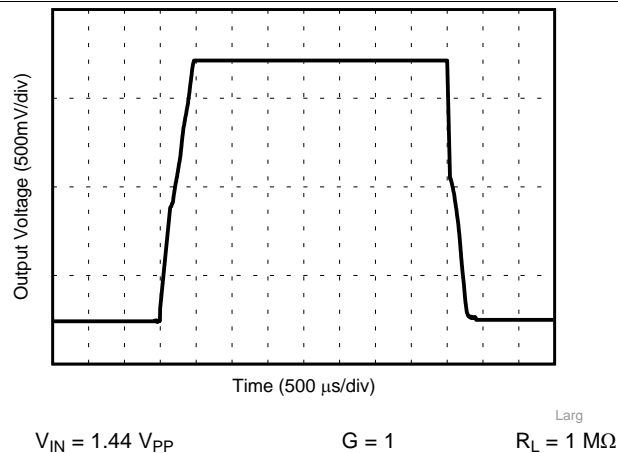
**Figure 31. Output Swing vs Sourcing Current, 1.8 V**



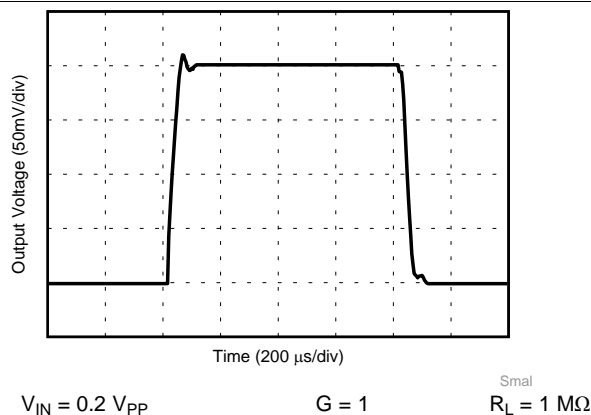
**Figure 32. Output Swing vs Sourcing Current, 3.3 V**



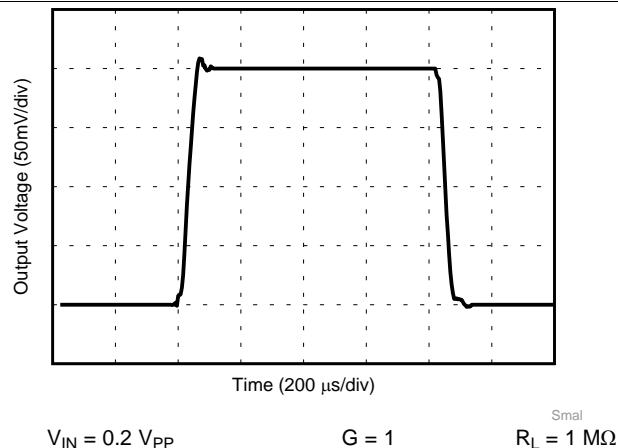
**Figure 33. Large-Signal Response, 3.3V**



**Figure 34. Large-Signal Response, 1.8V**



**Figure 35. Small Signal Response, 3.3V**



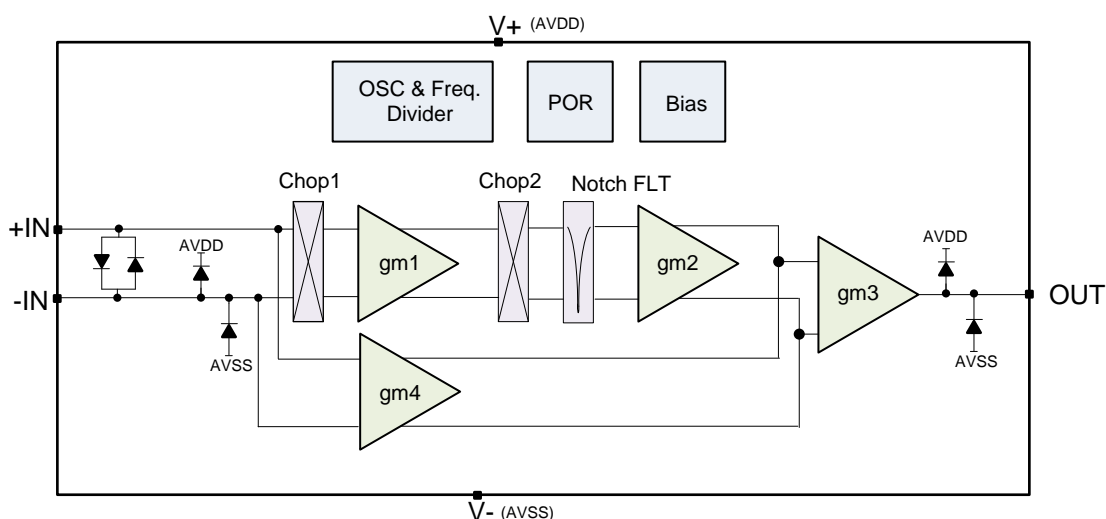
**Figure 36. Small-Signal Response, 1.8V**

## 8 Detailed Description

### 8.1 Overview

The LPV821 is a zero-drift, nanopower, rail-to-rail input and output operational amplifier. The device operates from 1.7 V to 3.7 V, is unity-gain stable, and is suitable for a wide range of general-purpose applications. The zero-drift architecture provides ultra low offset voltage and near-zero offset voltage drift.

### 8.2 Functional Block Diagram



### 8.3 Feature Description

The LPV821 is unity-gain stable and uses an auto-calibration technique to provide low offset voltage and very low drift over time and temperature. For lowest offset voltage and precision performance, optimize circuit layout and mechanical conditions. Avoid temperature gradients that create thermoelectric (Seebeck) effects in the thermocouple junctions formed from connecting dissimilar conductors. Cancel these thermally-generated potentials by assuring they are equal on both input terminals. Other layout and design considerations include:

- Use low thermoelectric-coefficient conditions (avoid dissimilar metals).
- Thermally isolate components from power supplies or other heat sources.
- Shield operational amplifier and input circuitry from air currents, such as cooling fans.

Following these guidelines reduces the likelihood of junctions being at different temperatures, which can cause thermoelectric voltages of 0.1  $\mu\text{V}/^\circ\text{C}$  or higher, depending on materials used.

#### 8.3.1 Operating Voltage

The LPV821 operational amplifier operates over a power-supply range of 1.7 V to 3.6 V ( $\pm 0.85$  V to  $\pm 1.8$  V). Parameters that vary over supply voltage or temperature are shown in the [Typical Characteristics](#) section.

#### CAUTION

Supply voltages higher than 4 V (absolute maximum) can permanently damage the device.

## Feature Description (continued)

### 8.3.2 Input

The LPV821 input common-mode voltage range extends to the supply rails. Typically, the input bias current is approximately 7 pA; however, input voltages that exceed the power supplies can cause excessive current to flow into or out of the input pins. Momentary voltages greater than the power supply can be tolerated if the input current is limited to 10 mA. This limitation is easily accomplished with adding a resistor in series with the input, as shown in [Figure 37](#).

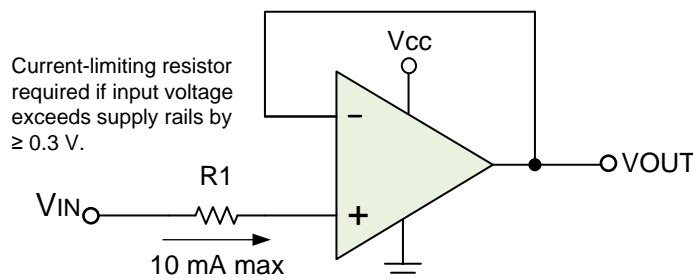


Figure 37. Input Current Protection

### 8.3.3 Internal Offset Correction

The LPV821 operational amplifier combines an auto-calibration technique with a time-continuous 8-kHz operational amplifier in the signal path. The amplifier's offset is zero-corrected every 1 ms using a proprietary technique. This design has no aliasing or flicker (1/f) noise.

### 8.3.4 Input Offset Voltage Drift

The LPV821 operational amplifier's input voltage offset drift is defined over the entire temperature range of  $-40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The maximum input voltage drift allows designers to calculate the worst-case input offset change over this temperature range. The maximum input voltage drift over temperature is defined using [Equation 1](#):

$$dV_{OS}/dT = \Delta V_{OS} / \Delta T$$

where

- $\Delta V_{OS}$  = Change in input offset voltage
- $\Delta T$  = Change in temperature ( $125^{\circ}\text{C} - (-40^{\circ}\text{C}) = 165^{\circ}\text{C}$ )
- $dV_{OS}/dT$  = Input offset voltage drift

(1)

The LPV821 datasheet maximum value for input offset voltage drift is specified for a sample size with a  $C_{pk}$  (process capability index) of 2.0.

## 8.4 Device Functional Modes

The LPV821 has a single functional mode. The device is powered on as long as the power supply voltage is between 1.7 V ( $\pm 0.85$  V) and 3.6 V ( $\pm 1.8$  V).

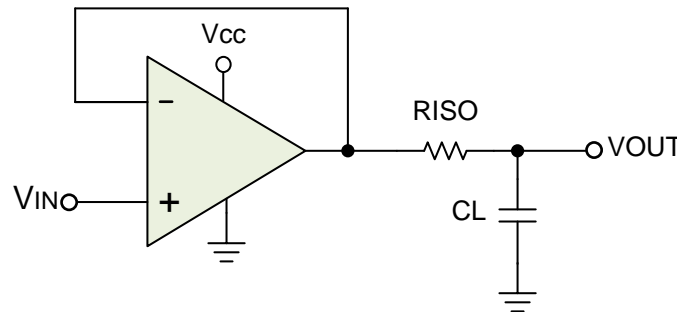
### 8.4.1 EMI Performance and Input Filtering

Operational amplifiers vary in susceptibility to EMI. If conducted EMI enters the operational amplifier, the dc offset at the amplifier output can shift from its nominal value when EMI is present. This shift is a result of signal rectification associated with the internal semiconductor junctions. Although all operational amplifier pin functions can be affected by EMI, the input pins are likely to be the most susceptible. The LPV821 operational amplifier incorporates an internal input low-pass filter that reduces the amplifier response to EMI. Both common mode and differential-mode filtering are provided by the input filter.

## Device Functional Modes (continued)

### 8.4.2 Driving Capacitive Load

The LPV821 is internally compensated for stable unity-gain operation, with a 8-kHz typical gain bandwidth. However, the unity-gain follower is the most sensitive configuration-to-capacitive load. The combination of a capacitive load placed directly on the output of an amplifier along with the output impedance of the amplifier creates a phase lag, which reduces the phase margin of the amplifier. If the phase margin is significantly reduced, the response is under-damped, which causes peaking in the transfer and, when there is too much peaking, the op amp might start oscillating.

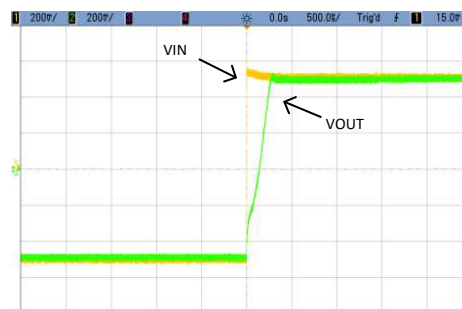


**Figure 38. Resistive Isolation of Capacitive Load**

In order to drive heavy ( $> 50$  pF) capacitive loads, use an isolation resistor,  $R_{ISO}$ , as shown in [Figure 38](#). The value of the  $R_{ISO}$  to be used should be decided depending on the size of the  $C_L$  and the level of performance desired. Recommended minimum values for  $R_{ISO}$  are given in the following table, for 3.3V supply. [Figure 39](#) shows the typical response obtained with the  $C_L = 50$  pF  $R_{ISO} = 160$  k $\Omega$ . By using the isolation resistor, the capacitive load is isolated from the output of the amplifier. The larger the value of  $R_{ISO}$ , the more stable the amplifier will be. If the value of  $R_{ISO}$  is sufficiently large, the feedback loop is stable, independent of the value of  $C_L$ . However, larger values of  $R_{ISO}$  (e.g. 50 k $\Omega$ ) result in reduced output swing and reduced output current drive.

**Table 1. Capacitive Loads vs. Needed Isolation Resistors**

$C_L$	$R_{ISO}$
0 – 20 pF	not needed
50 pF	160 k $\Omega$
100 pF	140 k $\Omega$
500 pF	54.9 k $\Omega$
1 nF	33 k $\Omega$
5 nF	15 k $\Omega$
10 nF	5.62 k $\Omega$



**Figure 39. Typical Step Response**

## 9 Application and Implementation

### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

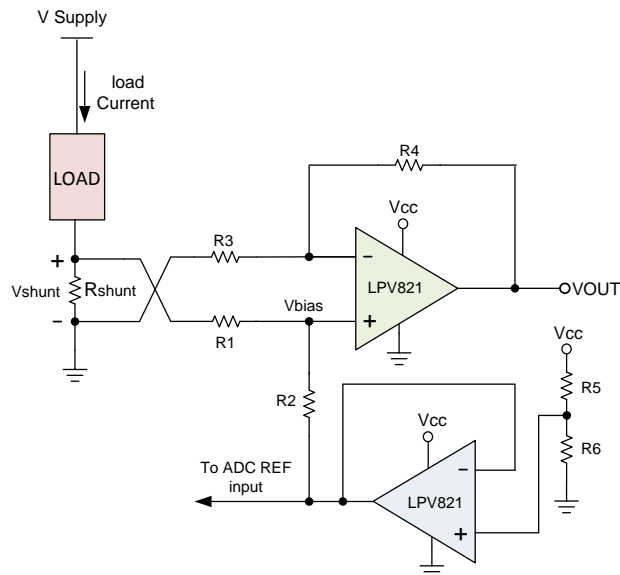
### 9.1 Application Information

The LPV821 is a unity-gain stable, precision operational amplifier with very low offset voltage drift; the device is also free from output phase reversal. Applications with noisy or high-impedance power supplies require decoupling capacitors close to the device power-supply pins. In most cases, 0.1- $\mu$ F capacitors are adequate.

### 9.2 Typical Applications

#### 9.2.1 Low-Side Current Measurement

This single-supply, low-side, current-sensing solution shown in [Figure 40](#) detects load currents up to 1 A. This design uses the LPV821 because of its low offset voltage and rail-to-rail input and output. The LPV821 in the main signal path is configured as a difference amplifier and a second LPV821 provides a buffered bias voltage to allow transition of signal below and above the bias level for bi-direction current sensing. The low offset voltage and offset drift of the LPV821 facilitate excellent dc accuracy for the circuit.



**Figure 40. Low-Side Current Measurement**

##### 9.2.1.1 Design Requirements

The design requirements are as follows:

- Supply Voltage: 3.3 V DC
- Input: 1 A (Max)
- Output:  $1.65\text{ V} \pm 1.54\text{ V}$  ; (110 mV to 3.19 V)

## Typical Applications (continued)

### 9.2.1.2 Detailed Design Procedure

Referring to [Figure 40](#), the load current passing through the shunt resistor ( $R_{shunt}$ ) develops the shunt voltage,  $V_{shunt}$  across the resistor. The shunt voltage is then amplified by the LPV821 by the ratio of  $R_4$  by  $R_3$ . The gain of the difference amplifier is set by the ratio of  $R_4$  to  $R_3$ . To minimize errors, set  $R_2 = R_4$  and  $R_1 = R_3$ . The bias voltage is supplied by buffering a resistor divider using a second LPV821 nanopower op amp. The circuit equations are provided below.

$$V_{out} = V_{shunt} * Gain_{Diff} + V_{bias} \quad (2)$$

$$V_{shunt} = I_{load} * R_{shunt} \quad (3)$$

$$Gain_{Diff} = R_4 / R_3 \quad (4)$$

$$V_{bias} = [R_6 / (R_6 + R_5)] * V_{CC} \quad (5)$$

$$R_{shunt} = [V_{shunt} (max)] / [I_{load} (max)] \quad (6)$$

Because  $V_{shunt}$  is a low-side measurement, a maximum value 100 mV was selected.

$$R_{shunt} = V_{shunt} / I_{load} = 100mV / 1A = 100m\Omega \quad (7)$$

The tolerance of the shunt resistor, the ratio of  $R_4$  to  $R_3$  and the ratio of  $R_2$  to  $R_1$  are the main sources of gain error in the signal path. To optimize the cost, a shunt resistor with a tolerance of 0.5% was chosen. The main sources of offset errors in the circuit are the voltage divider network comprised of  $R_5$ ,  $R_6$  and how closely the ratio of  $R_4 / R_3$  matches the ratio of  $R_2 / R_1$ . The latter value affects the CMRR of the difference amplifier, ultimately translating to an offset error.

The shunt voltage is scaled down by a divider network made of  $R_1$  and  $R_2$  before reaching the LPV821 amplifier stage. The voltage present at the non-inverting node of the LPV821 should not exceed the common-mode range of the device. The extremely low offset voltage and drift of the LPV821 ensures minimized offset error in the measurement.

In case a bi-direction current sensing is required, for symmetric load current of  $-1$  A to  $1$  A, the voltage divider resistors  $R_5$  and  $R_6$  must be equal. To minimize power consumption, 100-k $\Omega$  resistors with a tolerance of 0.5% were selected.

To set the gain of the difference amplifier, the common-mode range and output swing of the LPV821 must be considered. The gain of the difference amplifier can now be calculated as shown below

$$Gain = [V_{out} (max) - V_{out} (min)] / [R_{shunt} * (I_{max} - I_{min})] = [3.2 V - 100 mV] / [100 m\Omega] * [1A - (-1A)] = 15.5 V / V \quad (8)$$

## 10 Power Supply Recommendations

The LPV821 is specified for operation from 1.7 V to 3.6 ( $\pm 0.85$  V to  $\pm 1.8$  V); many specifications apply from  $-40^\circ\text{C}$  to  $125^\circ\text{C}$ . The [Typical Characteristics](#) presents parameters that can exhibit significant variance with regard to operating voltage or temperature.

### CAUTION

Supply voltages larger than 4 V can permanently damage the device (see the [Absolute Maximum Ratings](#)).

TI recommends placing 0.1- $\mu\text{F}$  bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, refer to the [Layout](#) section.



## 11 Layout

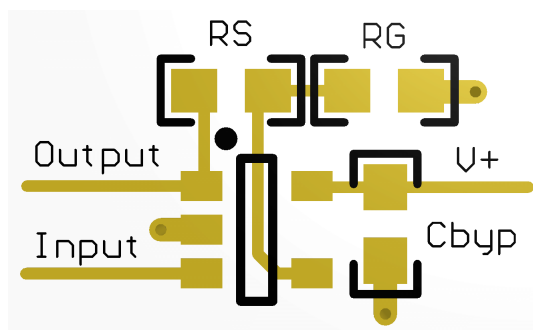
### 11.1 Layout Guidelines

#### 11.1.1 General Layout Guidelines

Pay attention to good layout practices. Keep traces short and when possible, use a printed-circuit-board (PCB) ground plane with surface-mount components placed as close to the device pins as possible. Place a 0.1- $\mu$ F capacitor closely across the supply pins. Apply these guidelines throughout the analog circuit to improve performance and provide benefits, such as reducing the electromagnetic interference (EMI) susceptibility.

Operational amplifiers vary in susceptibility to radio frequency interference (RFI). RFI can generally be identified as a variation in offset voltage or DC signal levels with changes in the interfering RF signal. The LPV821 is specifically designed to minimize susceptibility to RFI and demonstrates remarkably low sensitivity compared to previous generation devices. Strong RF fields may still cause varying offset levels.

### 11.2 Layout Example



**Figure 41. SOT-23 Layout Example**

## 12 Device and Documentation Support

### 12.1 Device Support

#### 12.1.1 Development Support

[TINA-TI SPICE-Based Analog Simulation Program](#)

[DIP Adapter Evaluation Module](#)

[TI Universal Operational Amplifier Evaluation Module](#)

[TI FilterPro Filter Design Software](#)

### 12.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

**Table 2. Related Links**

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
LPV821	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>

### 12.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 12.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 12.5 Trademarks

E2E is a trademark of Texas Instruments.

### 12.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 12.7 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LPV821DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	1CHF	<a href="#">Samples</a>
PLPV821DBV	ACTIVE	SOT-23	DBV	5	250	TBD	Call TI	Call TI	-40 to 125		<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**TAPE AND REEL INFORMATION**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LPV821DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

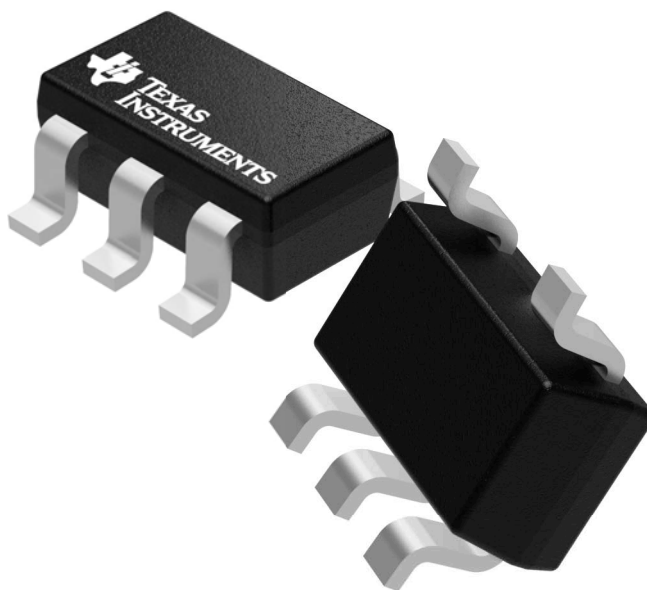
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LPV821DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0

## GENERIC PACKAGE VIEW

**DBV 5**

**SOT-23 - 1.45 mm max height**

SMALL OUTLINE TRANSISTOR



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4073253/P

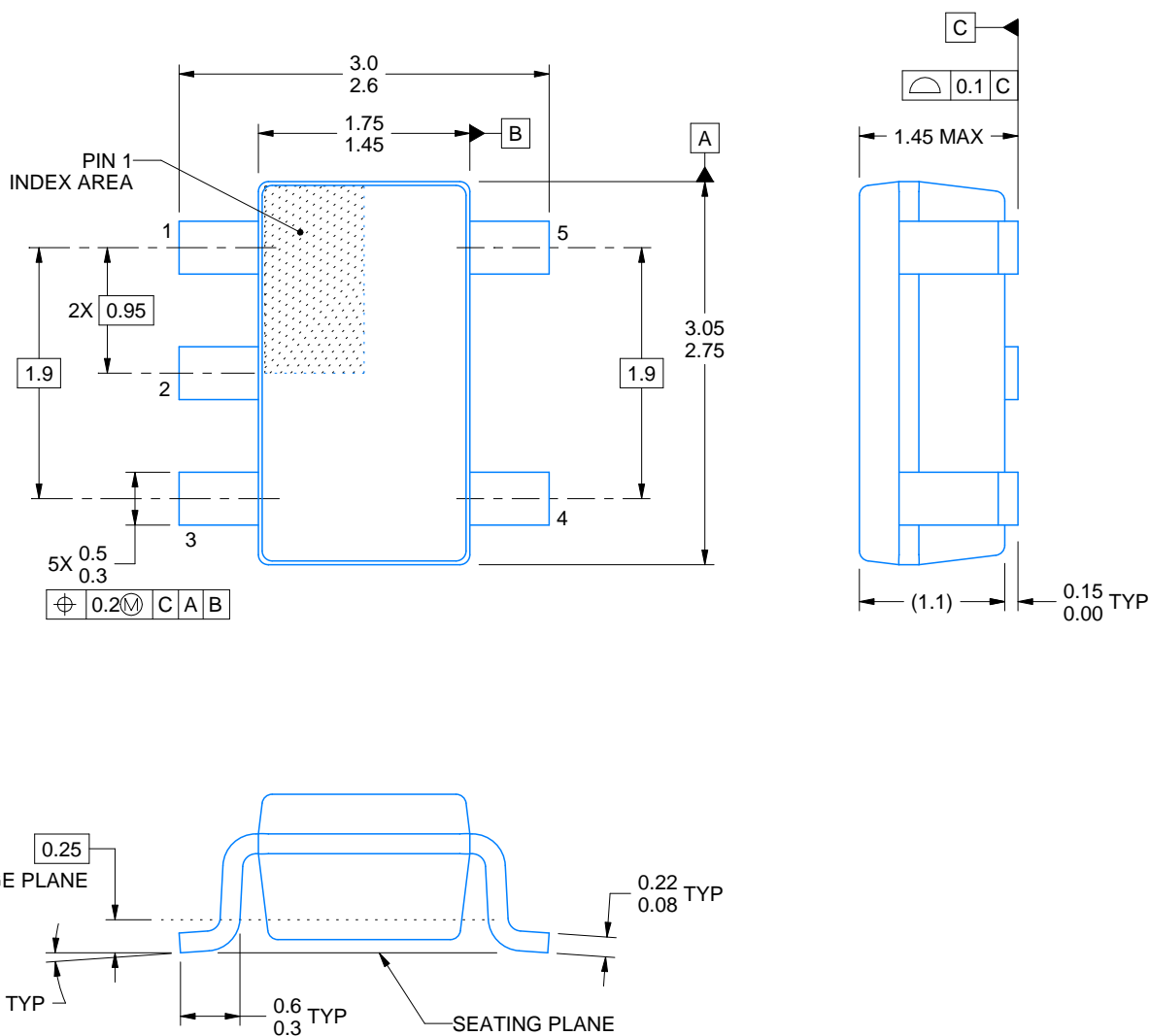


**DBV0005A**

# PACKAGE OUTLINE

**SOT-23 - 1.45 mm max height**

SMALL OUTLINE TRANSISTOR



4214839/C 04/2017

## NOTES:

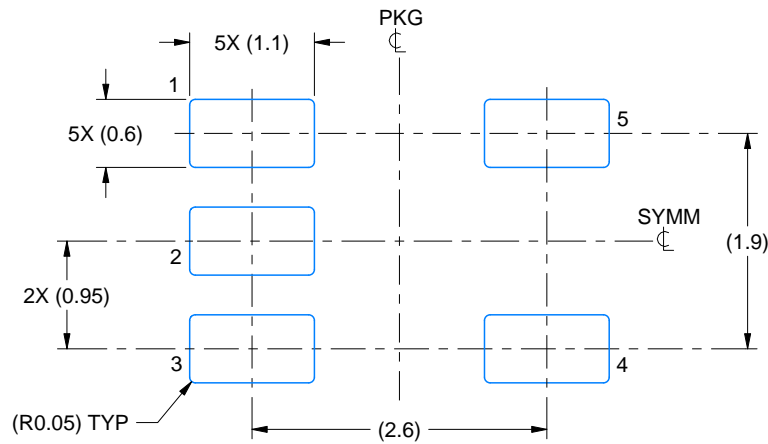
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-178.

# EXAMPLE BOARD LAYOUT

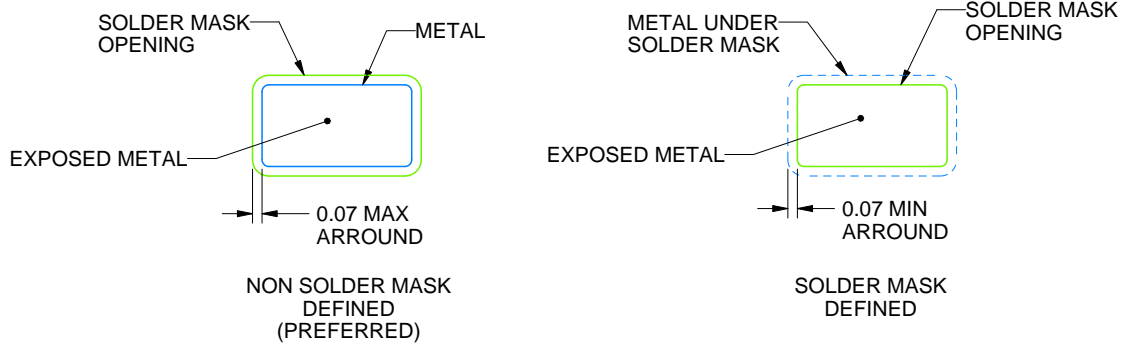
DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:15X



SOLDER MASK DETAILS

4214839/C 04/2017

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

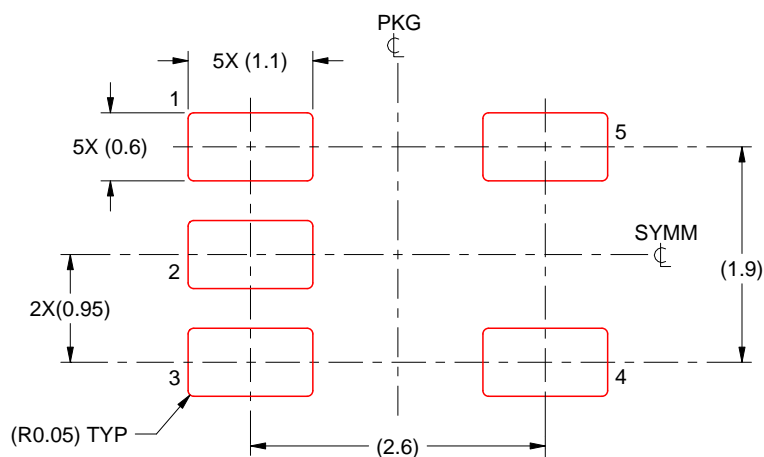


## EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:15X

4214839/C 04/2017

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

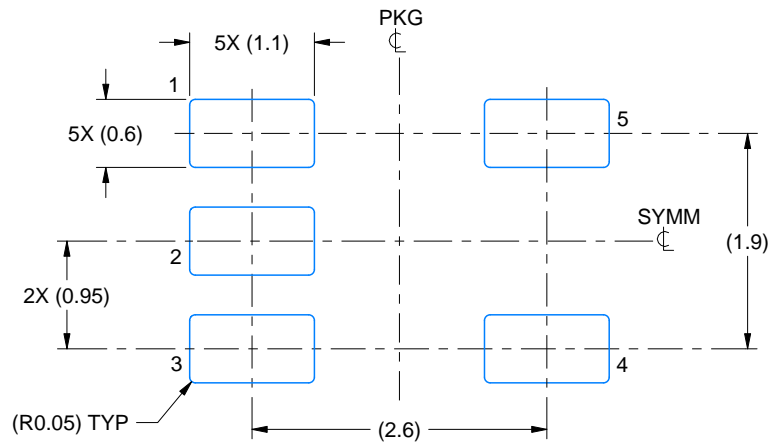


# EXAMPLE BOARD LAYOUT

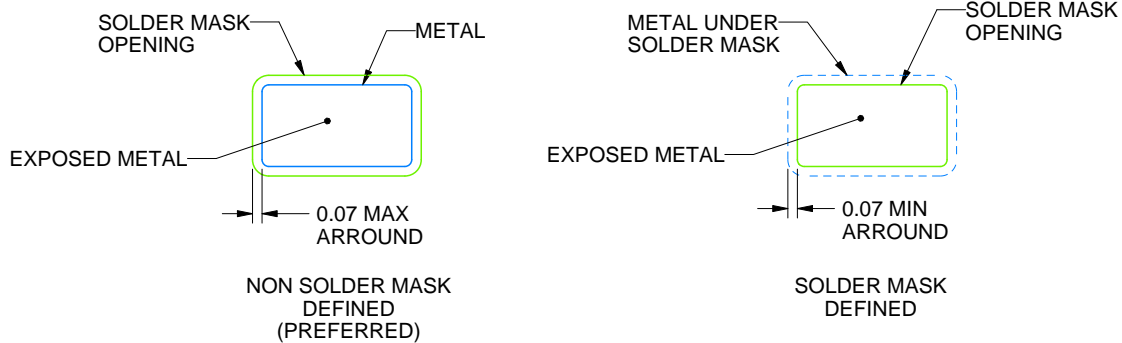
DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:15X



SOLDER MASK DETAILS

4214839/C 04/2017

NOTES: (continued)

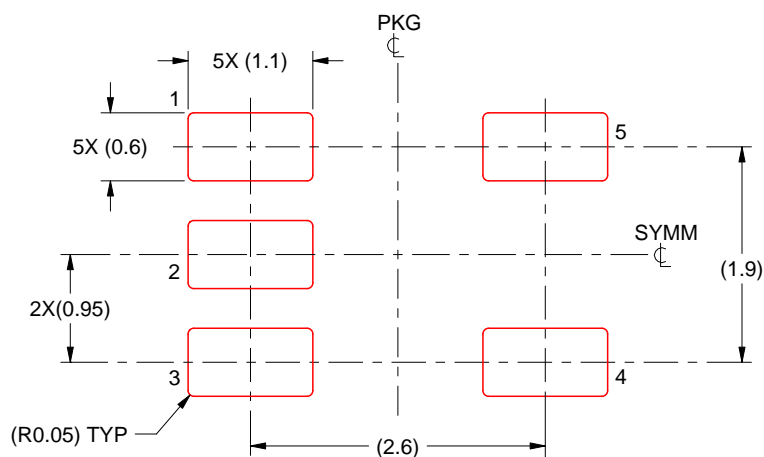
4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:15X

4214839/C 04/2017

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

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