16-Bit, 200ksps, Serial Sampling ADC

FEATURES

- **Sample Rate: 200ksps**
- **Input Ranges**
  Unipolar: 0V to 10V, 0V to 5V and 0V to 4V
  Bipolar: ±10V, ±5V and ±3.3V
- Serial I/O
- Single 5V Supply
- Power Dissipation: 65mW Typ
- Power Down Mode: 50µW
- SNR: 87dB Typ
- Operates with Internal or External Reference
- 28-Pin SSOP and 20-Pin SO Packages
- Improved 2nd Source to ADS7809 and AD977A

APPLICATIONS

- Industrial Process Control
- Multiplexed Data Acquisition Systems
- High Speed Data Acquisition for PCs
- Digital Signal Processing

DESCRIPTION

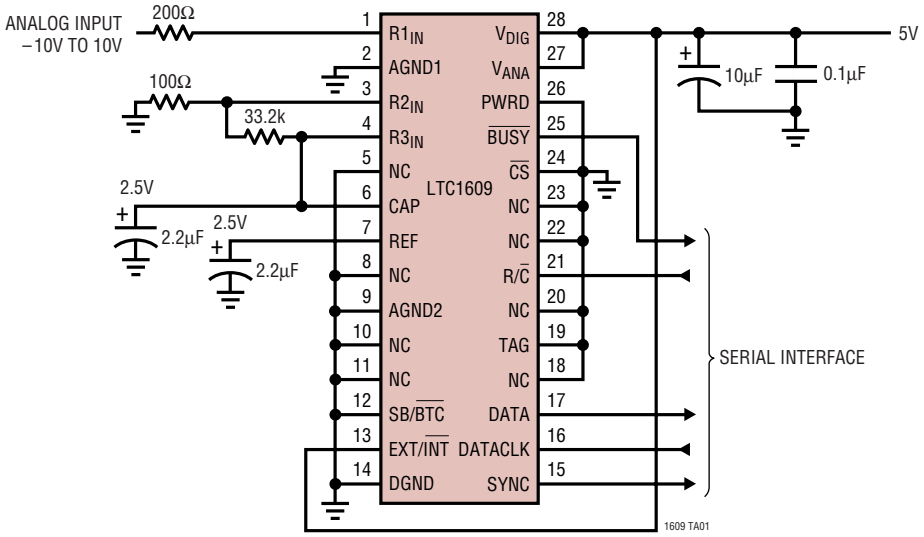
The LTC®1609 is a 200ksps, serial sampling 16-bit A/D converter that draws only 65mW (typical) from a single 5V supply. This easy-to-use device includes a sample-and-hold, a precision reference, a switched capacitor successive approximation A/D and trimmed internal clock.

The input range is specified for bipolar inputs of ±10V, ±5V and ±3.3V and unipolar inputs of 0V to 10V, 0V to 5V and 0V to 4V. Maximum DC specs include ±3LSB INL and 15-bit no missing codes over temperature. It has a typical signal-to-noise ratio of 87dB.

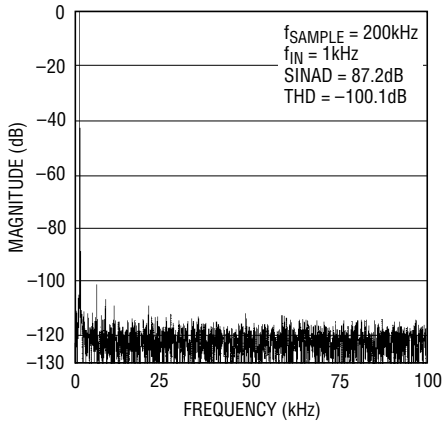
The ADC has a high speed serial interface. The serial output data can be clocked out using either the internal serial shift clock or be clocked out by an external shift clock. A separate convert start input (R/$\overline{C}$) and a data ready signal ($\overline{BUSY}$) ease connections to FIFOs, DSPs and microprocessors.

TYPICAL APPLICATION

200kHz, 16-Bit Serial Sampling ADC Configured for ±10V Inputs



Nonaveraged 4096 Point FFT Plot

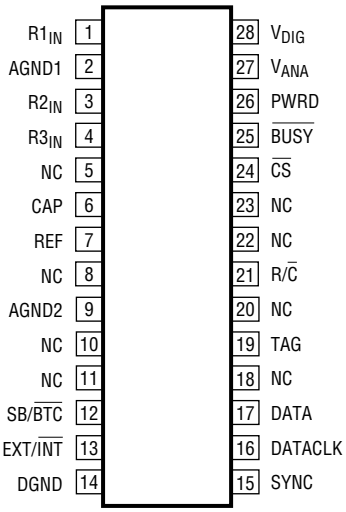


ABSOLUTE MAXIMUM RATINGS (Notes 1, 2)

V_{ANA} 7V
V_{DIG} to V_{ANA} 0.3V
V_{DIG} 7V
Ground Voltage Difference
DGND, AGND1 and AGND2 ..... ±0.3V
Analog Inputs (Note 3)
$R1_{IN}$, $R2_{IN}$, $R3_{IN}$ ..... ±25V
CAP ..... V_{ANA} + 0.3V to AGND2 – 0.3V
REF ..... Indefinite Short to AGND2
Momentary Short to V_{ANA}
Digital Input Voltage (Note 4) ..... DGND – 0.3V to 10V
Digital Output Voltage ..... DGND – 0.3V to V_{DIG} + 0.3V
Power Dissipation 500mW
Operating Ambient Temperature Range
LTC1609C ..... 0°C to 70°C
LTC1609I ..... –40°C to 85°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION

TOP VIEW



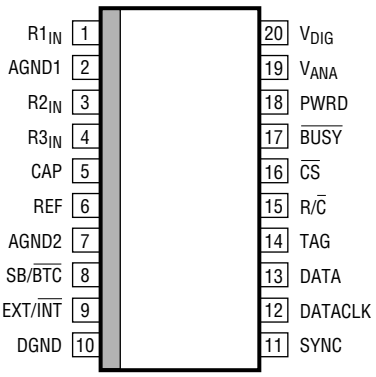
G PACKAGE
28-LEAD PLASTIC SSOP

T_{JMAX} = 125°C, θ_{JA} = 95°C/W

ORDER PART NUMBER

LTC1609CG
LTC1609IG

TOP VIEW



SW PACKAGE
20-LEAD PLASTIC SO

T_{JMAX} = 125°C, θ_{JA} = 130°C/W

ORDER PART NUMBER

LTC1609CSW
LTC1609ISW

Consult LTC Marketing for parts specified with wider operating temperature ranges.

CONVERTER CHARACTERISTICS

The ● indicates specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. With external reference (Notes 5, 6).

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Resolution		●	16			Bits
No Missing Codes		●	15			Bits
Transition Noise				0.9		LSB_{RMS}
Integral Linearity Error	(Note 7)	●			±3	LSB
Differential Linearity Error		●	–2		3	LSB
Bipolar Zero Error	External Reference = 2.5V (Note 8), Bipolar Ranges	●			±10	mV

CONVERTER CHARACTERISTICS

The ● indicates specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. With external reference (Notes 5, 6).

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Bipolar Zero Error Drift	Bipolar Ranges			±2		ppm/°C
Unipolar Zero Error	External Reference = 2.5V, Unipolar Ranges	●			±10	mV
Unipolar Zero Error Drift	Unipolar Ranges			±2		ppm/°C
Full-Scale Error Drift				±7		ppm/°C
Full-Scale Error	External Reference = 2.5V (Notes 12, 13)	●			±0.50	%
Full-Scale Error Drift	External Reference = 2.5V			±2		ppm/°C
Power Supply Sensitivity $V_{ANA} = V_{DIG} = V_{DD}$	V_{DD} = 5V ±5% (Note 9)				±8	LSB

ANALOG INPUT

The ● indicates specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN}	Analog Input Range (Note 9)	4.75V ≤ V_{ANA} ≤ 5.25V, 4.75V ≤ V_{DIG} ≤ 5.25V,	●		±10, 0V to 5V, etc. (See Tables 1a and 1b)		V
C_{IN}	Analog Input Capacitance				10		pF
R_{IN}	Analog Input Impedance				See Tables 1a and 1b		kΩ

DYNAMIC ACCURACY

(Notes 5, 14)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
S/(N + D)	Signal-to-(Noise + Distortion) Ratio	1kHz Input Signal (Note 14) 10kHz Input Signal 20kHz, –60dB Input Signal		87.5 87 30		dB dB dB
THD	Total Harmonic Distortion	1kHz Input Signal, First 5 Harmonics 10kHz Input Signal, First 5 Harmonics		–100 –94		dB dB
	Peak Harmonic or Spurious Noise	1kHz Input Signal 10kHz Input Signal		–102 –94		dB dB
	Full-Power Bandwidth	(Note 15)		275		kHz
	–3dB Input Bandwidth			1		MHz
	Aperture Delay			40		ns
	Aperture Jitter			Sufficient to Meet AC Specs		
	Transient Response	Full-Scale Step (Note 9)			2	µs
	Overvoltage Recovery	(Note 16)		150		ns

INTERNAL REFERENCE CHARACTERISTICS

The ● indicates specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 5)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{REF} Output Voltage	I_{OUT} = 0	●	2.470	2.500	2.520	V
V_{REF} Output Tempco	I_{OUT} = 0			±5		ppm/°C
Internal Reference Source Current				1		µA
External Reference Voltage for Specified Linearity	(Notes 9, 10)		2.30	2.50	2.70	V
External Reference Current Drain	External Reference = 2.5V (Note 9)	●			100	µA
CAP Output Voltage	I_{OUT} = 0			2.50		V

DIGITAL INPUTS AND DIGITAL OUTPUTS

The ● indicates specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 5)

SYMBOL	PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
V_{IH}	High Level Input Voltage	V_{DD} = 5.25V		●	2.4			V
V_{IL}	Low Level Input Voltage	V_{DD} = 4.75V		●			0.8	V
I_{IN}	Digital Input Current	V_{IN} = 0V to V_{DD}		●			±10	µA
C_{IN}	Digital Input Capacitance					5		pF
V_{OH}	High Level Output Voltage	V_{DD} = 4.75V	I_O = –10µA			4.5		V
			I_O = –200µA	●	4.0			V
V_{OL}	Low Level Output Voltage	V_{DD} = 4.75V	I_O = 160µA			0.05		V
			I_O = 1.6mA	●		0.10	0.4	V
I_{SOURCE}	Output Source Current	V_{OUT} = 0V				–10		mA
I_{SINK}	Output Sink Current	V_{OUT} = V_{DD}				10		mA

TIMING CHARACTERISTICS

The ● indicates specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
t_1	Convert Pulse Width	(Note 11)	●	40			ns
t_2	R/$\overline{C}$, $\overline{CS}$ to $\overline{BUSY}$ Delay	C_L = 25pF	●			80	ns
t_3	$\overline{BUSY}$ Low Time		●			3	µs
t_4	$\overline{BUSY}$ Delay After End of Conversion				100		ns
t_5	Aperture Delay				5		ns
t_6	Conversion Time		●			3	µs
t_7	Acquisition Time		●	2			µs
$t_6 + t_7$	Throughput Time		●			5	µs
t_8	R/$\overline{C}$ Low to DATACLK Delay				260		ns
t_9	DATACLK Period				150		ns
t_{10}	DATA Valid Setup Time		●	15			ns
t_{11}	DATA Valid Hold Time		●	40			ns
t_{12}	External DATACLK Period		●	50			ns
t_{13}	External DATACLK High		●	20			ns
t_{14}	External DATACLK Low		●	20			ns
t_{15}	R/$\overline{C}$, $\overline{CS}$ to External DATACLK Setup Time		●	15		t_{12}	ns
t_{16}	R/$\overline{C}$ to $\overline{CS}$ Setup Time		●	10			ns
t_{17}	External DATACLK to SYNC Delay		●	6		50	ns
t_{18}	External DATACLK to DATA Valid Delay		●	10		50	ns
t_{19}	$\overline{CS}$ to External DATACLK Rising Edge Delay		●	10			ns
t_{20}	Previous DATA Valid After $\overline{CS}$, R/$\overline{C}$ Low	(Note 9)	●	2.2			µs
t_{21}	$\overline{BUSY}$ to External DATACLK Setup Time	(Note 9)	●	5			ns
t_{22}	$\overline{BUSY}$ Falling Edge to Final External DATACLK	(Notes 10, 17)	●			1.2	µs
t_{23}	TAG Valid Setup Time		●	0			ns
t_{24}	TAG Valid Hold Time		●	15			ns

POWER REQUIREMENTS

The ● indicates specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{DD}	Positive Supply Voltage	(Notes 9, 10)		4.75		5.25	V
I_{DD}	Positive Supply Current	PWRD = Low	●		13	20	mA
P_{DIS}	Power Dissipation	PWRD = Low PWRD = High			65 50	100	mW µW

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: All voltage values are with respect to ground with DGND, AGND1 and AGND2 wired together (unless otherwise noted).

Note 3: When these pin voltages are taken below ground or above V_{ANA} = V_{DIG} = V_{DD}, they will be clamped by internal diodes. This product can handle input currents of greater than 100mA below ground or above V_{DD} without latch-up.

Note 4: When these pin voltages are taken below ground, they will be clamped by internal diodes. This product can handle input currents of 90mA below ground without latchup. These pins are not clamped to V_{DD}.

Note 5: V_{DD} = 5V, f_{SAMPLE} = 200kHz, t_r = t_f = 5ns unless otherwise specified.

Note 6: Linearity, offset and full-scale specifications apply for a V_{IN} input with respect to ground.

Note 7: Integral nonlinearity is defined as the deviation of a code from a straight line passing through the actual end points of the transfer curve. The deviation is measured from the center of the quantization band.

Note 8: Bipolar zero error is the offset voltage measured from –0.5 LSB when the output code flickers between 0000 0000 0000 0000 and 1111 1111 1111 1111. Unipolar zero error is the offset voltage measured when the output codes flickers between 0000. . .0000 and 0000. . .0001.

Note 9: Guaranteed by design, not subject to test.

Note 10: Recommended operating conditions.

Note 11: With $\overline{CS}$ low the falling R/$\overline{C}$ edge starts a conversion. If R/$\overline{C}$ returns high at a critical point during the conversion it can create small errors. For best results ensure that R/$\overline{C}$ returns high within 1.2µs after the start of the conversion.

Note 12: As measured with fixed 1% resistors shown in Figures 3a and 3b. Adjustable to zero with external potentiometer.

Note 13: Full-scale error is the worst-case of –FS or +FS untrimmed deviation from ideal first and last code transitions, divided by the transition voltage (not divided by the full-scale range) and includes the effect of offset error. For unipolar input ranges full-scale error is the deviation of the last code transition from ideal divided by the transiton voltage and includes the effect of offset error.

Note 14: All specifications in dB are referred to a full-scale ±10V input.

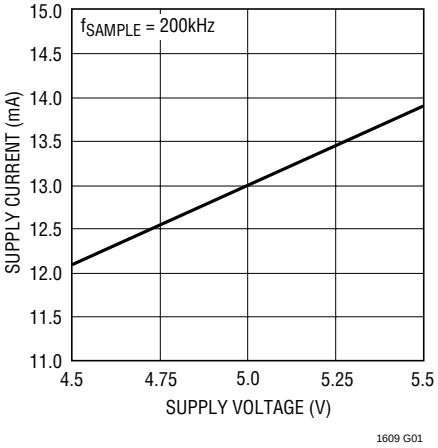
Note 15: Full-power bandwidth is defined as full-scale input frequency at which a signal-to-(noise + distortion) degrades to 60dB or 10 bits of accuracy.

Note 16: Recovers to specified performance after (2• FS) input overvoltage.

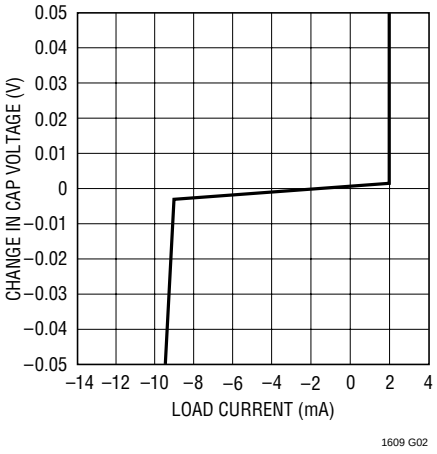
Note 17: When data is shifted out during a conversion, with an external data clock, complete the process within 1.2µs from the start of the conversion ($\overline{BUSY}$ falling). This will help keep any external disturbances from causing an error in the conversion result.

TYPICAL PERFORMANCE CHARACTERISTICS

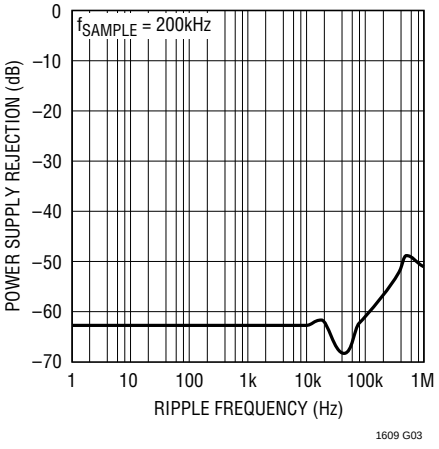
Supply Current vs Supply Voltage



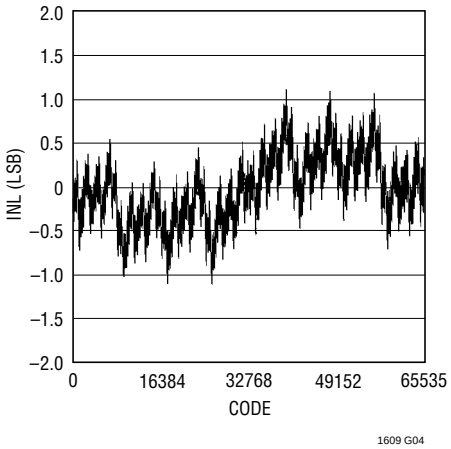
Change in CAP Voltage vs Load Current



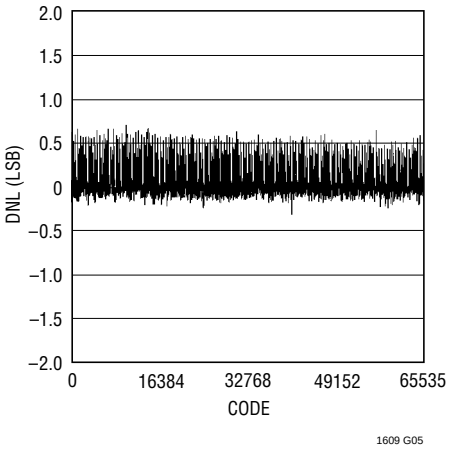
Power Supply Rejection vs Ripple Frequency



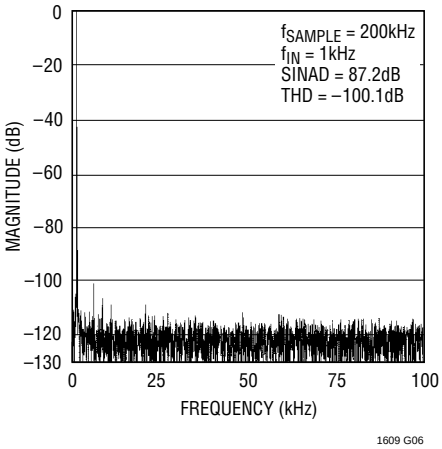
Typical INL Curve



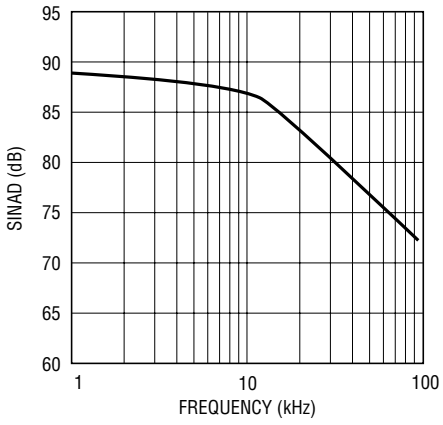
Typical DNL Curve



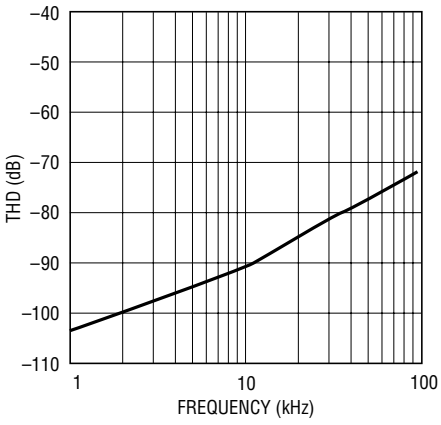
Nonaveraged 4096 Point FFT Plot



SINAD vs Input Frequency



THD vs Input Frequency



PIN FUNCTIONS (20-Pin SO/28-Pin SSOP)

$R1_{IN}$ (Pin 1/Pin 1): Analog Input. See Table 1 and Figure 1 for input range connections.

AGND1 (Pin 2/Pin 2): Analog Ground. Tie to analog ground plane.

$R2_{IN}$ (Pin 3/Pin 3): Analog Input. See Table 1 and Figure 1 for input range connections.

$R3_{IN}$ (Pin 4/Pin 4): Analog Input. See Table 1 and Figure 1 for input range connections.

NC (28-Pin SSOP Only—Pins 5, 8, 10, 11, 18, 20, 22, 23): No Connect.

CAP (Pin 5/Pin 6): Reference Buffer Output. Bypass with 2.2µF tantalum capacitor.

REF (Pin 6/Pin 7): 2.5V Reference Output. Bypass with 2.2µF tantalum capacitor. Can be driven with an external reference.

AGND2 (Pin 7/Pin 9): Analog Ground. Tie to analog ground plane.

SB/$\overline{\text{BTC}}$ (Pin 8/Pin 12): Select straight binary or two's complement data output format. Tie pin high for straight binary or tie low for two's complement format.

EXT/$\overline{\text{INT}}$ (Pin 9/Pin 13): Select external or internal clock for shifting out the output data. Tie the pin high to synchronize the output data to the clock that is applied to the DATACLK pin. If the pin is tied low, a convert command will start transmitting the output data from the previous conversion synchronized to 16 clock pulses that are outputted on the DATACLK pin.

DGND (Pin 10/Pin 14): Digital Ground.

SYNC (Pin 11/Pin 15): Sync Output. If EXT/$\overline{\text{INT}}$ is high, either a rising edge on R/$\overline{\text{C}}$ with $\overline{\text{CS}}$ low or a falling edge on $\overline{\text{CS}}$ with R/$\overline{\text{C}}$ high will output a pulse on SYNC synchronized to the external clock applied on the DATACLK pin.

DATACLK (Pin 12/Pin 16): Either an input or an output depending on the level set on EXT/$\overline{\text{INT}}$. The output data is synchronized to this clock. When EXT/$\overline{\text{INT}}$ is high an external shift clock is applied to this pin. If EXT/$\overline{\text{INT}}$ is taken low, 16 clock pulses are output during each conversion. The pin will stay low between conversions.

DATA (Pin 13/Pin 17): Serial Data Output. The output data is synchronized to the DATACLK and the format is determined by SB/$\overline{\text{BTC}}$. In the external shift clock mode, after 16 bits of data have been shifted out and $\overline{\text{CS}}$ is low and R/$\overline{\text{C}}$ is high, the level in the TAG pin will be outputted. This can be used to daisy-chain the serial data output from several LTC1609s. If EXT/$\overline{\text{INT}}$ is low, the output data is valid on both the rising and falling edge of the internal shift clock which is outputted on DATACLK. In between conversions, DATA will stay at the level of the TAG input when the conversion was started.

TAG (Pin 14/Pin 19): Tag input is used in the external clock mode. If EXT/$\overline{\text{INT}}$ is high, digital inputs applied to TAG will be shifted out on DATA delayed 16 DATACLK pulses as long as $\overline{\text{CS}}$ is low and R/C is high.

R/$\overline{\text{C}}$ (Pin 15/Pin 21): Read/$\overline{\text{Convert}}$ Input. With $\overline{\text{CS}}$ low, a falling edge on R/C puts the internal sample-and-hold into the hold state and starts a conversion. With $\overline{\text{CS}}$ low, a rising edge on R/$\overline{\text{C}}$ enables the serial output data.

$\overline{\text{CS}}$ (Pin 16/Pin 24): Chip Select. Internally OR'd with R/C. With R/$\overline{\text{C}}$ low, a falling edge on $\overline{\text{CS}}$ will initiate a conversion. With R/$\overline{\text{C}}$ high, a falling edge on $\overline{\text{CS}}$ will enable the serial output data.

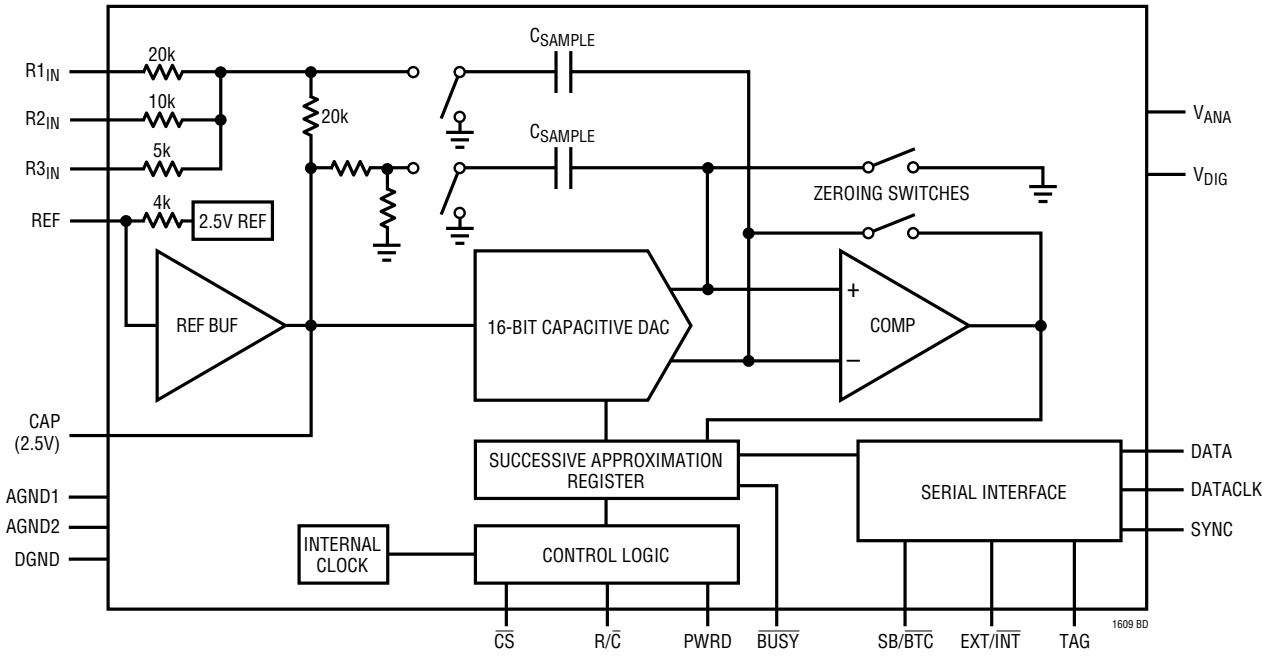
$\overline{\text{BUSY}}$ (Pin 17/Pin 25): Output Shows Converter Status. It is low when a conversion is in progress. Data valid on the rising edge of $\overline{\text{BUSY}}$. $\overline{\text{CS}}$ or R/$\overline{\text{C}}$ must be high when $\overline{\text{BUSY}}$ rises or another conversion will start without time for signal acquisition.

PWRD (Pin 18/Pin 26): Power Down Input. If the pin is tied high, conversions are inhibited and power consumption is reduced (10µA typ). Results from the previous conversion are maintained in the output shift register.

V_{ANA} (Pin 19/Pin 27): 5V Analog Supply. Bypass to ground with a 0.1µF ceramic and a 10µF tantalum capacitor.

V_{DIG} (Pin 20/Pin 28): 5V Digital Supply. Connect directly to V_{ANA}.

FUNCTIONAL BLOCK DIAGRAM



APPLICATIONS INFORMATION

Conversion Details

The LTC1609 uses a successive approximation algorithm and an internal sample-and-hold circuit to convert an analog signal to a 16-bit serial output. The ADC is complete with a precision reference and an internal clock. The control logic provides easy interface to microprocessors and DSPs. (Please refer to the Digital Interface section for timing information.)

Conversion start is controlled by the $\overline{CS}$ and R/$\overline{C}$ inputs. At the start of conversion the successive approximation register (SAR) is reset. Once a conversion cycle has begun it cannot be restarted.

During the conversion, the internal 16-bit capacitive DAC output is sequenced by the SAR from the most significant bit (MSB) to the least significant bit (LSB). Referring to Figure 1, V_{IN} is connected through the resistor divider to the sample-and-hold capacitor during the acquire phase and the comparator offset is nulled by the autozero switches. In this acquire phase, a minimum delay of 2µs will provide enough time for the sample-and-hold capacitor to acquire the analog signal. During the convert phase, the autozero switches open, putting the comparator into the compare mode. The input switch switches C_{SAMPLE} to ground, injecting the analog input charge onto the summing junction. This input charge is successively compared with the binary-weighted charges supplied by the capacitive DAC. Bit decisions are made by the high speed comparator. At

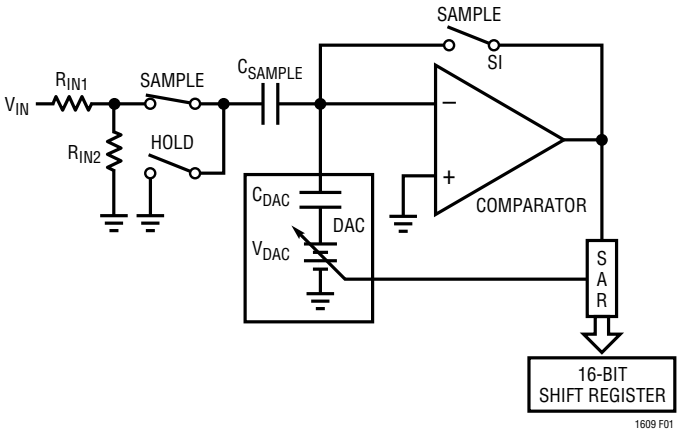


Figure 1. LTC1609 Simplified Equivalent Circuit

APPLICATIONS INFORMATION

the end of a conversion, the DAC output balances the V_{IN} input charge. The SAR contents (a 16-bit data word) that represents the V_{IN} are loaded into the 16-bit output shift register.

Driving the Analog Inputs

The LTC1609 analog input ranges, along with the nominal input impedances, are shown in Tables 1a and 1b. The inputs are overvoltage protected to ±25V. The input impedance can get as low as 10kΩ, therefore, it should be driven with a low impedance source. Wideband noise coupling into the input can be minimized by placing a 1000pF capacitor at the input as shown in Figure 2. An NPO-type capacitor gives the lowest distortion. Place the capacitor as close to the device input pin as possible. If an amplifier is to be used to drive the input, care should be taken to select an amplifier with adequate accuracy, linearity and noise for the application. The following list is a summary of the op amps that are suitable for driving the LTC1609. More detailed information is available in the Linear Technology data books and LinearView™ CD-ROM.

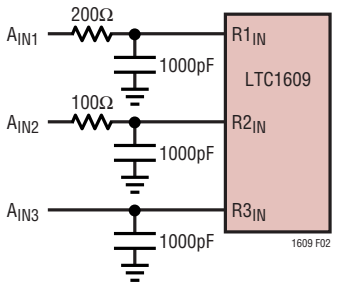


Figure 2. Analog Input Filtering

LT1007 - Low noise precision amplifier. 2.7mA supply current ±5V to ±15V supplies. Gain bandwidth product 8MHz. DC applications.

LT1097 - Low cost, low power precision amplifier. 300μA supply current. ±5V to ±15V supplies. Gain bandwidth product 0.7MHz. DC applications.

LT1227 - 140MHz video current feedback amplifier. 10mA supply current. ±5V to ±15V supplies. Low noise and low distortion.

LT1360 - 37MHz voltage feedback amplifier. 3.8mA supply current. ±5V to ±15V supplies. Good AC/DC specs.

LT1363 - 50MHz voltage feedback amplifier. 6.3mA supply current. Good AC/DC specs.

LT1364/LT1365 - Dual and quad 50MHz voltage feedback amplifiers. 6.3mA supply current per amplifier. Good AC/DC specs.

LT1468 - 90MHz, 22V/μs 16-bit accurate amplifier

LT1469 - Dual LT1468

Offset and Gain Adjustments

The LTC1609 is specified to operate with three unipolar and three bipolar input ranges. Pins $R1_{IN}$, $R2_{IN}$ and $R3_{IN}$ are connected as shown in Tables 1a and 1b for the different input ranges. The tables also list the nominal input impedance for each range. Table 1c shows the output codes for the ideal input voltages of each of the six input ranges.

The LTC1609 offset and full-scale errors have been trimmed at the factory with the external resistors shown in Figures 3a and 3b. This allows for external adjustment of offset and full scale in applications where absolute accuracy is important. The offset and gain adjustment circuits for the six input ranges are also shown in Figures 3a and 3b. To adjust the offset for a bipolar input range, apply an input voltage equal to –0.5LSB where 1LSB = (+FS – –FS)/65536 and change the offset resistor so the output code is changing between 1111 1111 1111 1111 and 0000 0000 0000 0000. The gain is trimmed by applying an input voltage of +FS – 1.5LSB and adjusting the gain trim resistor until the output code is changing between 0111 1111 1111 1110 and 0111 1111 1111 1111. In both cases the data is in two's complement format (SB/BTC = LOW)

To adjust the offset for a unipolar input range, apply an input voltage equal to +0.5LSB where 1LSB = +FS/65536. Then adjust the offset trim resistor until the output code changes between 0000 0000 0000 0000 and 0000 0000 0000 0001. To adjust the gain, apply an input voltage equal to +FS – 1.5LSB and vary the gain trimming resistor until the output code is changing between 1111 1111 1111 1110 and 1111 1111 1111 1111. In the unipolar case, the data is in straight binary format (SB/$\overline{BTC}$ = HIGH). Figures 4a and 4b show the transfer characteristics of the LTC1609.

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APPLICATIONS INFORMATION

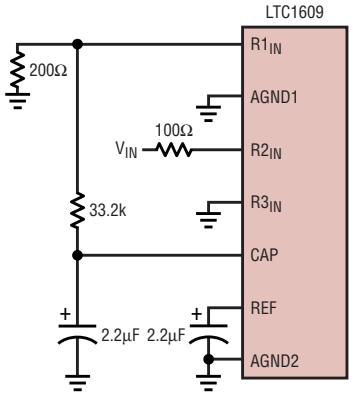
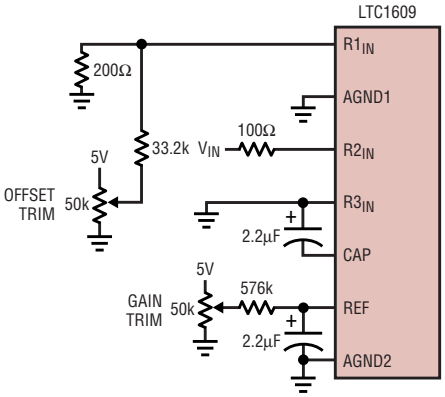
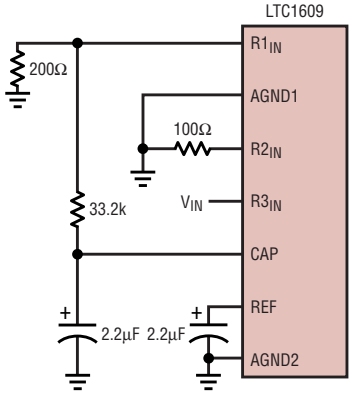
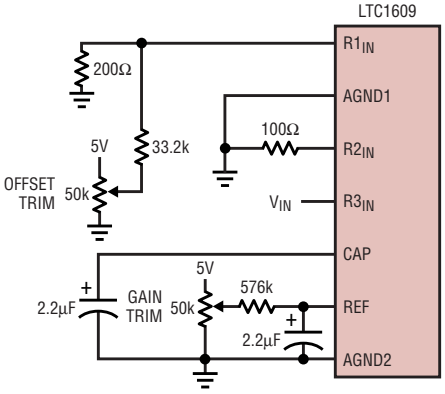
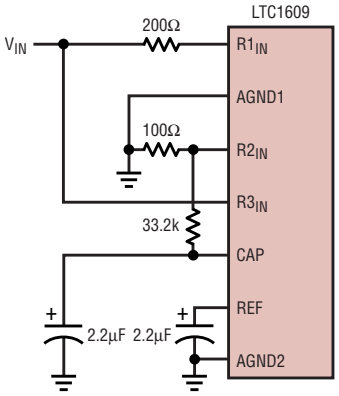
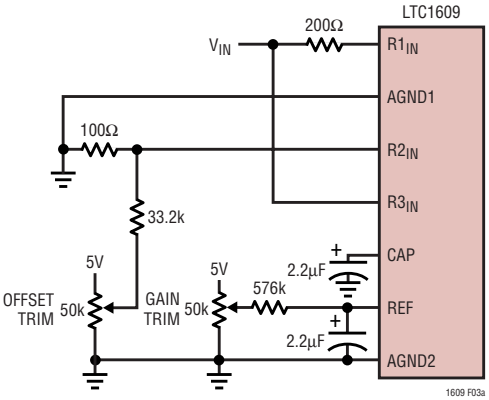
INPUT RANGE	WITHOUT TRIM	WITH TRIM (ADJUST OFFSET FIRST AT 0V, THEN ADJUST GAIN)
0V TO 10V		
0V TO 5V		
0V TO 4V		

Figure 3a. Offset/Gain Circuits for Unipolar Input Ranges

Table 1a. Analog Input Range Connections for Figure 3a

ANALOG INPUT RANGE	CONNECT $R1_{IN}$ VIA 200Ω TO	CONNECT $R2_{IN}$ VIA 100Ω TO	CONNECT $R3_{IN}$ TO	INPUT IMPEDANCE
0V to 10V	AGND	V_{IN}	AGND	13.3kΩ
0V to 5V	AGND	AGND	V_{IN}	10kΩ
0V to 4V	V_{IN}	AGND	V_{IN}	10.7kΩ

APPLICATIONS INFORMATION

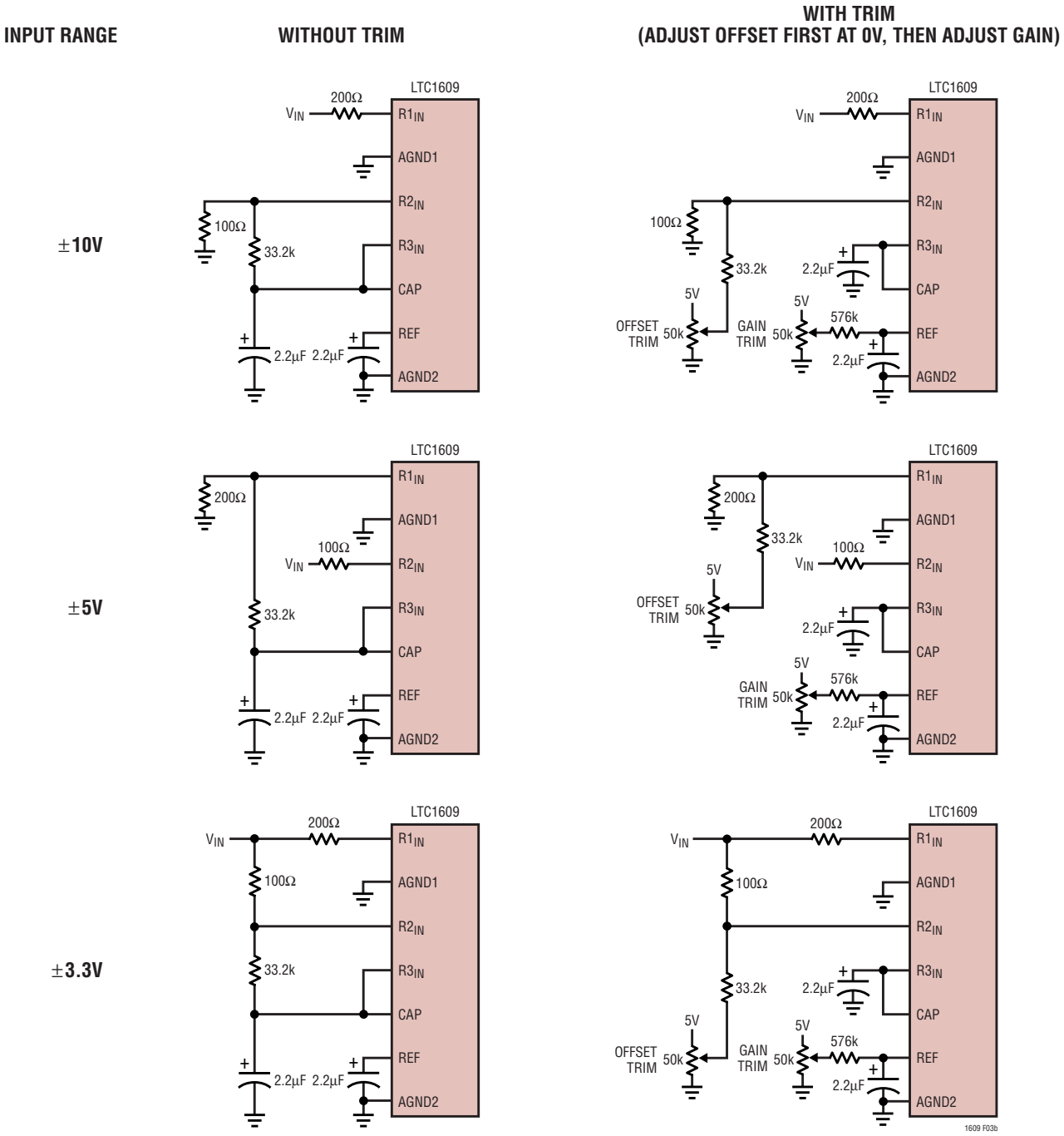


Figure 3b. Offset/Gain Circuits for Bipolar Input Ranges

Table 1b. Analog Input Range Connections for Figure 3b

ANALOG INPUT RANGE	CONNECT $R1_{IN}$ VIA 200Ω TO	CONNECT $R2_{IN}$ VIA 100Ω TO	CONNECT $R3_{IN}$ TO	INPUT IMPEDANCE
±10V	V_{IN}	AGND	CAP	22.9kΩ
±5V	AGND	V_{IN}	CAP	13.3kΩ
±3.3V	V_{IN}	V_{IN}	CAP	10.7kΩ

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Table 1c. LTC1609 Output Codes for Ideal Input Voltages

DESCRIPTION	ANALOG INPUT						TWO'S COMPLEMENT (SB/$\overline{BTC}$ LOW)	STRAIGHT BINARY (SB/$\overline{BTC}$ HIGH)
Full-Scale Range	±10V	±5V	±3.34	0V to 10V	0V to 5V	0V to 4V		
Least Significant Bit	305µV	153µV	102µV	153µV	76µV	61µV		
+Full Scale (FS – 1LSB)	9.999695V	4.999847V	3.339898V	9.999847V	4.999924V	3.999939V	0111 1111 1111 1111	1111 1111 1111 1111
Midscale	0V	0V	0V	5V	2.5V	2V	0000 0000 0000 0000	1000 0000 0000 0000
1LSB Below Midscale	–305µV	–153µV	–102µV	4.999847V	2.499924V	1.999939V	1111 1111 1111 1111	0111 1111 1111 1111
–Full Scale	–10V	–5V	–3.340000V	0V	0V	0V	1000 0000 0000 0000	0000 0000 0000 0000

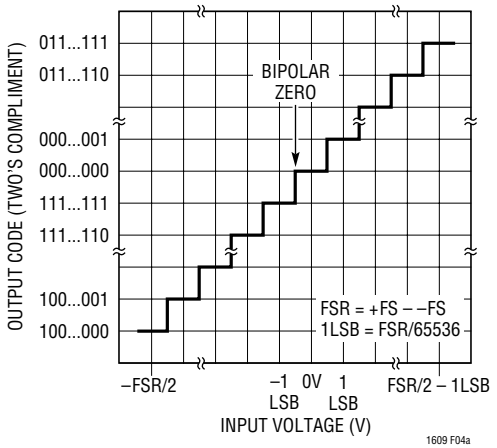

Figure 4a. LTC1609 Bipolar Transfer Characteristics

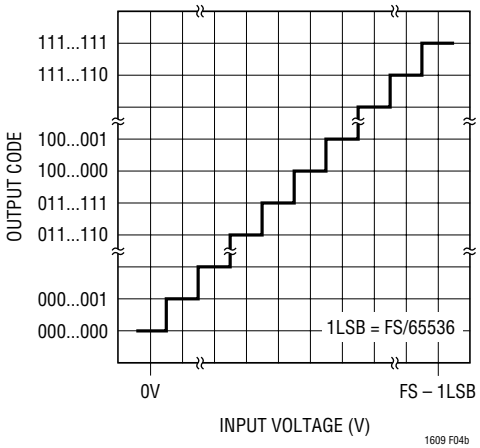

Figure 4b. LTC1609 Unipolar Transfer Characteristics

The ideal ±FS value for the ±3.3V range is 3.340000V – 1LSB and –3.340000V, respectively. The external 33.2k resistor that is connected between the CAP pin and the $R2_{IN}$ pin, slightly attenuates the input signal applied to $R2_{IN}$. Without the 33.2k resistor the ±FS value would be 3.333333V – 1LSB and –3.333333V (zero volt offset), respectively.

DC Performance

One way of measuring the transition noise associated with a high resolution ADC is to use a technique where a DC signal is applied to the input of the ADC and the resulting output codes are collected over a large number of conversions. For example in Figure 5 the distribution of output code is shown for a DC input that has been digitized 4096 times. The distribution is Gaussian and the RMS code transition is about 0.9LSB.

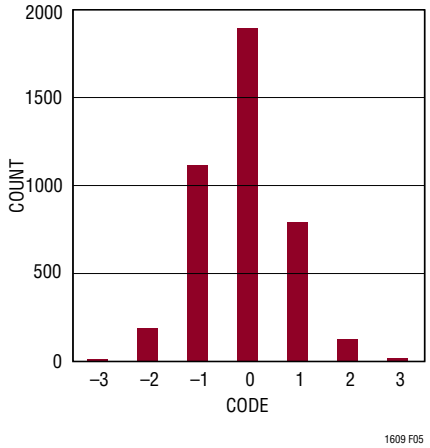

Figure 5. Histogram for 4096 Conversions

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Dynamic Performance

FFT (Fast Fourier Transform) test techniques are used to test the ADC's frequency response, distortion and noise at the rated throughput. By applying a low distortion sine wave and analyzing the digital output using an FFT algorithm, the ADC's spectral content can be examined for frequencies outside the fundamental. Figure 6 shows a typical LTC1609 FFT plot which yields a SINAD of 87.2dB and THD of –100dB.

Signal-to-Noise Ratio

The Signal-to-Noise and Distortion Ratio (SINAD) is the ratio between the RMS amplitude of the fundamental input frequency to the RMS amplitude of all other frequency components at the A/D output. The output is band limited to frequencies from above DC and below half the sampling frequency. Figure 6 shows a typical SINAD of 87.2dB with a 200kHz sampling rate and a 1kHz input.

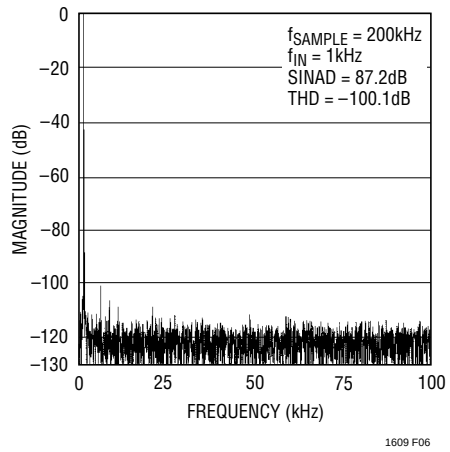

Figure 6. LTC1609 Nonaveraged 4096 Point FFT Plot

Total Harmonic Distortion

Total Harmonic Distortion (THD) is the ratio of the RMS sum of all harmonics of the input signal to the fundamental itself. The out-of-band harmonics alias into the frequency band between DC and half the sampling frequency. THD is expressed as:

$$THD = 20\log\frac{\sqrt{V_2^2 + V_3^2 + V_4^2 \ldots + V_N^2}}{V_1}$$

where V_1 is the RMS amplitude of the fundamental frequency and V_2 through V_N are the amplitudes of the second through Nth harmonics.

Internal Voltage Reference

The LTC1609 has an on-chip, temperature compensated, curvature corrected, bandgap reference, which is factory trimmed to 2.50V. The full-scale range of the ADC scales with V_{REF}. The output of the reference is connected to the input of a unity-gain buffer through a 4k resistor (see Figure 7). The input to the buffer or the output of the reference is available at REF. The internal reference can be overdriven with an external reference if more accuracy is needed. The buffer output drives the internal DAC and is available at CAP. The CAP pin can be used to drive a steady DC load of less than 2mA. Driving an AC load is not recommended because it can cause the performance of the converter to degrade.

For minimum code transition noise the REF pin and the CAP pin should each be decoupled with a capacitor to filter wideband noise from the reference and the buffer (2.2µF tantalum).

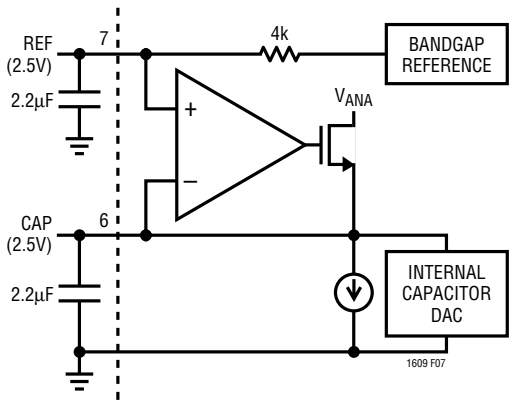

Figure 7. Internal or External Reference Source

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Power Shutdown

When the PWRD pin is tied high, power consumption drops to a typical value of 50µW from a specified maximum of 100mW. In the power shutdown mode, the result from the previous conversion is still available in the internal shift register, assuming the data had not been clocked out before going into power shutdown.

The internal reference buffer and the reference are shut down, so the power-up recovery time will be dependent upon how fast the bypass capacitors on these pins can be charged. If the internal reference is used, the 4k resistor in series with the output and the external bypass capacitor, typically 2.2µF, will be the main time constant for the power-up recovery time. If an external reference is used, the reference buffer output will be able to ramp from 0V to 2.5V in 1ms, while charging a typical bypass capacitor of 2.2µF. The recovery time will be less if the bypass capacitor has not completely discharged.

DIGITAL INTERFACE

Internal Conversion Clock

The ADC has an internal clock that is trimmed to achieve a typical conversion time of 2.7µs. No external adjustments are required and, with the typical acquisition time of 1.5µs, throughput performance of 200ksps is assured.

Timing and Control

Conversion start and data read are controlled by two digital inputs: $\overline{CS}$ and R/$\overline{C}$. To start a conversion and put the sample-and-hold into the hold mode bring $\overline{CS}$ and R/$\overline{C}$ low for no less than 40ns. Once initiated it cannot be restarted until the conversion is complete. Converter status is indicated by the $\overline{BUSY}$ output and this is low while the conversion is in progress.

The conversion result is clocked out serially on the DATA pin. It can be synchronized by using the internal data clock or by using an external clock provided by the user. Tying the EXT/$\overline{INT}$ pin high puts the LTC1609 in the external clock mode and the DATACLK pin is a digital input. Tying the EXT/$\overline{INT}$ pin low puts the part in the internal clock mode and the DATACLK pin becomes a digital output.

Internal Clock Mode

With the EXT/$\overline{INT}$ pin tied low, the LTC1609 provides the data clock on the DATACLK pin. The timing diagram is shown in Figure 8. Typically, $\overline{CS}$ is tied low and the R/$\overline{C}$ pin is used to start a conversion. During the conversion a 16-bit word will be shifted out MSB-first on the DATA pin. This word represents the result from the previous conversion. The DATACLK pin outputs 16 clock pulses used to synchronize the data. The output data is valid on both the rising and falling edges of the clock. After the LSB bit has been clocked out, the DATA pin will take on the state of the TAG pin at the start of the conversion. The DATACLK pin goes low until the next conversion is requested. The data clock is derived from the internal conversion clock. To avoid errors from occurring during the current conversion, minimize the loading on the DATACLK pin and the DATA pin. For the best conversion results the external clock mode is recommended.

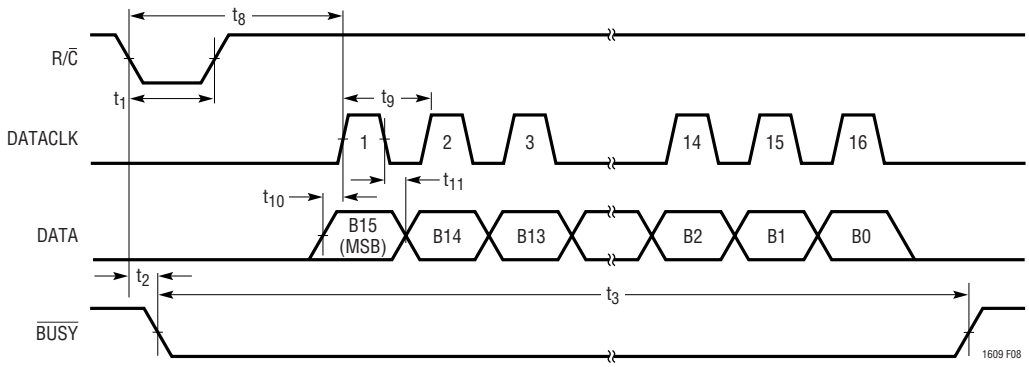

Figure 8. Serial Data Timing Using Internal Clock ($\overline{CS}$, EXT/$\overline{INT}$ and TAG Tied Low)

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External Clock Mode

With the EXT/$\overline{INT}$ pin tied high, the DATACLK pin becomes a digital input and the LTC1609 can accept an externally supplied data clock. There are several ways in which the conversion results can be clocked out. The data can be clocked out during or after a conversion with a continuous or discontinuous data clock. Figures 9 to 12 show the timing diagram for each of these methods.

External Discontinuous Data Clock Data Read After the Conversion

Figure 9 shows how the result from the current conversion can be read out after the conversion has been completed. The externally supplied data clock is running discontinuously. R/$\overline{C}$ is used to initiate a conversion with $\overline{CS}$ tied low. The conversion starts on the falling edge of R/$\overline{C}$. R/$\overline{C}$ should be returned high within 1.2µs to prevent the transition from disturbing the conversion. After the conversion has been completed ($\overline{BUSY}$ returning high), a pulse on the SYNC pin will be generated on the rising edge of DATACLK #0. The SYNC output can be captured on the falling edge of DATACLK #0 or on the rising edge of DATACLK #1. After the rising edge of DATACLK #1, the SYNC output will go low and the MSB will be clocked out on the DATA pin. This bit can be latched on the falling edge of DATACLK #1 or on the rising edge of DATACLK #2. The LSB will be valid on the falling edge of DATACLK #16 or the rising edge of DATACLK #17. After the rising edge of DATACLK #17 the DATA pin will take on the value of the TAG pin that occurred at the rising edge of DATACLK #1. A minimum of 17 clock pulses are required if the data is captured on falling clock edges.

Using the highest frequency permitted for DATACLK (20MHz), shifting the data out after the conversion will not degrade the 200kHz throughput. This method minimizes the possible external disturbances that can occur while a conversion is in progress and will yield the best performance.

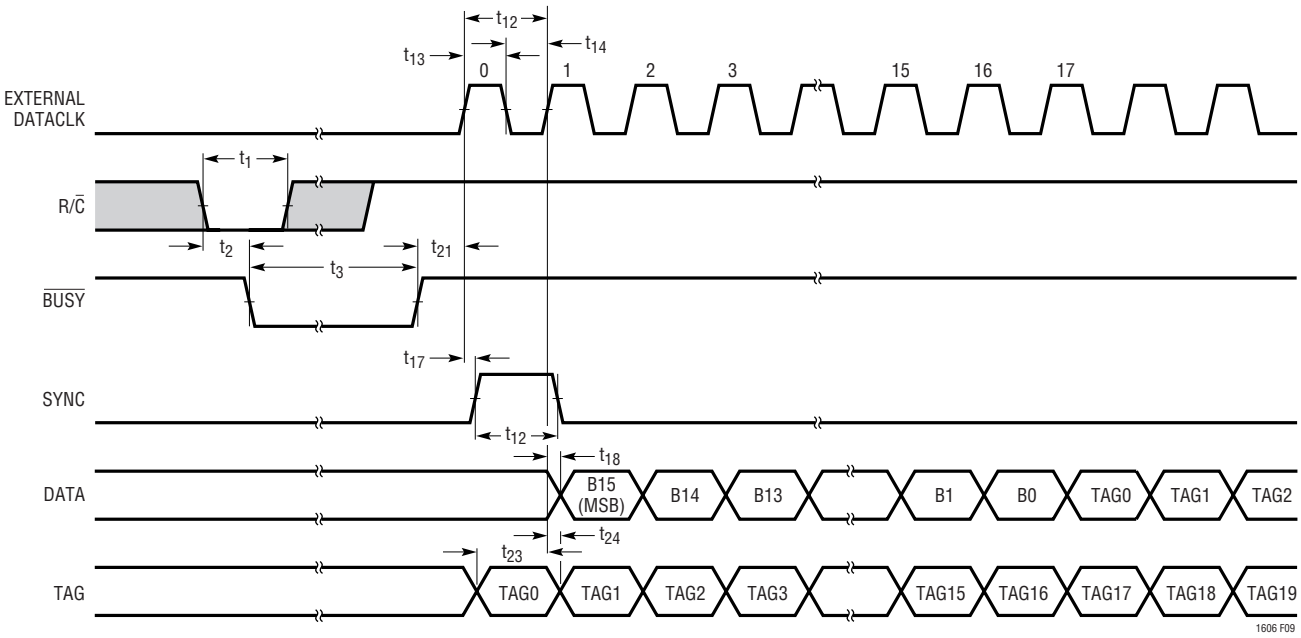

Figure 9. Conversion and Read Timing Using an External Discontinuous Data Clock (EXT/$\overline{INT}$ Tied High, $\overline{CS}$ Tied Low). Read Conversion Result After the Conversion

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External Data Clock Data Read After the Conversion

Figure 10 shows how the result from the current conversion can be read out after the conversion has been completed. The externally supplied data clock is running continuously. $\overline{CS}$ and R/$\overline{C}$ are first used together to initiate a conversion and then $\overline{CS}$ is used to read the result. The conversion starts on the falling edge of $\overline{CS}$ with R/$\overline{C}$ low. Both $\overline{CS}$ and R/$\overline{C}$ should be returned high within 1.2µs to prevent the transition from disturbing the conversion. After the conversion has been completed ($\overline{BUSY}$ returning high), a pulse on the SYNC pin will be generated after the first rising edge of DATACLK #1 that occurs after $\overline{CS}$ goes low (R/$\overline{C}$ high). The SYNC output can be captured on the falling edge of DATACLK #1 or on the rising edge of DATACLK #2. After the rising edge of DATACLK #2, the SYNC output will go low and the MSB will be clocked out on the DATA pin. This bit can be latched on the falling edge of DATACLK #2 or on the rising edge of DATACLK #3. The LSB will be valid on the falling edge of DATACLK #17 or the rising edge of DATACLK #18. After the rising edge of DATACLK #18 the DATA pin will take on the value of the TAG pin that occurred at the rising edge of DATACLK #2.

Using the highest frequency permitted for DATACLK (20MHz), shifting the data out after the conversion will not degrade the 200kHz throughput.

External Discontinuous Data Clock Data Read During the Conversion

Figure 11 shows how the result from the previous conversion can be read out during the current conversion. The externally supplied data clock is running discontinuously. R/$\overline{C}$ is used to initiate a conversion with $\overline{CS}$ tied low. The conversion starts on the falling edge of R/$\overline{C}$. R/$\overline{C}$ should be returned high within 1.2µs to prevent the transition from disturbing the conversion. A pulse on the SYNC pin will be generated on rising edge of DATACLK #0. The SYNC output can be captured on the falling edge of DATACLK #0 or on the rising edge of DATACLK #1. After the rising edge of DATACLK #1, the SYNC output will go low and the MSB will be clocked out on the DATA pin. This bit can be latched on the falling edge of DATACLK #1 or on the rising edge of DATACLK #2. The LSB will be valid on the falling edge of DATACLK #16. Another clock pulse would be needed if the LSB is captured on a rising edge. A minimum of 17 clock pulses are required if the data is captured on falling clock edges.

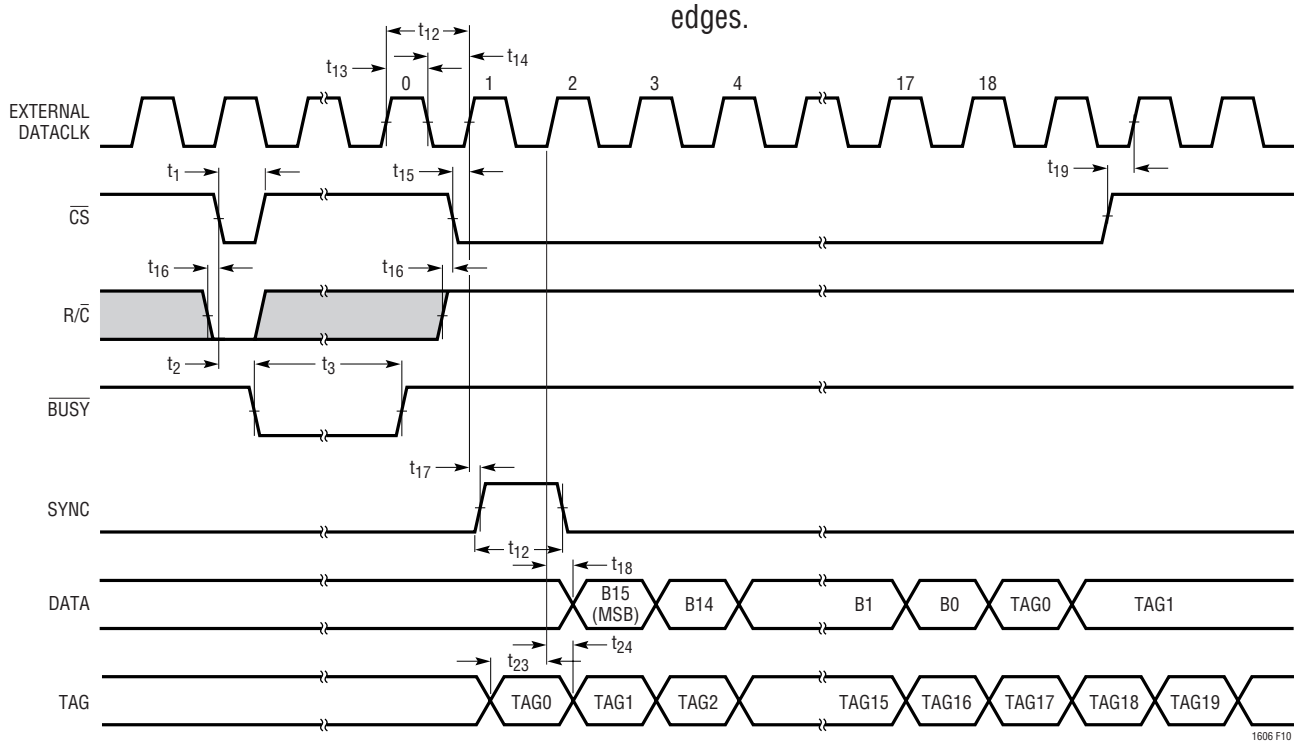

Figure 10. Conversion and Read Timing with External Clock (EXT/$\overline{INT}$ Tied High). Read After Conversion

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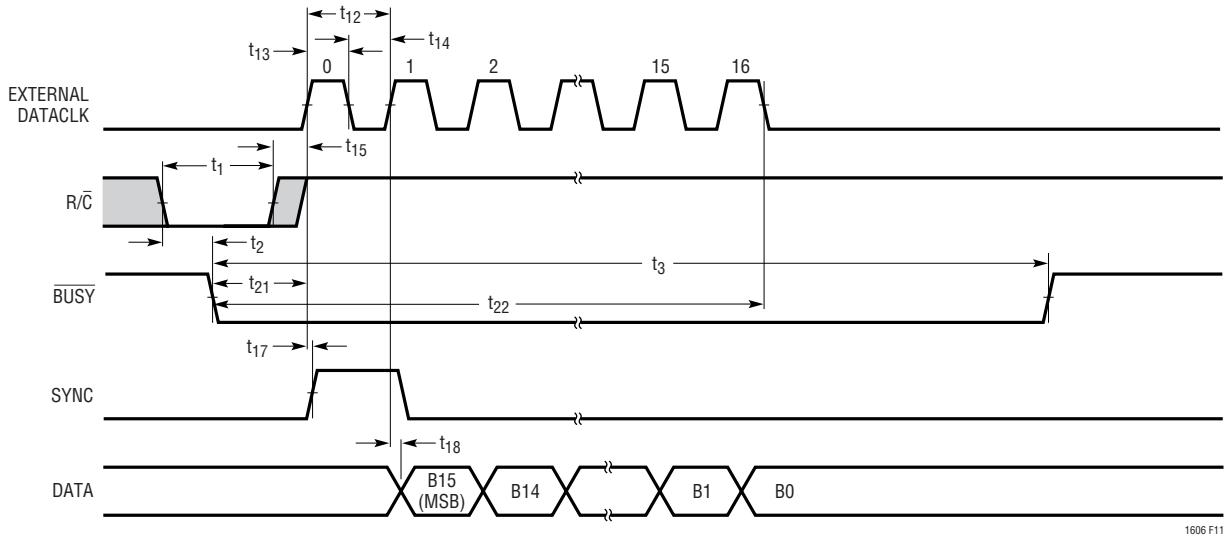

Figure 11. Conversion and Read Timing Using a Discontinuous Data Clock (EXT/$\overline{INT}$ Tied High, $\overline{CS}$ Tied Low). Read Previous Conversion Result During the Conversion. For Best Performance, Complete Read in Less Than 1.2µs

To minimize the possible external disturbances that can occur while a conversion is in progress, the data needs to be shifted out within 1.2µs from the start of the conversion. Using the maximum data clock frequency of 20MHz will ensure this condition is met.

External Data Clock Data Read During the Conversion

Figure 12 shows how the result from the previous conversion can be read out during the current conversion. The externally supplied data clock is running continuously. $\overline{CS}$ and R/$\overline{C}$ are used to initiate a conversion and read the data from the previous conversion. The conversion starts on the falling edge of $\overline{CS}$ after R/$\overline{C}$ is low. A pulse on the SYNC pin will be generated on the first rising edge of DATACLK #1 after R/$\overline{C}$ has returned high. The SYNC output can be captured on the falling edge of DATACLK #1 or on the rising edge of DATACLK #2. After the rising edge of DATACLK #2 the SYNC output will go low and the MSB will be clocked out on the DATA pin. This bit can be latched on the falling edge of DATACLK #2 or on the rising edge of DATACLK #3. The LSB will be valid on the falling edge of DATACLK #17 or the rising edge of DATACLK #18. After the rising edge of DATACLK #18 the DATA pin will take on the value of the TAG pin that occurred at the rising edge of DATACLK #2.

To minimize the possible external disturbances that can occur while a conversion is in progress, the data needs to be shifted out within 1.2µs from the start of the conversion. Using the maximum data clock frequency of 20MHz will ensure this condition is met. Since there is no throughput penalty for clocking the data out after the conversion, clocking the data out during the conversion is not recommended.

Use of the TAG Input

The TAG input pin is used to daisy-chain multiple converters. This is useful for applications where hardware constraints may limit the number of lines needed to interface to a large number of converters. This mode of operation works only using the external clock method of shifting out the data.

Figure 13 shows how this feature can be used. R/$\overline{C}$, $\overline{CS}$ and the DATACLK are tied together on both LTC1609s. $\overline{CS}$ can be grounded if a discontinuous data clock is used. A falling edge on R/$\overline{C}$ will allow both LTC1609s to capture their respective analog input signals simultaneously. Once the conversion has been completed the external data clock DCLK is started. The MSB from device #1 will be valid after the rising edge of DCLK #1. Once the LSB from device #1 has been shifted out on the rising edge of DCLK #16, a null

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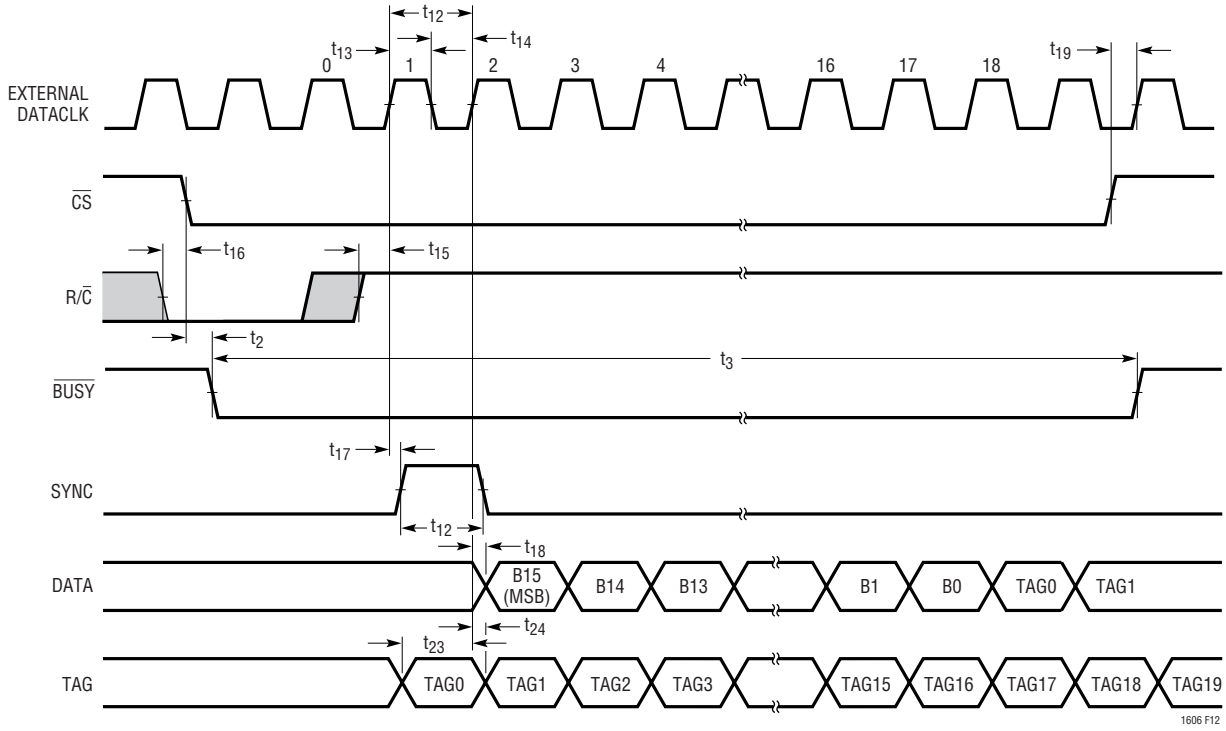

Figure 12. Conversion and Read Timing Using an External Data Clock (EXT/$\overline{INT}$ Tied High). Read Previous Conversion Result During the Conversion. For Best Performance, Complete Read in Less Than 1.2µs

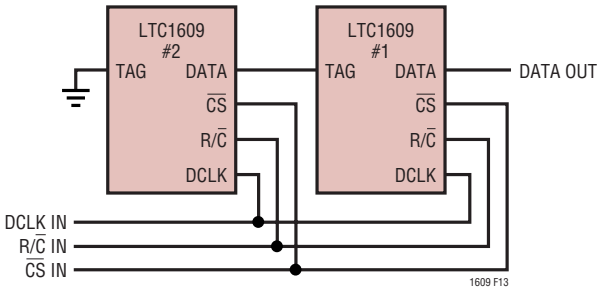

Figure 13. Two LTC1609s Cascaded Together Using the TAG Input

bit will be shifted out on the following clock pulse before the MSB from device #2 becomes available (Figure 14). The reason for this is the MSB from device #2 will not be valid soon enough to meet the minimum setup time of device #1's TAG input. A minimum of 34 clock pulses are needed to shift out the results from both LTC1609s assuming the data is captured on the falling clock edge. Using the highest frequency permitted for DATACLK (20MHz), a 200kHz throughput can still be achieved.

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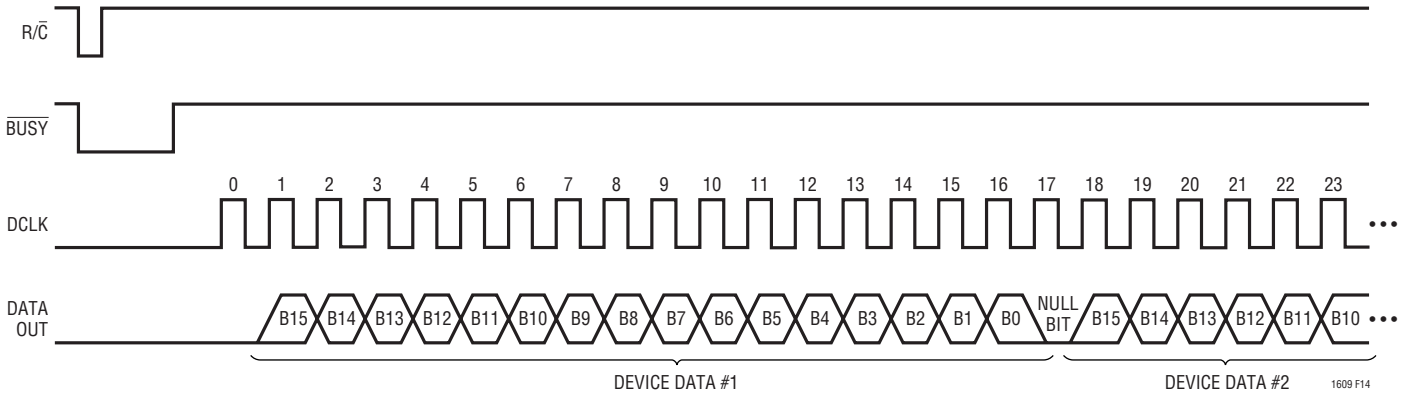

Figure 14. Data Output from Cascading Two ($\overline{CS}$ = Low, TAG (#2) = Low) LTC1609s Together

Output Data Format

The SB/$\overline{BTC}$ pin controls the format of the serial digital output word. With the pin tied high the format is straight binary. With the pin tied low the data format is two's complement. See Table 1c.

Board Layout, Power Supplies and Decoupling

Wire wrap boards are not recommended for high resolution or high speed A/D converters. To obtain the best performance from the LTC1609, a printed circuit board is required. Layout for the printed circuit board should ensure the digital and analog signal lines are separated as much as possible. In particular, care should be taken not to run any digital track alongside an analog signal track or underneath the ADC. The analog input should be screened by AGND.

Pay particular attention to the design of the analog and digital ground planes. Placing the bypass capacitor as close as possible to the V_{DIG} and V_{ANA} pins, the REF pin and reference buffer output is very important. Low impedance common returns for these bypass capacitors are essential to low noise operation of the ADC, and the foil width for these tracks should be as wide as possible. Also, since any potential difference in grounds between the signal source and ADC appears as an error voltage in series with the input signal, attention should be paid to reducing the ground circuit impedance as much as possible. The digital output latches and the onboard sampling clock have been placed on the digital ground plane. The two ground planes are tied together at the power supply ground connection.

A "postage stamp" (1.6in $\times$ 1.5in) evaluation board is available and allows fast in-situ evaluation of the LTC1609. See Figures 15a through 15d, inclusive.

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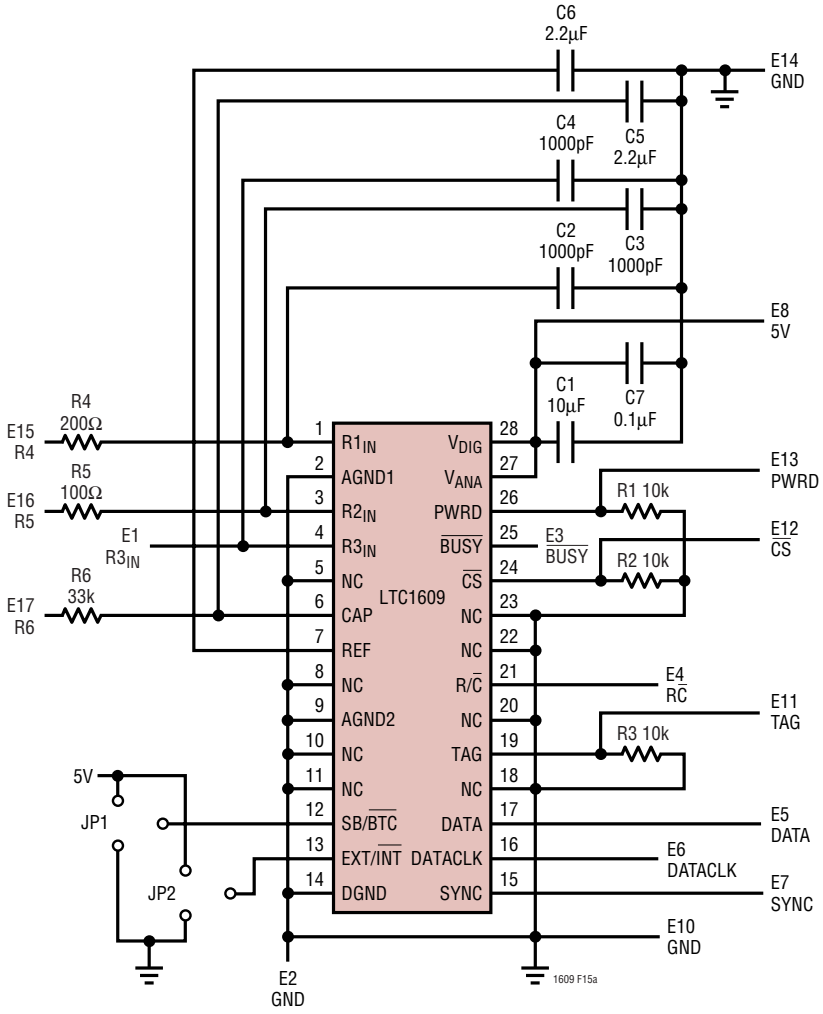


Figure 15a. LTC1609 "Postage Stamp" Evaluation Circuit Schematic

APPLICATIONS INFORMATION

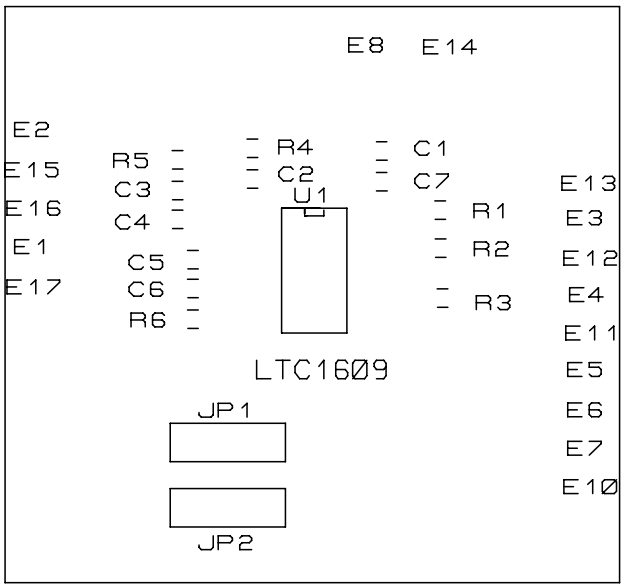


Figure 15b. LTC1609 "Postage Stamp" Evaluation Board Silkscreen (2× Actual Size)

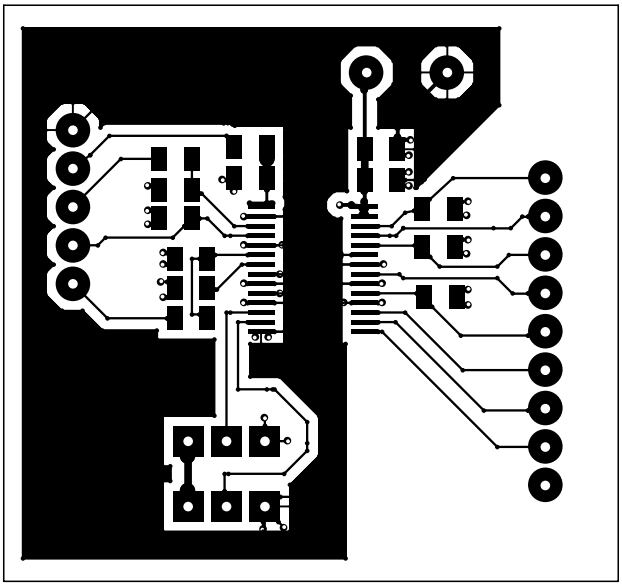


Figure 15c. LTC1609 "Postage Stamp" Evaluation Board Top Metal Layer (2× Actual Size)

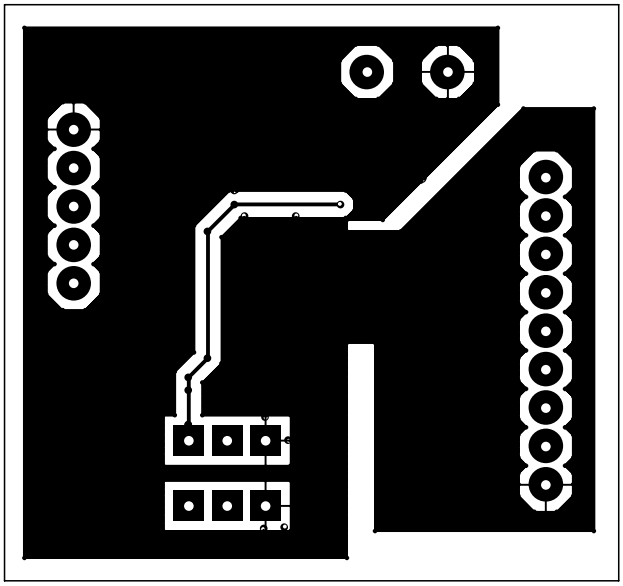
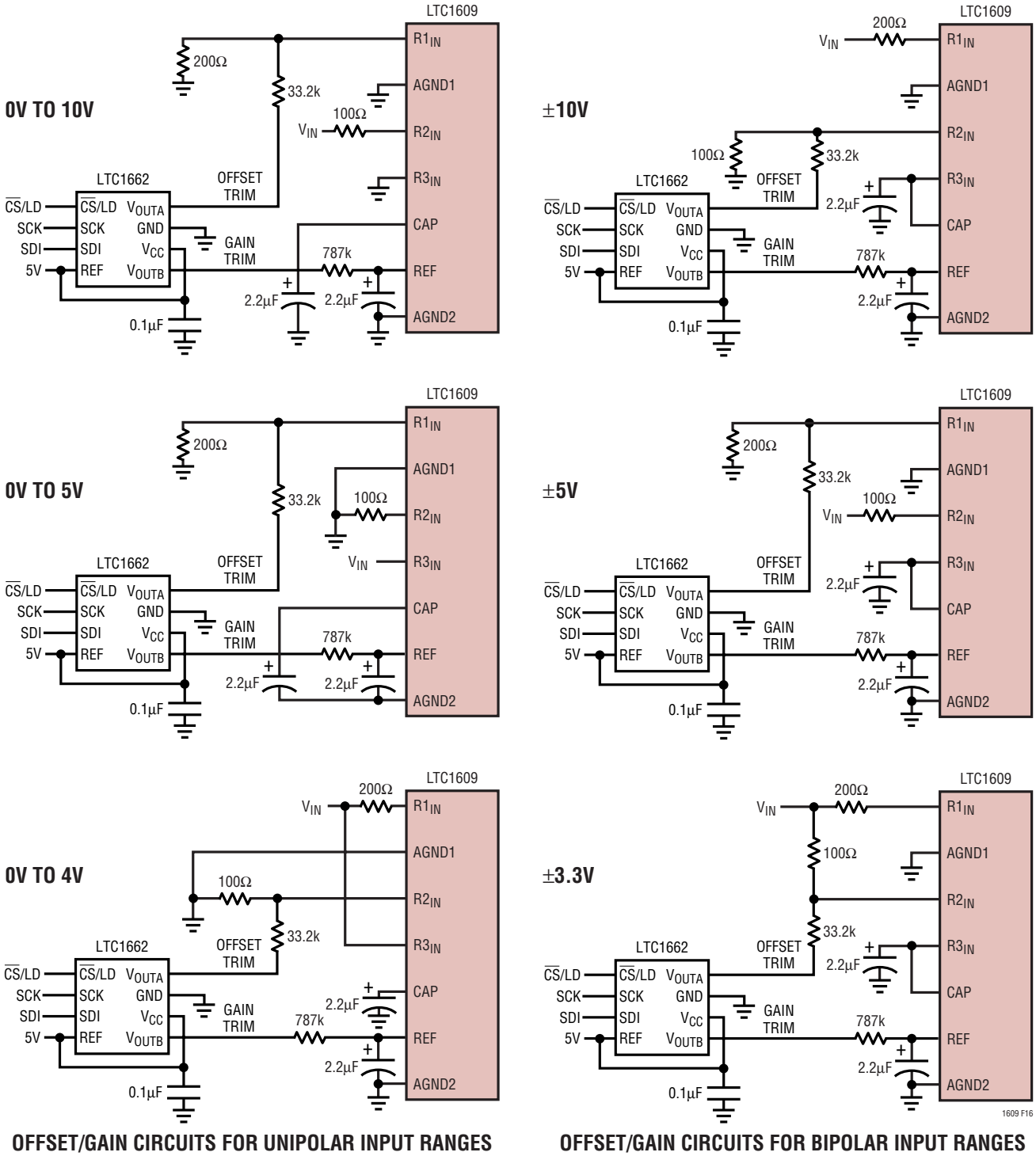


Figure 15d. LTC1609 "Postage Stamp" Evaluation Board Bottom Metal Layer (2× Actual Size)

APPLICATIONS INFORMATION



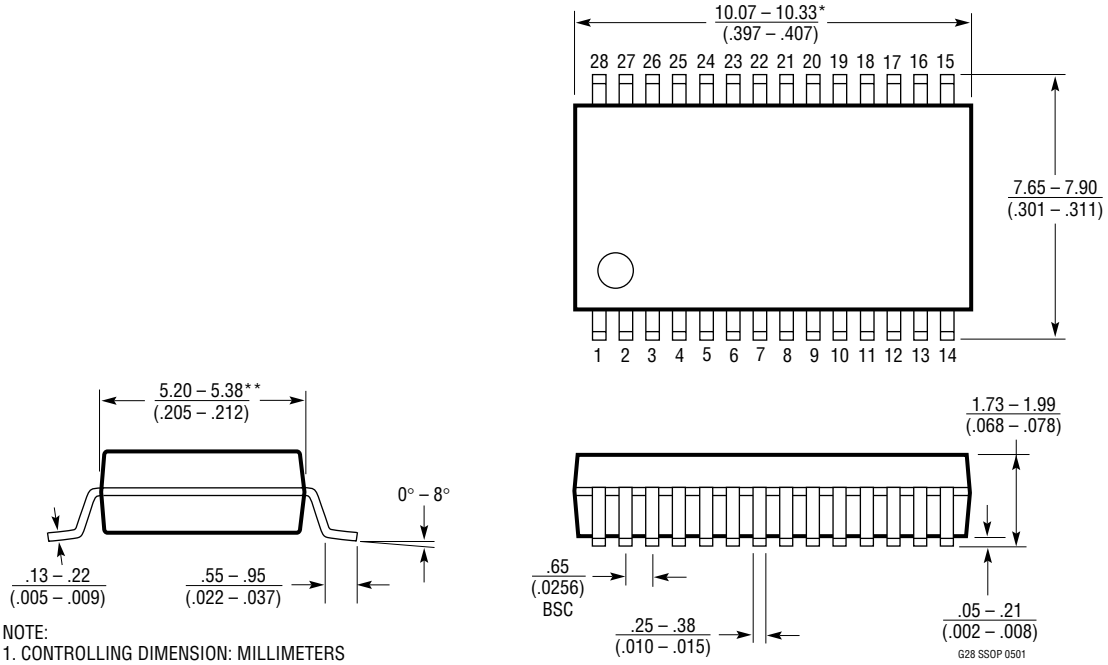
OFFSET/GAIN CIRCUITS FOR UNIPOLAR INPUT RANGES

OFFSET/GAIN CIRCUITS FOR BIPOLAR INPUT RANGES

Figure 16. Digitally-Controlled Offset and Full-Scale Adjust Circuits Using the LTC1662 Dual 10-Bit V_{OUT} DAC (Adjust Offset First at 0V, Then Adjust Gain)

PACKAGE DESCRIPTION

G Package
28-Lead Plastic SSOP (5.3mm)
(Reference LTC DWG # 05-08-1640)



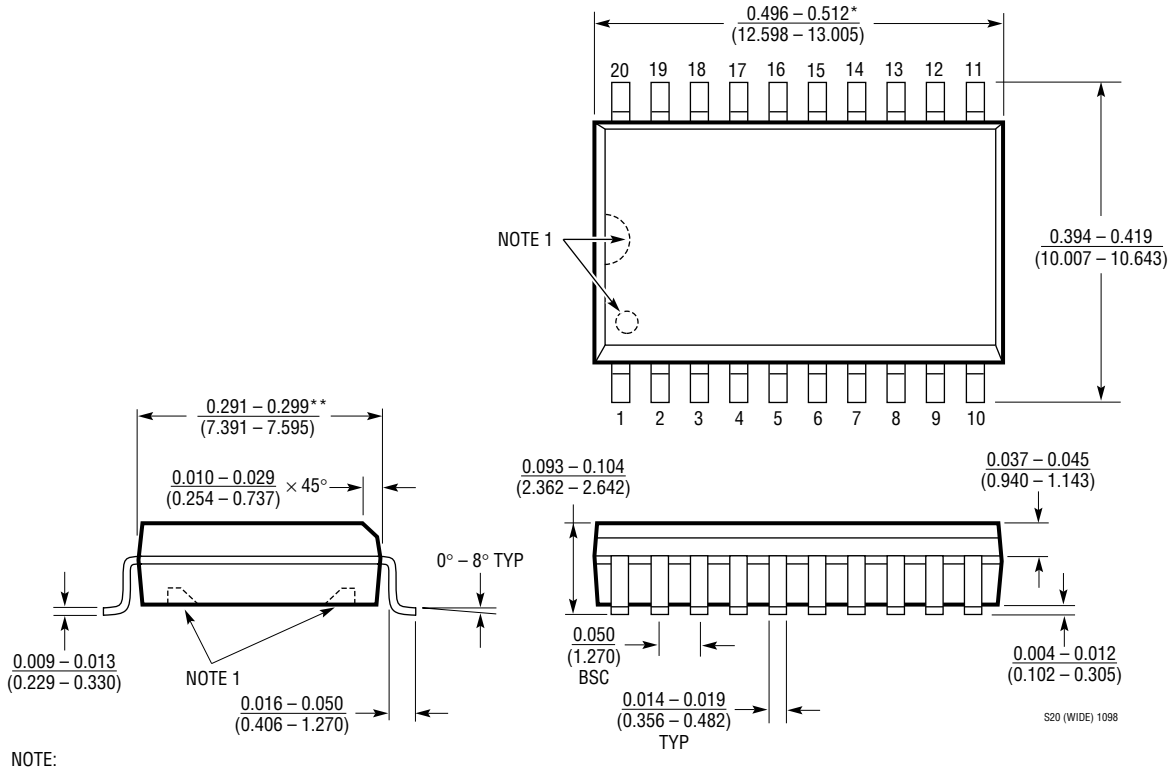
NOTE:
1. CONTROLLING DIMENSION: MILLIMETERS
2. DIMENSIONS ARE IN $\frac{\text{MILLIMETERS}}{\text{(INCHES)}}$
3. DRAWING NOT TO SCALE

*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .152mm (.006") PER SIDE

**DIMENSIONS DO NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED .254mm (.010") PER SIDE

PACKAGE DESCRIPTION

SW Package
20-Lead Plastic Small Outline (Wide .300 Inch)
(Reference LTC DWG # 05-08-1620)



NOTE:
1. PIN 1 IDENT, NOTCH ON TOP AND CAVITIES ON THE BOTTOM OF PACKAGES ARE THE MANUFACTURING OPTIONS. THE PART MAY BE SUPPLIED WITH OR WITHOUT ANY OF THE OPTIONS

*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1417	Low Power 400ksps 14-Bit ADC	20mW, Single 5V or ±5V, Serial I/O
LTC1418	Low Power 200ksps 14-Bit ADC	15mW, Single 5V or ±5V, Serial/Parallel I/O
LTC1595/LTC1596	16-Bit Mulitplying DACs	Low Glitch, Serial I/O, SO-8/S16 Packages
LTC1597	16-Bit Mulitplying DAC	4-Quadrant Resistors On-Chip, Low Glitch, Parallel I/O
LTC1604	16-Bit 333ksps Sampling ADC	±2.5V Input, 90dB SINAD, 100dB THD, Parallel I/O
LTC1605	Low Power 100ksps 16-Bit ADC	Single 5V, ±10V Input
LTC1605-1	Low Power 100ksps 16-Bit ADC	Single 5V, 0V to 4V Input
LTC1605-2	Low Power 100ksps 16-Bit ADC	Single 5V, ±4V Input
LTC1606	Low Power 250ksps 16-Bit ADC	Single 5V, ±10V Input, Parallel I/O
LTC1608	16-Bit 500ksps Sampling ADC	±2.5V Input, Pin Compatible with LTC1604
LTC1650	16-Bit ±5V Voltage Output DAC	Low Glitch, 4µs Settling Time, Serial I/O
LTC1655/LTC1655L	16-Bit Single 5V/3V Voltage Output DACs	SO-8 Package, Micropower, Serial I/O

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