Ordering number : ENA1610A

SANYO Semiconductors
DATA SHEET

An ON Semiconductor Company

Bi-CMOS IC

LV71081E — For Video/Audio Signal Input/ Output Interface of DVD Recorder

Overview

The LV71081E is for video/audio signal input/output interface of DVD recorder.

Functions

- Video audio canal SW
- S signal 3 input switch
- 6dB amplifier
- 6MHz/12MHz/27MHz-LPF / 6MHz/12MHz/27MHz low pass filter
- 6ch video driver (AV1, AV2, Line output, R•G•B output)
- Video signal detection
- Composite sync output

Specifications

Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage 1	V_{CC} max		6.0	V
Maximum supply voltage 2	V_{CC} max		13.0	V
Allowable power dissipation	Pd max	Ta ≤ 75°C Mounted on a specified board *	1200	mW
Operating temperature	Topr		-20 to +75	°C
Storage temperature	Tstg		-40 to +150	°C

* Mounted on a specified board : 114.3mm × 76.1mm × 1.6mm, glass epoxy

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Recommended Operating Conditions at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Recommended supply voltage 1	V_{CC}		5.0	V
Recommended supply voltage 2	V_{CC}		12.0	V
Operating supply voltage range 1	V_{CC} opg		4.5 to 5.3	V
Operating supply voltage range 2	V_{CC} opg		11.1 to 12.5	V

Electrical Characteristics at Ta = 25°C, V_{CC} = 2.8V

Parameter	Symbol	Input signal			Out	Test condition	Ratings			Unit
		Point	Signal	Freq	Point		min	typ	max	
Current dissipation 1 (5V)	$I_{CC}1$					Pin6, 8, 25, 40 flow in current when non-signal	97.7	115.0	132.2	mA
Current dissipation 2 (ALL5V)	$I_{CC}2$					Pin42, 84, 94 flow in current when non-signal	20.0	23.0	26.0	mA
Current dissipation 3 (11.6V)	$I_{CC}3$					Pin46 flow in current when non-signal	18.7	22.0	25.3	mA
Video CANAL SW part										
Output voltage 1	VDCC				26 28	AV1, AV2-OUT (Sync tip)	0.3	0.5	0.7	V
Voltage gain	VGC			100k	26 28	V_{IN} = 1Vp-p, AV1, AV2-OUT	5.5	6.0	6.5	dB
Frequency characteristics	VFC				26 28	V_{IN} = 1Vp-p, f = 10MHz/100kHz	-1.0	0.0	+1.0	dB
Differential gain	DGC				26 28	V_{IN} = Video : 1Vp-p	-1	0	+1	%
Differential phase	DPC				26 28	V_{IN} = Video : 1Vp-p	-1.5	0	+1.5	°C
Cross-talk	CTC			4.43M	26 28	Selected input = GND Non-selected input = 1Vp-p, f = 4.43MHz		-60	-50	dB
Picture S/N	VSNC				26 28	V_{IN} = Video (50%White)		-70	-65	dB
Maximum output level	V_OMAXC				26 28	Output level ar which the linearity of AVI-OUT (pin 26) and AV2-OUT (pin 28) exceeds 1%. V_{IN} = Linearity (lamp) signal Output level at linearity 1%	2.8	3.0		Vp-p
Video INPUT SW part										
Output voltage 1	VDCI1				83	Composite (Sync-Tip)	0.8	1.0	1.2	V
Output voltage 2	VDCI2				83	Y (Sync-Tip)	0.8	1.0	1.2	V
Output voltage 3	VDCI3				81	Chroma (Center)	1.8	2.1	2.4	V
Voltage gain 1	VGI1			100k	81 83	V_{IN} = 1Vp-p, load = 10kΩ	-0.5	0.0	+0.5	dB
Voltage gain 2	VGI2			100k	85	V_{IN} = 1Vp-p, load = 10kΩ (SLICER output only)	5.5	6.0	6.5	dB
Frequency characteristics	VFI				81 83	V_{IN} = 1Vp-p, f = 10MHz/100kHz	-1.0	0.0	+1.0	dB
Differential Gain	DGSW				83	V_{IN} = Video :1Vp-p	-1	0	+1	%
Differential Phase	DPSW				83	V_{IN} = Video :1Vp-p	-1.5	0	+1.5	°C
Cross-talk	CTC			4.43M	81 83	Selected input = GND Non-selected input = 1Vp-p, f = 4.43MHz		-60	-50	dB
Picture S/N	VSNC				83	V_{IN} = Video (50%White)		-66	-60	dB
Maximum output level	V_OMAXSW				83	Output level when the linearity of pin 83 exceeds 1%. V_{IN} = Linearity (lamp) signal Output level at linearity 1%	1.8	2.0		Vp-p

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Parameter	Symbol	Input signal			Out	Test condition	Ratings			Unit
		Point	Signal	Freq	Point		min	typ	max	
Video Driver part										
Output voltage 1	VDCD1	95 97 99			9 12 17	RGB (Pedestal)	0.3	0.5	0.7	V
Output voltage 2	VDCD2	93			14 23	Y (Sync tip)	0.5	0.7	0.9	V
Voltage gain 1	VGD			100k		V_{IN} = 1Vp-p, Line output : 2 drives, Scart output: DC directly-coupled single drive Note 1)	5.5	6.0	6.5	dB
Frequency characteristics 1	VFD1					V_{IN} = 1Vp-p, f = 6MHz/100kHz when 6MHzLPF is selected	-1.5	0.0	+1.5	dB
Frequency characteristics 2	VFD2					f = 27MHz/100kHz when 6MHzLPF is selected		-35	-25	dB
Frequency characteristics 3	VFD3					f = 12MHz/100kHz when 12MHzLPF is selected	-1.5	0.0	+1.5	dB
Frequency characteristics 4	VFD4					f = 54MHz/100kHz when 12MHzLPF is selected		-40	-30	dB
Group delay	VGDD1					f = 6MHz/100kHz when 6MHzLPF is selected		20	35	ns
Mute attenuation	VMUD					V_{IN} = 1Vp-p, f=4.43MHz		-60	-50	dB
Differential Gain	DG1	91 93			23	V_{IN} = Video : 1Vp-p	-1	0	+1	%
Differential Phase	DP1	91 93			23	V_{IN} = Video : 1Vp-p	-1.5	0	+1.5	°C
Cross-talk	CTD			4.43M		V_{IN} = 1Vp-p, f = 4.43MHz, Driver output terminated with 75Ω		-60	-50	dB
Picture S/N	VSND					V_{IN} = Video (50%White)		-70	-65	dB
Maximum output level 1	V_OMAXD1				9 12 17	Output level when the linearity of pins 9, 12, and 17 exceeds 1%. V_{IN} = Linearity (lamp) signal Output level at linearity 1%	2.8	3.0		Vp-p
Maximum output level 2	V_OMAXD2				14 19 23	Output level when the linearity of pins 14, 19, and 23 exceeds 1% V_{IN} = Linearity (lamp) signal Output level at linearity 1%	2.6	2.8		Vp-p
Maximum output level 3	V_OMAXD3				7 11 22	Output level at which the linearity of pins 7, 11, and 22 exceeds 1% V_{IN} = sin 10kHz Output level at linearity 1%	2.0	2.5		Vp-p
Sync-SEP part										
C.SYNC output High voltage	VCSH				86		4.3	4.7	5.0	V
C.SYNC output Low voltage	VCSL				86		0	0.3	0.6	V
C.SYNC output delay time	TDCS				86	Note 2)	1.0	1.7	2.4	μs
C.SYNC output pulse width	TWCS				86	Note 2)	3.2	4.2	5.2	μs
V.SYNC output High voltage	VVSH				82		4.3	4.7	5.0	V
V.SYNC output Low voltage	VVSL				82		0	0.3	0.6	V

Note 1) The Line output can drive two systems through capacitive coupling while the Scart output drives only one system through DC direct coupling.

Note 2) When pin 10 is open

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Parameter	Symbol	Input signal			Out	Test condition	Ratings			Unit
		Point	Signal	Freq	Point		min	typ	max	
V.SYNC output delay time	TDVS				82	Note 2)	7	15	25	μs
V.SYNC output pulse width	TWVS				82	V_{IN} = PAL Video : 1Vp-p Note 2)	125	155	185	μs
V.DET output High voltage	VDETH				90		4.3	4.7	5.0	V
V.DET output Low voltage	VDETL				90		0	0.3	0.6	V
Audio canal switches part										
Maximum output level	V_OMAXC				71 to 74	AV1, AV2-OUT (L, R) BW = 400 to 30kHz Output level at f = 1kHz, THD = 1%	2.2	2.5		Vrms
Channel balance	CVSW				71 to 74	V_{IN} = 2Vrms, f = 1kHz Lch Gain-Rch Gain	-1.5	0.0	+1.5	dB
Total harmonic distortion	THDAC				71 to 74	V_{IN} = 2Vrms, f = 1kHz, BW = 400 to 30kHz		0.003	0.01	%
Output noise voltage	VNAC				71 to 74	Rg = 0Ω, BW = JIS-A		-100	-80	dBV
Mute attenuation	VMUAC				71 to 74	V_{IN} = 2Vrms, f = 1kHz, BW = JIS-A 20log (V_{OUT}/V_{IN})		-90	-75	dB
Input impedance	Z_{IN}						80	100	120	kΩ
Cross talk between channel and selctors	CTSW				71 to 74	V_{IN} = 2Vrms, f = 1kHz Rg = 0Ω, BW = JIS-A		-110	-80	dB
Tuner gain	G_{TU}				71 to 74	V_{IN} = 0.5Vrms	10.0	12.0	14.0	dB
Output off set voltage	V_{OFSET}				71 to 74	Off set voltage at the time of changeover SW.	-20	0	+20	mV
Audio ADC block										
Voltage gain 1	VGA1				78 79	V_{IN} = 1Vrms, f = 1kHz, EVR = 0dB Serial control select 6dB.	4.5	6.0	7.5	dB
Voltage gain 2	VGA2				78 79	V_{IN} = 1Vrms, f = 1kHz, EVR = 0dB Serial control select 5.5dB.	4.0	5.5	7.0	dB
Voltage gain 3	VGA3				78 79	V_{IN} = 1Vrms, f = 1kHz, EVR = 0dB Serial control select 5dB.	3.5	5.0	6.5	dB
Voltage gain 4	VGA4				78 79	V_{IN} = 1Vrms, f = 1kHz, EVR = 0dB Serial control select 0dB.	-1.5	0.0	+1.5	dB
Channel balance	CVVR				78 79	V_{IN} = 2Vrms, f = 1kHz, AMP = 5.5dB, AEVR = -12dB Lch Gain-Rch Gain	-1.5	0.0	1.5	dB
Maximum output level	V_OMAXI				78 79	ADC-OUT (L, R), AMP = 0dB, EVR = 0dB BW = 400 to 30kHz Output level at f = 1kHz, THD = 1%	2.2	2.5		Vrms
Total harmonic distortion	THDAI				78 79	V_{IN} = 2Vrms, f = 1kHz, AMP = 5.5dB, EVR = -12dB BW = 400 to 30kHz		0.002	0.005	%

Note 2) When pin 10 is open

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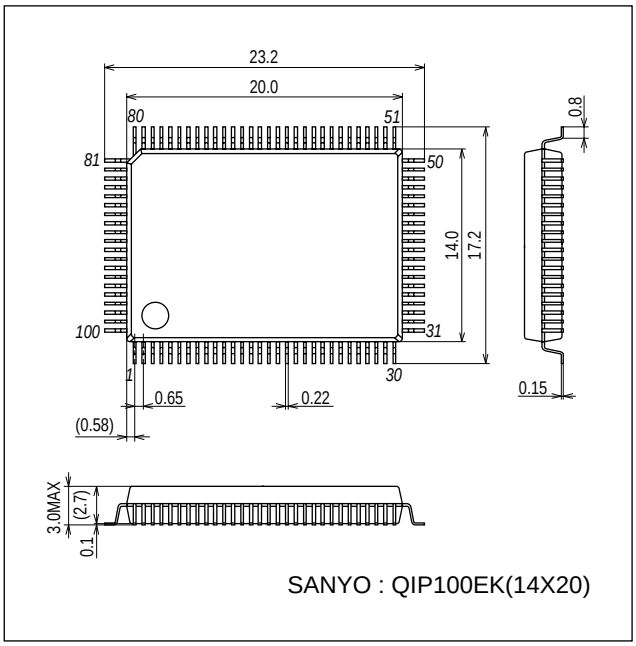
Parameter	Symbol	Input signal			Out	Test condition	Ratings			Unit
		Point	Signal	Freq	Point		min	typ	max	
Output noise voltage	VNAI				78 79	AMP = 5.5dB, EVR = -12dB Rg = 0Ω, BW = JIS-A		-100	-80	dBV
Cross talk between channel and selctors	CTVR				78 79	V_{IN} = 2Vrms, f = 1kHz, AMP = 5.5dB, EVR = -12dB Rg = 0Ω, BW = JIS-A		-110	-80	dB
Max attenuation amount	VMUAI				78 79	V_{IN} = 2Vrms, f = 1kHz, AMP = 5.5dB, BW = JIS-A EVR = mute/EVR = 0dB		-106	-85	dB
Residual noise voltage	VNAR				78 79	AMP = 5.5dB, EVR = mute Rg = 0Ω, BW = JIS-A		-106	-80	dBV
External control part										
I^2C-BUS High level input voltage	V_{IH}	88 89					2.5		V_{CC}	V
I^2C-BUS Low level input voltage	V_{IL}	88 89					GND		0.8	V
FSS output H voltage	VHFSS				27	Serial control select FSS OUT H, load = 10kΩ external output resistor 470 recommended	10.6	11.1	11.6	V
FSS output M voltage	VMFSS				27	Serial control select FSS OUT M, load = 10kΩ external output resistor 470 recommended	5.5	6.3	7.0	V
FSS output L voltage	VLFSS				27	Serial control select FSS OUT, load = 10kΩ	0.0	0.1	0.5	V
FSS risinge time	TFSSLH				27				1.0	ms
FB output H voltage	VHFB				34	Serial control select FB OUT H. load = 150Ω	3.0	4.0	5.0	V
FB output L voltage	VLFB				34	Serial control select FB OUT L. load = 150Ω	0.0	0.2	0.4	V
FB external control L range	VLFBIN	32				Pin 32 input voltage range at which the pin 34 output becomes L	0.0		0.5	V
FB external control H range	VHFBIN	32				Pin 32 input voltage range when the pin 34 output becomes H	1.0		3.0	V
External control output H voltage	V_{EXTH}				10 36 38	2kΩ load for data 1	4.0	4.5	5.0	V
External control output L voltage	V_{EXTL}				10 36 38	2kΩ load for data 0	0.0	0.3	1.0	V
Internal reference regulator										
REG2.5V	VREG25				2 100	Pins 2 and 100 voltage	2.3	2.5	2.7	V
REG9.0V	VREG90				57 65	Pins 57 and 65 voltage	8.7	9.0	9.3	V
VRE4.5	VREG45				49	Pin 49 voltage	4.3	4.5	4.7	V

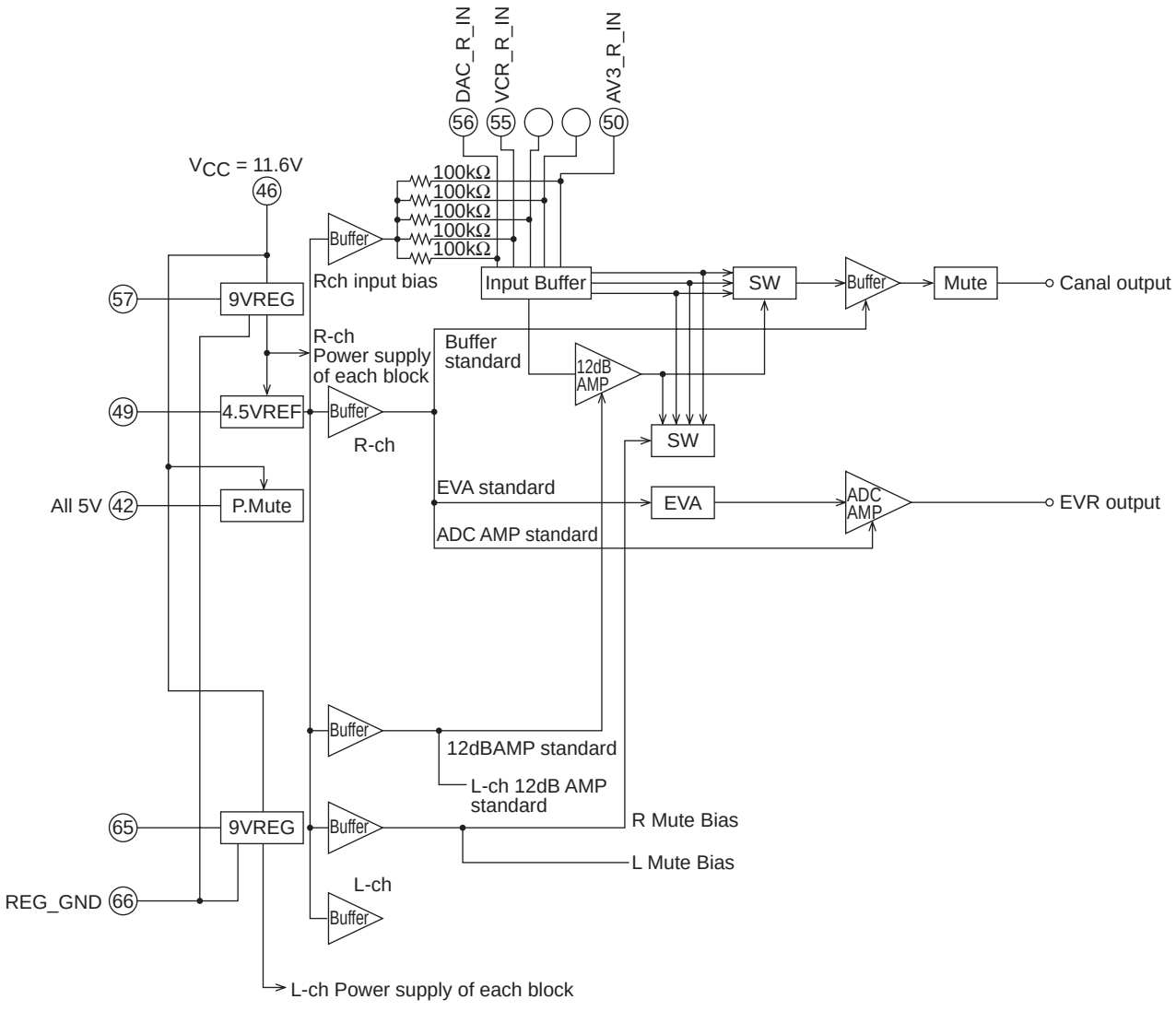
Package Dimensions

unit : mm (typ)

3349

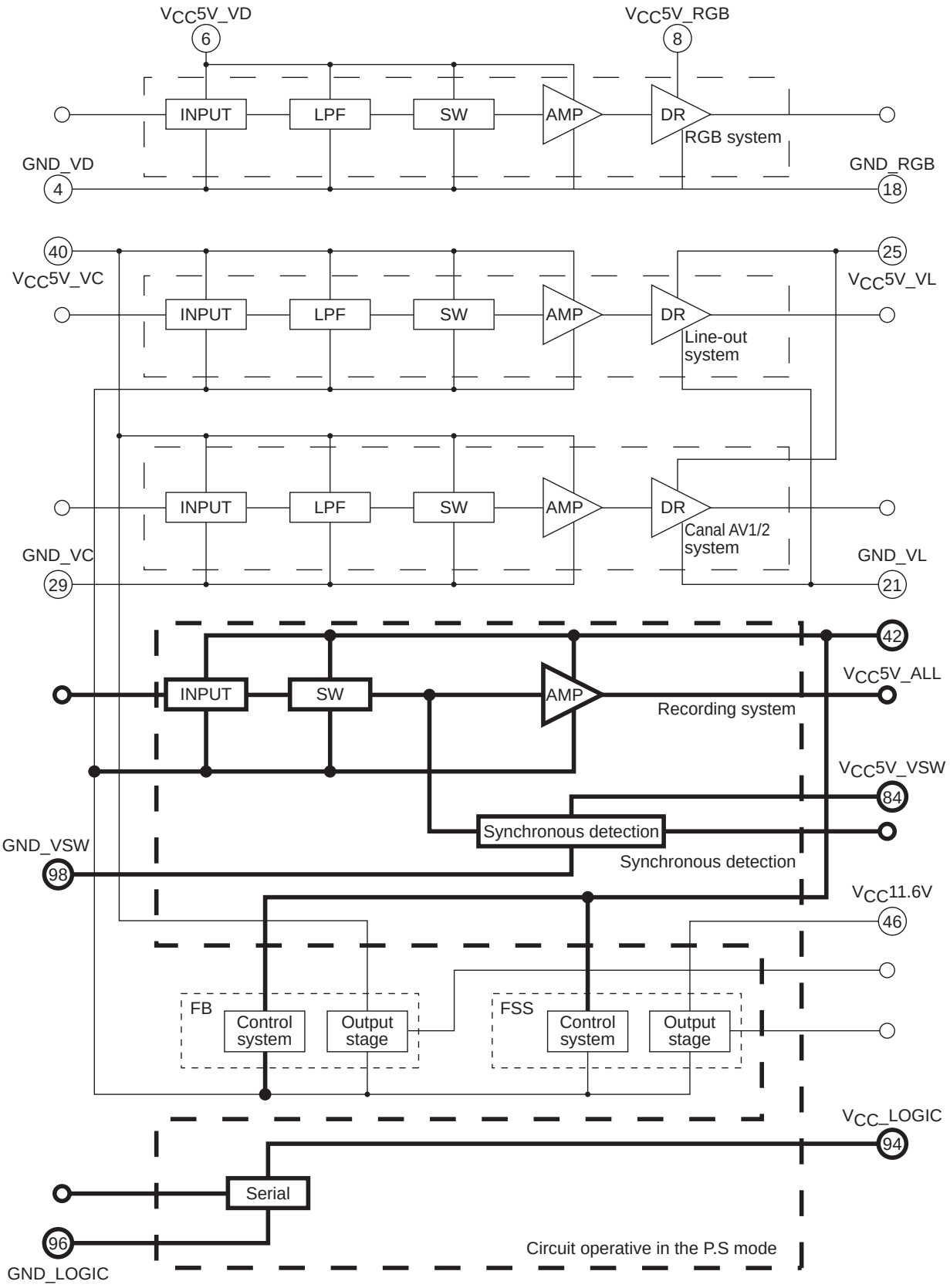


Graphical View of Audio Block Power Supply

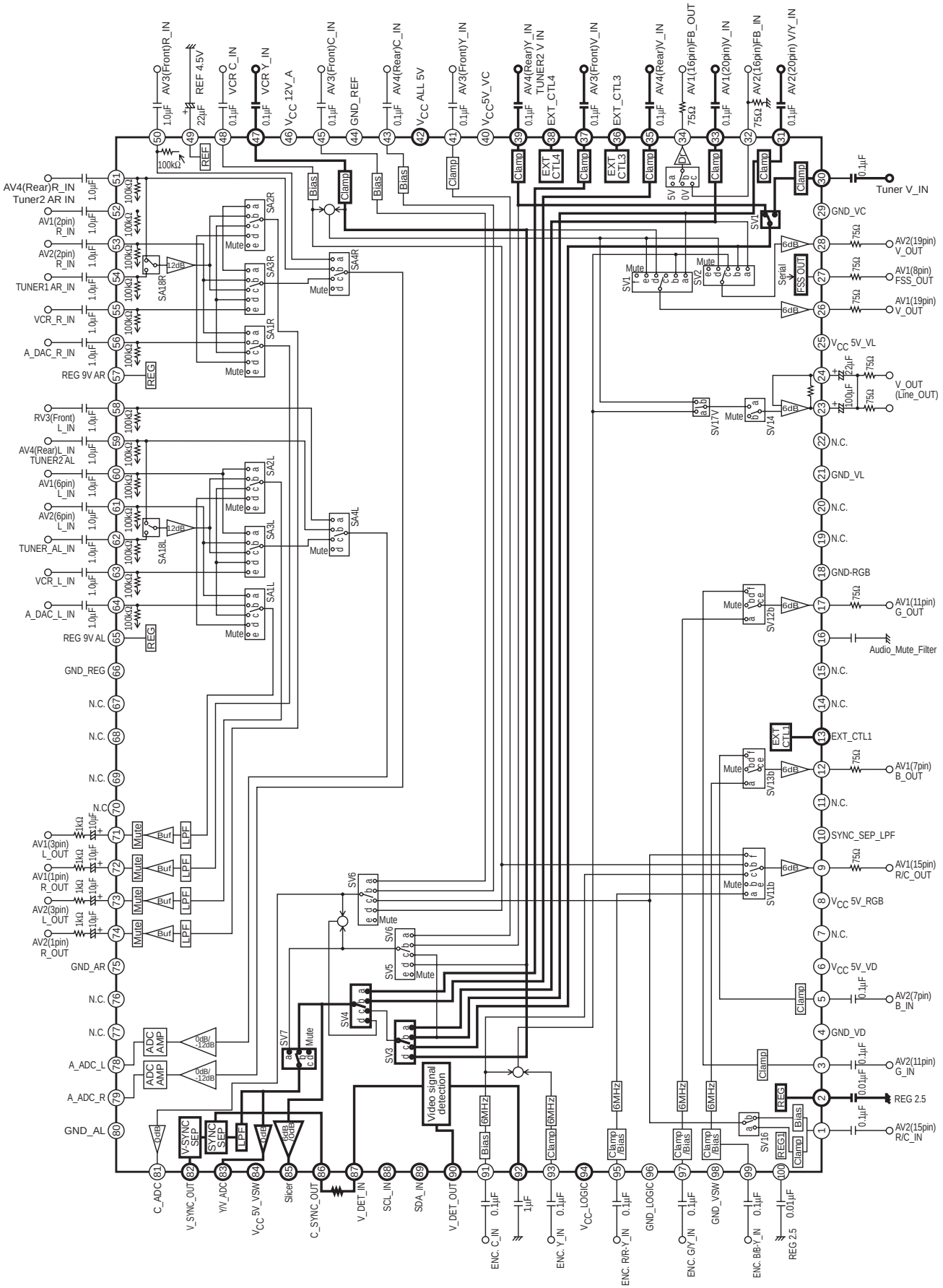


Graphical View of The Video Block Power Supply

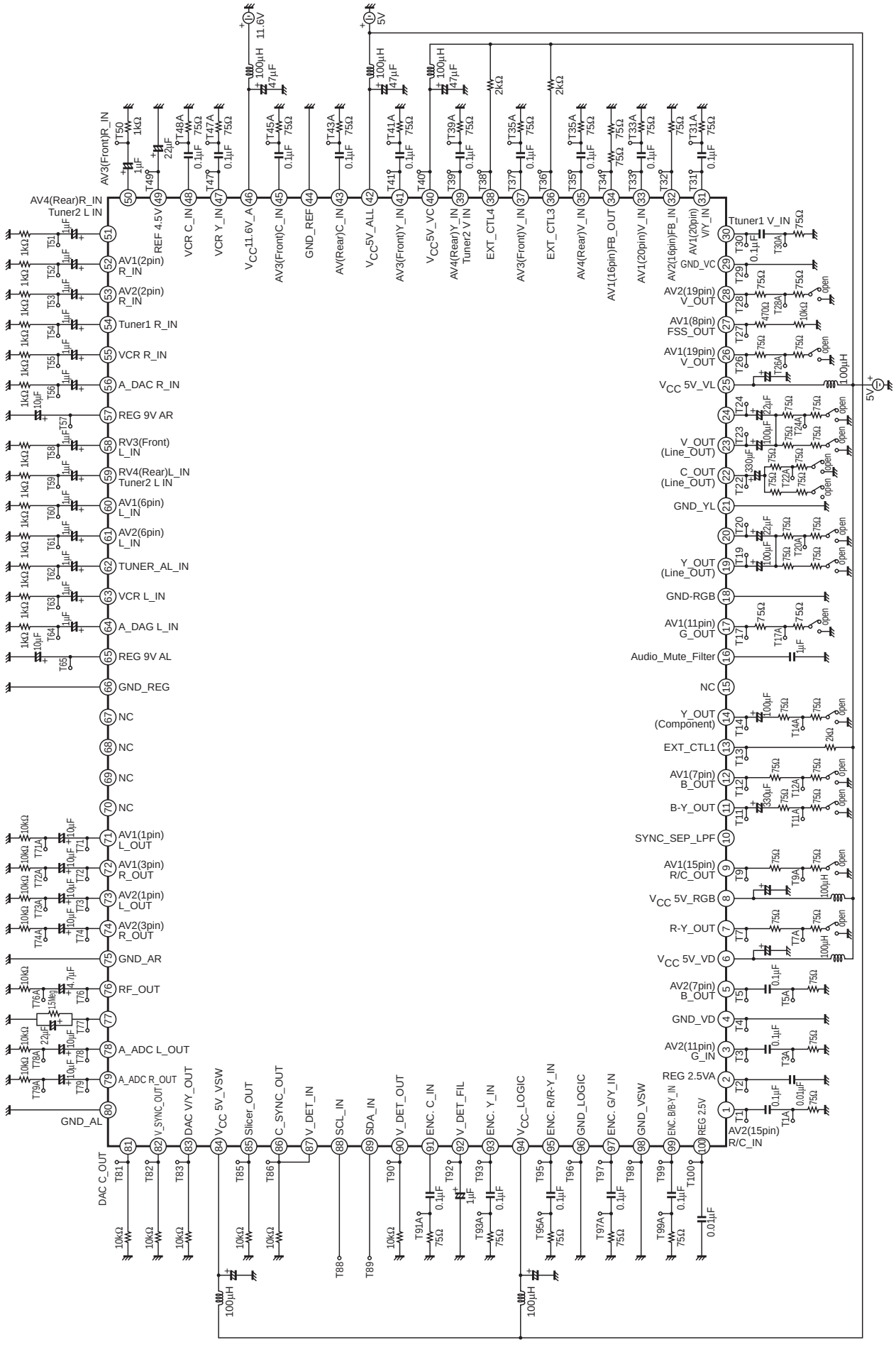
* The thick line indicates the circuit operative in the power save mode.
  In the power save mode, 5V is applied to Pin 42 (V_{CC}5_All), pin 84 (V_{CC}5V_VSW), and pin 94 (V_{CC}_LOGIC) only.



Block Diagram



Test Circuit

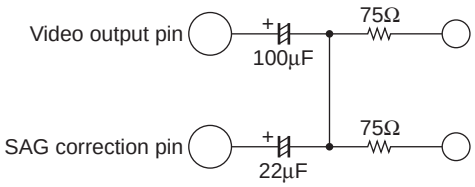


Cautions for Use

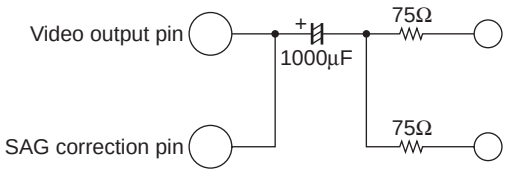
1. Drive capacity of video driver
   Line and component outputs can drive two system through capacitive coupling.
   Scart output can drive one system only through DC coupling.

2. Application not using the SAG correction function in the video driver with SAG correction
   When the SAG correction function is not to be used in the video driver with SAG correction, short-circuit output and correction pins for output through capacitive coupling.

Application using SAG correction function



Application without using SAG correction function



3. Treatment of the pin when Audio RF_MOD output is not used
   When RF MOD OUT (Pin76) is not used, it is recommended to pull up the ALC filter pin (pin77) to V_{CC} (11.6V).

4. Audio Mute
   This IC incorporates a mute transistor to reduce the POP noise of audio output when power is turned ON/OFF.
   Mute control can be made by serial control.

5. Resistor to limit the Audio input
   When the large signal is input in the input pin with power OFF, cross-talk between input and output occurs through the protective diode and parasitic elements. Because of the structure of LSI, such cross-talk is difficult to avoid. If cross-talk at a time of power OFF presents a problem, the cross-talk amount can be reduced by inserting the limiting resistor in the input. In this case, the input signal level changes depending on the resistance value. Determine the constant while taking both the cross-talk amount and input level into account.

6. Pin treatment when external control is not to be used
   When external control pins (Pins 13, 36, and 38) are not used, pull-down to GND is recommended.

7. Pin treatment of N.C pin
   It is recommended to connect N.C. pins (Pins 67, 68, 69, and 70) directly to the GND.

8. Audio 9V_REG pin external capacitance
   Use the Audio 9V_REG pins (pins 57 and 66) external capacitance of 10µF or more and with the equivalent series resistance component of 7Ω or less.

9. Power application and disconnection sequences
   The recommended power application sequence to this IC is V_{CC}_ALL5V (Pin42) → V_{CC}5V (Pins 6, 8, 25, 40, 84 and 94), V_{CC}11.6V (Pin46).
   (No particular order is established between V_{CC}5V and V_{CC}11.6V.) It is recommended to reverse the above sequence when power supply is turned OFF.

Serial Control Table

* indicates initial.

ADDRESS		8	7	6	5	4	3	2	1				Remarks	
Group 1 00000001 VIDEO CANAL-SW VIDEO	SV1									SV1				
							0	0	0	V (AV2)				*
							0	0	1	Y+C MIX (ENC)			PB	
							0	1	0	Y (ENC)			PB (SCART Y/C)	
							0	1	1	Y (VCR)			PB (VCR SCART Y/C)	
							1	0	0	CV (VCR)			PB (VCR)	
							1	0	1	MUTE				
							1	1	*	PROHIBIT				
	SV2									SV2				
				0	0	0				V (AV1)				*
				0	0	1				V (TU)				
				0	1	0				Y+C MIX (ENC)			PB	
				0	1	1				CV (VCR)			PB (VCR)	
				1	0	0				MUTE				
				1	0	1	and after			PROHIBIT				
	SV3									SV3				
		0	0							V (AV1)				
		0	1							V (AV2)				*
		1	0							V (TU)				
		1	1							Y (VCR)			PB	

ADDRESS		8	7	6	5	4	3	2	1				Remarks	
Group 2 00000010 VIDEO INPUT-SW	SV4									SV4				
								0	0	V (AV3)				
								0	1	V (AV4)				
								1	0	SV3-OUT				*
								1	1	SV5/6 MIX				
	SV5/6									SV5	SV6			
					0	0	0			Y (AV3)	C (AV3)		FRONT	
					0	0	1			Y (AV4)	C (AV4)		REAR	
					0	1	0			Y (AV2)	C (AV2)		SCART-YC	
					0	1	1			Y (VCR)	C (VCR)			
					1	0	0			MUTE	MUTE			*
					1	0	1	and after		PROHIBIT	PROHIBIT			
	SV7									SV7				
			0	0						Y				
			0	1						CV				
			1	0						MUTE				*
			1	1						MUTE				
	SV16 Note 1)									SV16				
		0								THROUGH				*
		1								CLAMP input fixed				

Note 1) G2D8/G3D8 = “11” is prohibited. Follow the AV2 (16) FB_IN (Pin32) control in case of THROUGH.

AV2_16pin SV16

H a : Clamp input (RGB)

L b : Bias input (COMPONENT)

ADDRESS		8	7	6	5	4	3	2	1				Remarks	
Group 3 00000011 VIDEO OTHER-1	12/27MHz LPF SW													
									0				x = 12MHz	*
									1				x = 27MHz	
	RGB output									SV11b	SV12b	SV13b		
								0		According to G3D3/D4/D5 control				
								1		AV2_R	AV2_G	AV2_B	f : AV2_RGB (EXTERNAL)	*
	N/A													
					0	0	0			N/A	N/A	N/A		*
					0	0	1			N/A	N/A	N/A		
					0	1	0			N/A	N/A	N/A		
					0	1	1			N/A	N/A	N/A		
					1	0	0			N/A	N/A	N/A		
					1	0	1			N/A	N/A	N/A		
					1	1	0	and after		PROHIBIT	PROHIBIT	PROHIBIT		
	SV11b SV12b SV13b * effective at G3D2 = “0”									SV11b	SV12b	SV13b		
					0	0	0			ENC_R	ENC_G	ENC_B	a : ENC_RGB (6MLPF)	*
					0	0	1			MUTE	MUTE	MUTE	b : mute	
					0	1	0			ENC_C	MUTE	MUTE	c : ENC_C	
					0	1	1			VCR_C	MUTE	MUTE	d : VCR_C	
					1	0	0			MUTE	MUTE	MUTE	e : mute	
					1	0	1			AV2_R	AV2_G	AV2_B	f : AV2_RGB (EXTERNAL)	
					1	1	0	and after		PROHIBIT	PROHIBIT	PROHIBIT		
	SV14									SV14				
				0						CV (PB)			PB	
				1						MUTE				*
	N/A													
			0							N/A	N/A			
			1							MUTE	MUTE			*
	SV16 Note 1)									SV16				
		0								THROUGH				
		1								BIAS input fixed				*

Note 1) G2D8/G3D8 = “11” is prohibited. Follow the AV2 (16) FB_IN (Pin32) control in case of THROUGH.

AV2_16pin SV16

H a : Clamp input (RGB)

L b : Bias input (COMPONENT)

ADDRESS		8	7	6	5	4	3	2	1				Remarks	
Group 4 00000100 VIDEO & AUDIO OTHER-1	SV17 DVD/VCR Note 2)									SV17 (V/C/Y)	SA17 (L/R)			
									0	Y+C MIX (ENC)	AUDIO (DAC)		PB (DVD)	*
									1	Y+C MIX (VCR)	AUDIO (VCR)		PB (VCR)	
	SV18 TUNER1/2 Note 2)									SV18	SA18 (L/R)			
								0		Tuner1	Tuner1			*
								1		Tuner2	Tuner2			
	FB AV1 (16)									SWF				
						0	0			0				
						0	1			5V				
						1	0			THROUGH				*
						1	1			THROUGH				
	FSS AV1 (8) Note 3)									FSS-OUT				
				0	0					LOW (0.5V)				*
				0	1					MID (6.0V)				
				1	0					HIGH (11.0V)				
				1	1					HIGH (11.0V)				
	SLICE AMP									SLICE AMP gain				
			0							0dB				*
			1							6dB				
	A-MUTE Note 4)									All MUTE (Audio)				
		0								THROUGH				
		1								MUTE			Pins 71 to 74 output MUTE	*

Note 2) Operates in VIDEO/AUDIO interlock.

Note 3) Same polarity as the AV2 (16) FB_IN (Pin32) control in case of THROUGH.

Note 4) AUDIO MUTE control

RF_MOD output : Serial control MUTE, Power-ON_MUTE

CANAL output : Serial control MUTE, Power-ON_MUTE

ADDRESS		8	7	6	5	4	3	2	1				Remarks	
Group 5 00000101 AUDIO CANAL-SW	SA1L/R									SA1L	SA1R			
							0	0	0	L (AV2)	R (AV2)			*
							0	0	1	L (DAC)	R (DAC)		PB (DAC)	
							0	1	0	L (DAC)	R (DAC)		PB (DAC)	
							0	1	1	L (VCR)	R (VCR)		PB (VCR)	
							1	0	0	MUTE	MUTE			
				and after			1	0	1	PROHIBIT	PROHIBIT			
	SA2L/R									SA2L	SA2R			
				0	0	0				L (AV1)	R (AV1)			*
				0	0	1				L (TU)	R (TU)			
				0	1	0				L (DAC)	R (DAC)		PB	
				0	1	1				L (VCR)	R (VCR)		PB	
				1	0	0				MUTE	MUTE			
				1	0	1	and after			PROHIBIT	PROHIBIT			
	SA4L/R									SA4L	SA4R			
		0	0							L (AV3)	R (AV3)			
		0	1							L (AV4)	R (AV4)			
		1	0							SL3 out	SR3 out			*
		1	1							MUTE	MUTE			

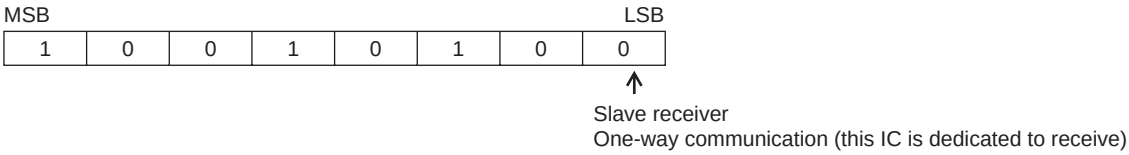
ADDRESS		8	7	6	5	4	3	2	1				Remarks	
Group 6 00000110 AUDIO INPUT-SW MUTE	SA3L/R									SA3L	SA3R			
							0	0	0	L (AV1)	R (AV1)			
							0	0	1	L (AV2)	R (AV2)			*
							0	1	0	L (TU)	R (TU)			
							0	1	1	L (DAC)	R (DAC)		PB	
							1	0	0	L (VCR)	R (VCR)			
				and after			1	0	1	PROHIBIT	PROHIBIT			
	N/A													
						0				N/A				
						1				N/A				*
	N/A													
				0	0					N/A				
				0	1					N/A				*
				1	0					N/A				
				1	1					PROHIBIT				
	ADC-AMP									ADC-AMP-gain				
		0	0							6.0dB				
		0	1							5.5dB				*
		1	0							5.0dB				
		1	1							PROHIBIT				

ADDRESS		8	7	6	5	4	3	2	1				Remarks	
Group 7 00000111	AUDIO EVR-L									Audio EVR (L)				
				0	0	0	0	0	0	0dB				
				0	0	1	1	0	0	-12dB				
				1	1	1	1	1	1	Mute			Pin 78 output MUTE	*
						Other than above				PROHIBIT				
	General purpose 1									EXT_CTL1 (Pin13)				
			0							L			General purpose OUT1	
			1							H				*
	Changeover of VIDEO input BIAS/CLAMP									R/R-Y_IN (Pin95)	G/Y_IN (Pin97)	B/B-Y_IN (Pin99)	Input changeover	
		0								BIAS input	CLAMP input	BIAS input	Component	
		1								CLAMP input	CLAMP input	CLAMP input	RGB	*

ADDRESS		8	7	6	5	4	3	2	1				Remarks	
Group 8 00001000	AUDIO EVR-R									Audio EVR (R)				
				0	0	0	0	0	0	0dB				
				0	0	1	1	0	0	-12dB				
				1	1	1	1	1	1	Mute			Pin 79 output MUTE	*
						Other than above				PROHIBIT				
	General purpose 3									EXT_CTL3 (Pin36)				
			0							L			General purpose OUT3	*
			1							H				
	General purpose 4									EXT_CTL4 (Pin38)				
		0								L			General purpose OUT4	*
		1								H				

Serial Control Specification

1. Slave address



2. DATA TRANSFER MANUAL : [1] is High level. [0] is Low level.

I^{2}C-BUS control system is adopted in SW LSI. SW LSI is controlled by SCL (Serial Clock) and SDA (Serial Data) At first, please set up the START condition[*1] by these two terminals (SCL and SDA). And next, please input the 8bits data, which should be synchronized with SCL into SDA terminal. Still more, please give priority to high rank bit at data transfer order (MSB→LSB). The 9th bit is called as ACK (Acknowledge), SW LSI sends [0] to the SDA terminal during SCL [1] period. So, please open the port of microprocessor during this period. LV71081E adopt auto-increment, so you input only first group-address and you can transfer data in order. As thus the Data transfer Stop condition[*2] is finished.

[*1] SDA rise up during SCI is [1]

[*2] SDA fall down during SCL is [1]

3. TRANSFER DATA FORMAT

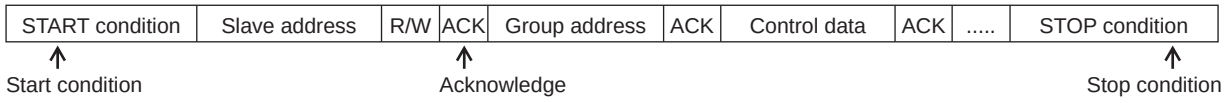
The transfer data is composed by START condition, Slave address, Group address[*1], data, and STOP condition.
After setting up the START condition, please transfer the Slave Address (regulated as “1001000” in SW LSI). Group and next control data[*2] (Please see the Fig.1)
Slave Address is composed by 7bits, and this bit 8th bit[*3] should be set as [0].

The both of Group address and control data are composed by 8bits, and the one control action is defined with combination of these two data. And if you want to control 2 or more groups at the same mode, you can realize it by sending some control data together.
The data makes meaning with all bits, so you cannot stop the sending until all data transfer is over.
But LV71081E adopt auto-increment, for example you can stop to transfer STOP condition after group 2 data.
If you want to stop transfer action, please transfer the STOP condition without fail.

[*1/2] There are 8 control groups.

[*3] This 8th bit called as R/W bit, and this bit shows the data transmission direction. [0] means send mode (accept mode with SW LSI) and [1] means accept mode (send mode with SW LSI) fundamentally. But SW LSI is not equipped with such a data out function, please keep this bit as [0].

Fig. 1 DATA STRUCTURE



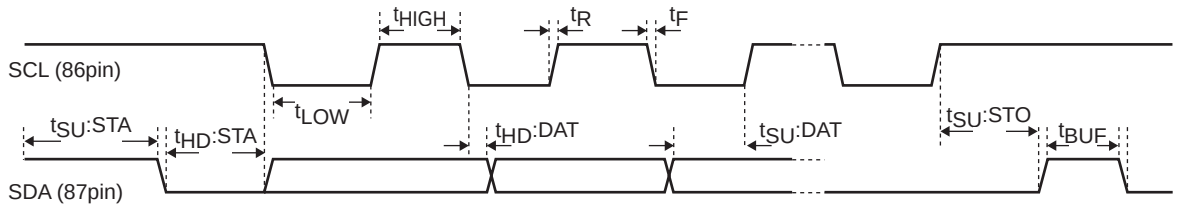
4. INITIALIZE AND OTHERS

SW LSI is initialized as the following mode for circuit protection. Please see “SERIAL CONTROL TABLE”.

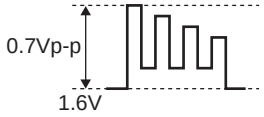
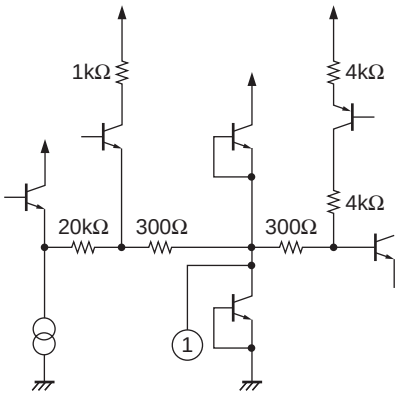
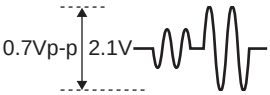
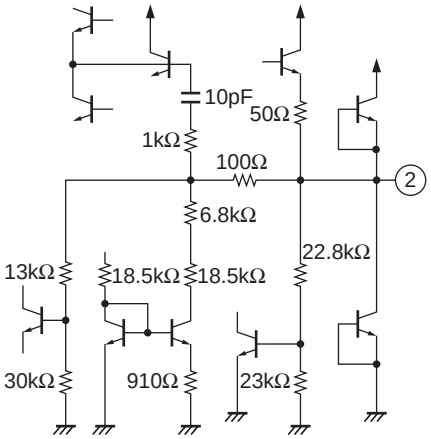
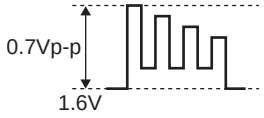
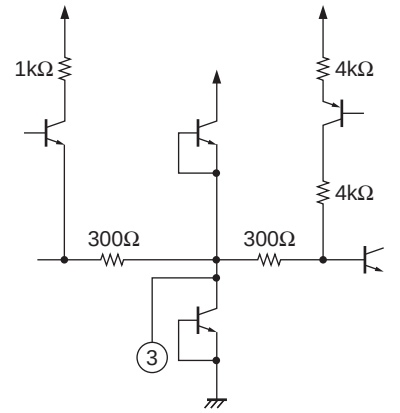
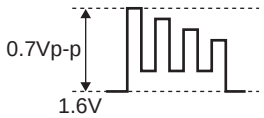
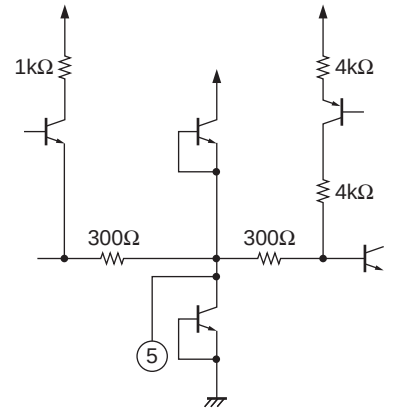
Characteristics of the SDA and SCL 1/0 stages for SW LSI

Parameter	Symbol	Min	Max	Unit
LOW level input voltage	V_{IL}	0	0.8	V
HIGH level input voltage	V_{IH}	3.0	5.0	V
LOW level output current	I_{OL}		3.0	mA
SCL clock frequency	f_{SCL}		400	kHz
Set-up time for a repeated START condition	t_{SU} : STA	0.6		μs
Hold time START condition. After this period, the first clock pulse is generated.	t_{HD} : STA	0.6		μs
LOW period of the SCL clock	t_{LOW}	1.3		μs
Rise time of both SDA and SDL signals	t_R	0	0.3	μs
HIGH period of the SCL clock	t_{HIGH}	0.6		μs
Fall time of both SDA and SDL signals	t_F	0	0.3	μs
Data hold time:	t_{HD} : DAT	0	0.9	μs
Data set-up time	t_{SU} : DAT	100		ns
Set-up time for STOP condition	t_{SU} : STO	0.6		μs
BUS fredd time between a STOP and START condition	t_{BUF}	1.3		μs

Fig.2 Definition of timing.



Pin Function

Pin No.	Pin name	DC voltage	Signal wave form	In put/Out put form
P1	AV2R/C_IN	1.6V R		
		2.1V Chroma		
P2	REG 2.5VA	2.5V	DC	
P3	AV2 G_IN	1.6V G		
P4	GND_VD			
P5	AV2 B_IN	1.6V B		
P6	V_{CC} 5V_VD			
P7	N.C.			
P8	V_{CC} 5V_RGB			

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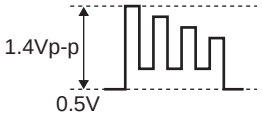
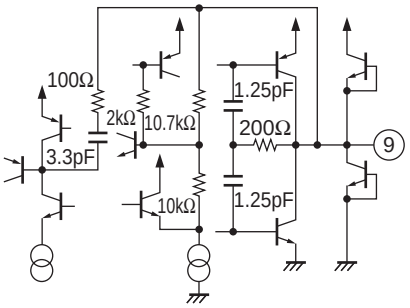
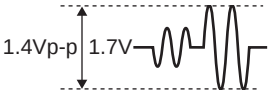
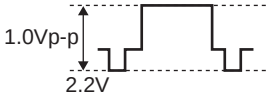
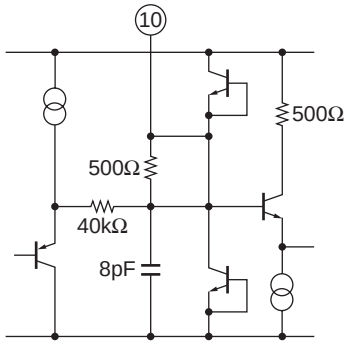
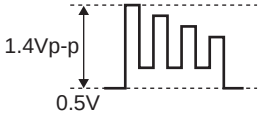
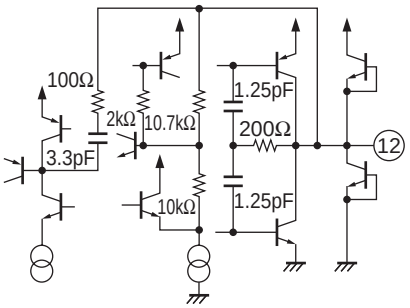
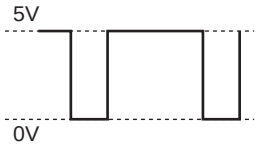
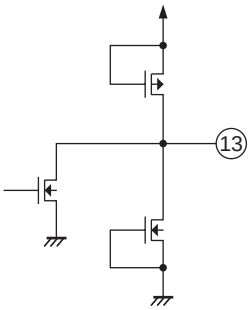
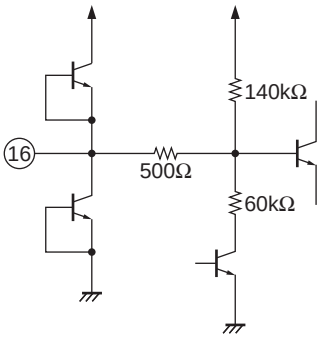
Pin No.	Pin name	DC voltage	Signal wave form	In put/Out put form
P9	AV1 R/C_OUT	0.5V R		
		1.7V Chroma		
P10	SYNC_SEP_LPF	1.0V Y		
P11	N.C.			
P12	AV1 B_OUT	0.5V B		
P13	EXT_CTL1			
P14	N.C.			
P15	N.C.			
P16	Audio_Mute_ Filter			

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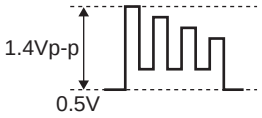
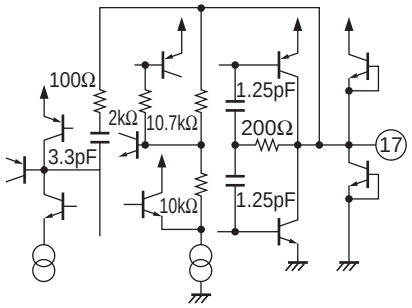
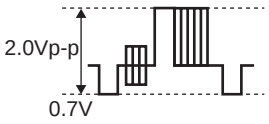
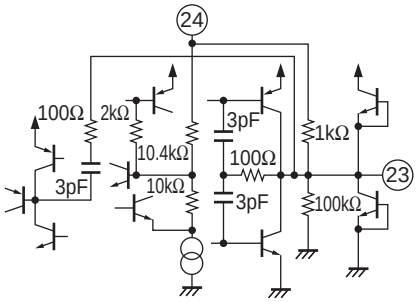
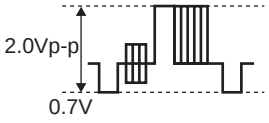
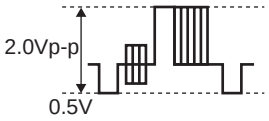
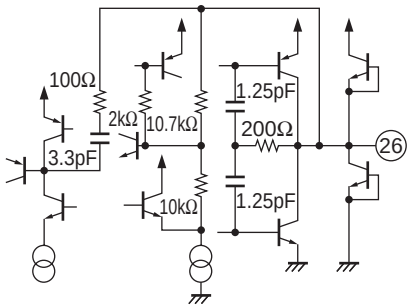
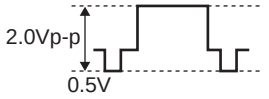
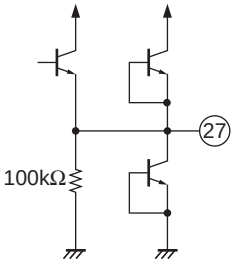
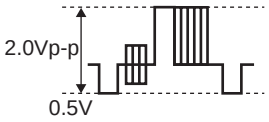
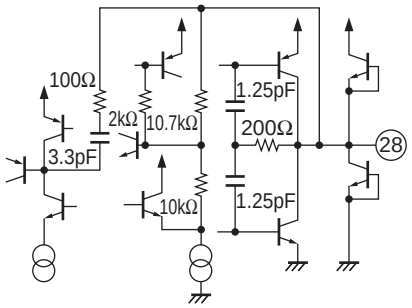
Pin No.	Pin name	DC voltage	Signal wave form	In put/Out put form
P17	AV1 G_OUT	0.5V G		
P18	GND_RGB			
P19	N.C.			
P20	N.C.			
P21	GND_VL			
P22	N.C.			
P23	V_OUT (Line_OUT)	0.7V Video		
P24	V_SAG_IN (Line_OUT)	0.7V Video		
P25	V_{CC} 5V_VL			
P26	AV1 V_OUT	0.5V Video		
		0.5V Y		
P27	AV1 FSS_OUT	Low : 0.5V Midol : 6.0V High : 11.1V	DC	
P28	AV2 V_OUT	0.5V Video		
P29	GND_VC			

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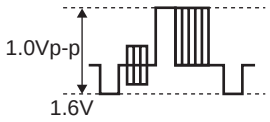
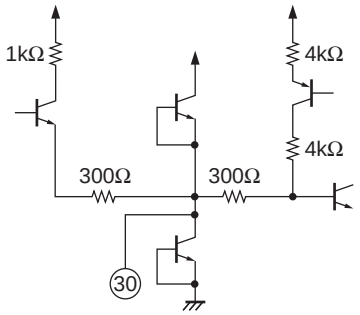
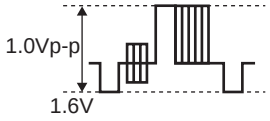
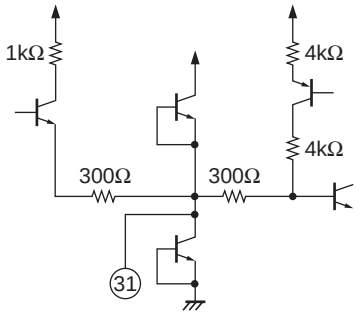
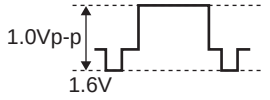
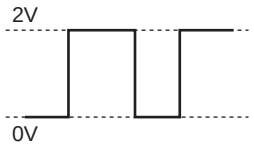
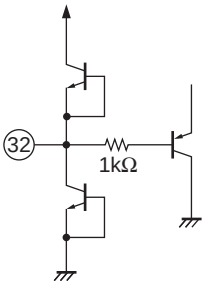
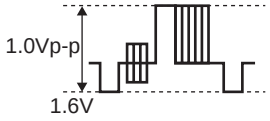
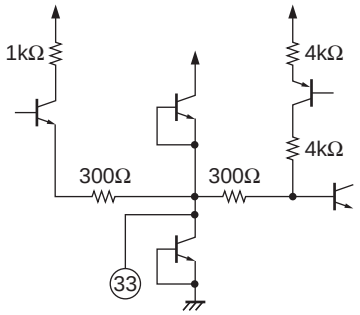
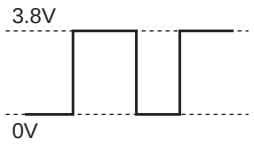
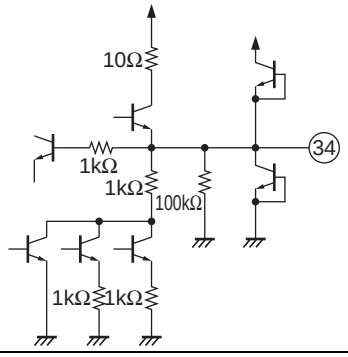
Pin No.	Pin name	DC voltage	Signal wave form	In put/Out put form
P30	Tuner1 V_IN	1.6V Video		
P31	AV2 V/Y_IN	1.6V Video		
		1.6V Y		
P32	AV2 FB_IN			
P33	AV1 V_IN	1.6V Video		
P34	AV1 FB_OUT	L : 0V H : 3.8V Through :0/3.8V		

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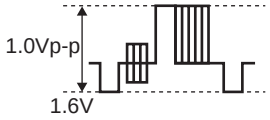
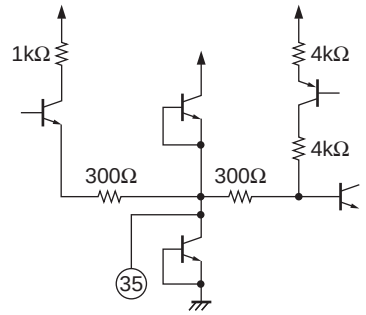
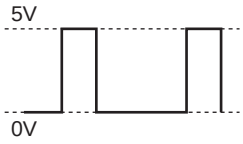
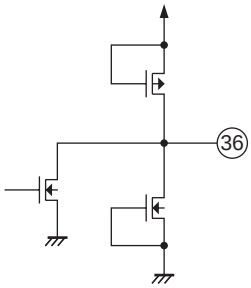
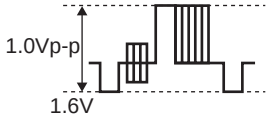
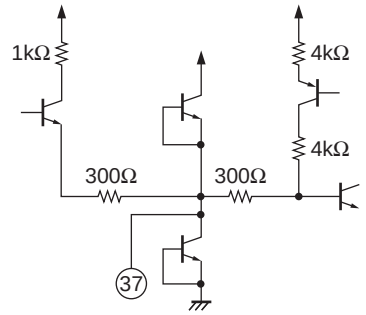
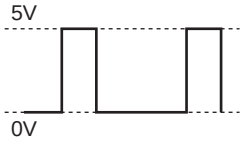
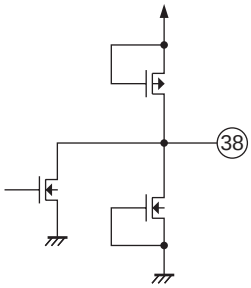
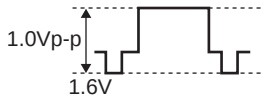
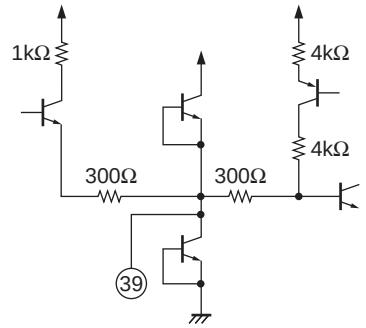
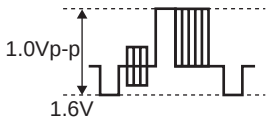
Pin No.	Pin name	DC voltage	Signal wave form	In put/Out put form
P35	AV4 V_IN	1.6V Video		
P36	EXT_CTL3			
P37	AV3 V_IN	1.6V Video		
P38	EXT_CTL4			
P39	AV4 Y_IN/ Tuner2 V_IN	1.6V Y		
		1.6V Video		
P40	V_{CC} 5V_VC			

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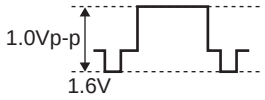
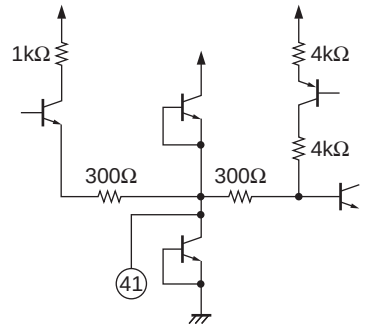
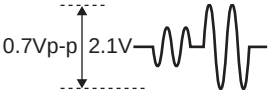
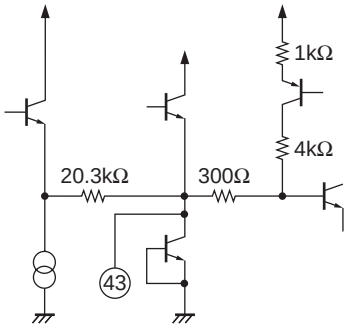
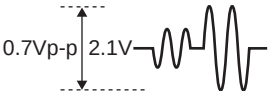
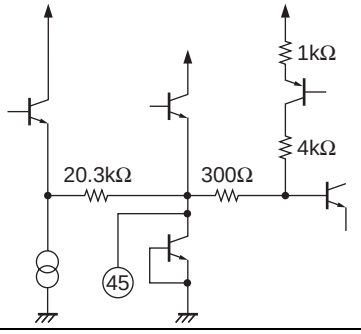
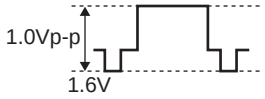
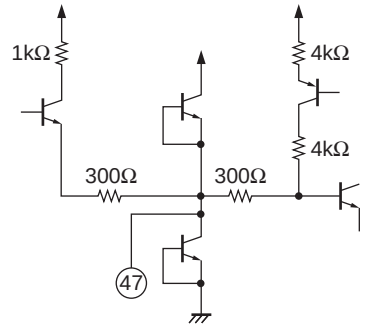
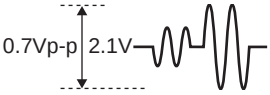
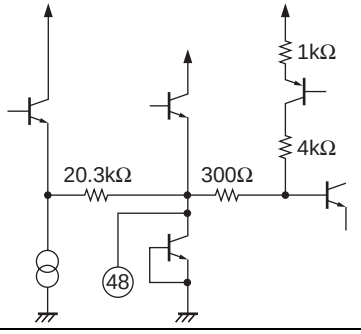
Pin No.	Pin name	DC voltage	Signal wave form	In put/Out put form
P41	AV3 Y_IN	1.6V Y		
P42	V_{CC} 5V_ALL	5V	DC	
P43	AV4 C_IN	2.1V Chroma		
P44	GND_REF	0V	DC	
P45	AV3 C_IN	2.1V Chroma		
P46	V_{CC} 11.6V_A	11.6V	DC	
P47	VCR Y_IN	1.6 Y		
P48	VCR C_IN	2.1V Chroma		

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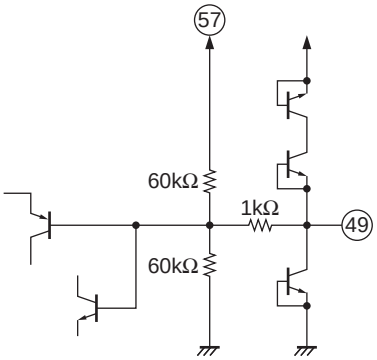
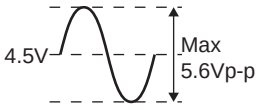
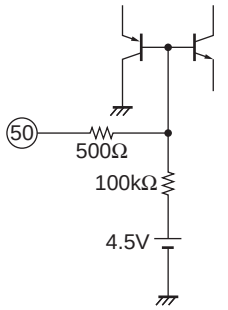
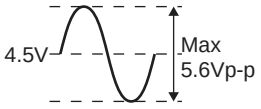
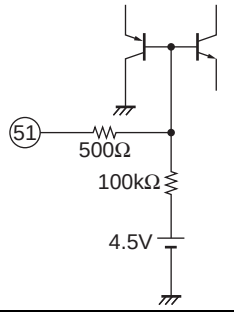
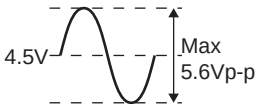
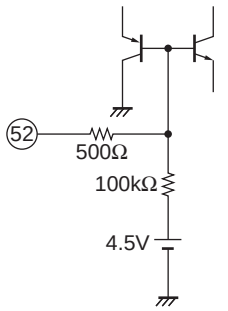
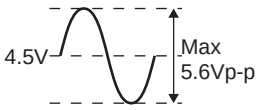
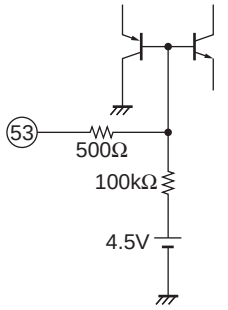
Pin No.	Pin name	DC voltage	Signal wave form	In put/Out put form
P49	REF 4.5V	4.5V		
P50	AV3 R_IN	4.5V		
P51	AV4 R_IN/ Tuner2 R_IN	4.5V		
P52	AV1 R_IN	4.5V		
P53	AV2 R_IN	4.5V		

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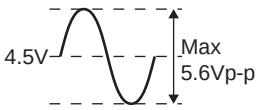
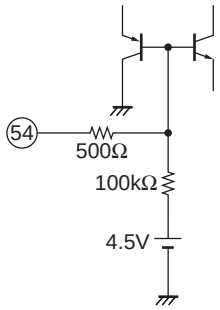
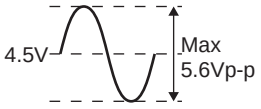
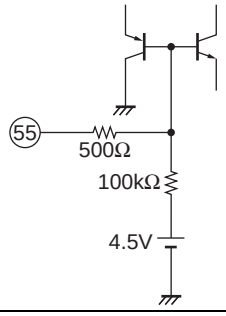
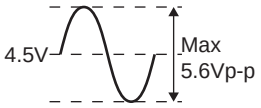
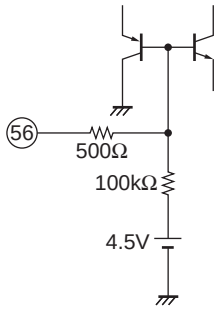
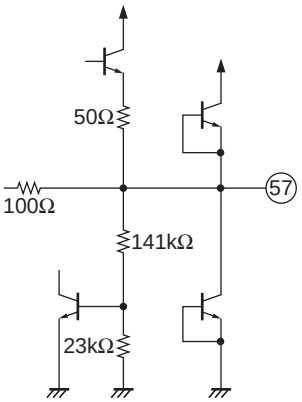
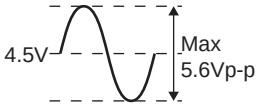
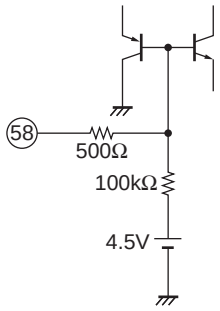
Pin No.	Pin name	DC voltage	Signal wave form	In put/Out put form
P54	Tuner1 R_IN	4.5V		
P55	VCR R_IN	4.5V		
P56	A_DAC R_IN	4.5V		
P57	REG 9V AR	9V	DC	
P58	AV3 L_IN	4.5V		

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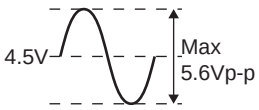
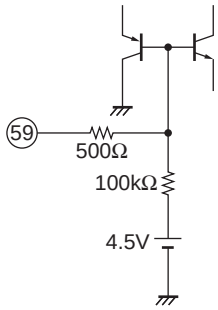
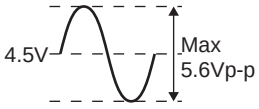
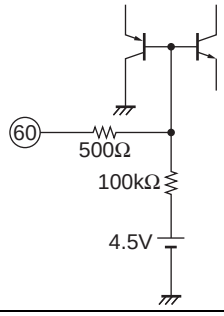
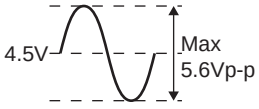
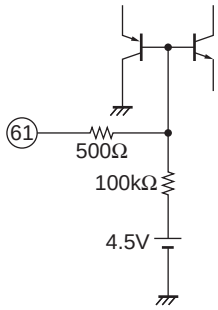
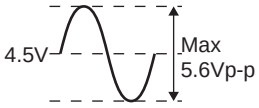
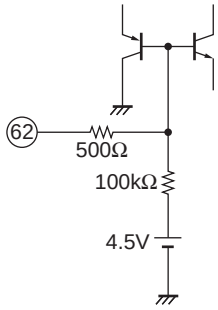
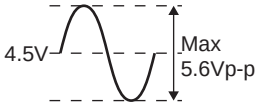
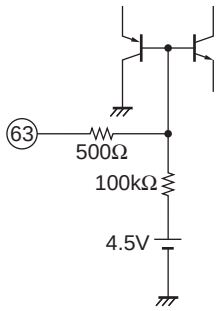
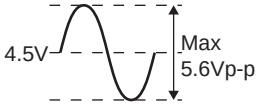
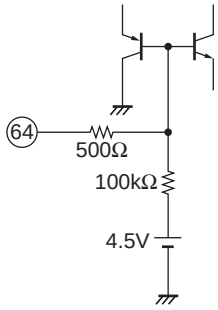
Pin No.	Pin name	DC voltage	Signal wave form	In put/Out put form
P59	AV4 L_IN/ Tuner2 L_IN	4.5V		
P60	AV1 L_IN	4.5V		
P61	AV2 L_IN	4.5V		
P62	Tuner1 L_IN	4.5V		
P63	VCR L_IN	4.5V		
P64	A_DAC L_IN	4.5V		

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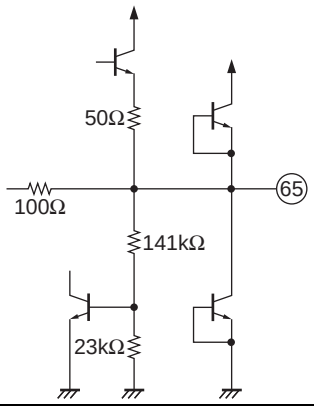
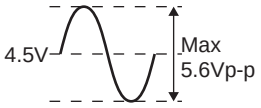
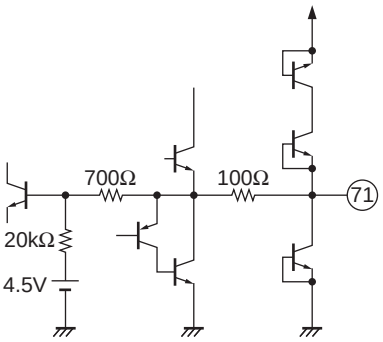
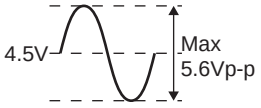
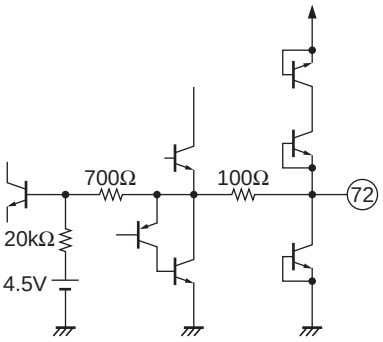
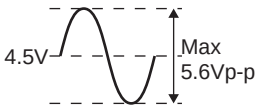
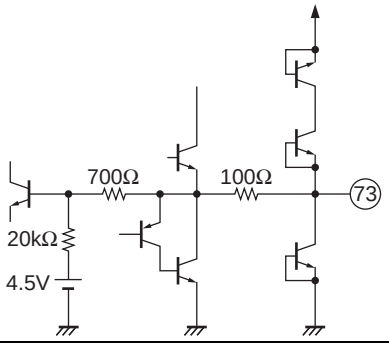
Pin No.	Pin name	DC voltage	Signal wave form	In put/Out put form
P65	REG 9V AL	9V	DC	
P66	GND_REG	0V	DC	
P67	N.C.			
P68	N.C.			
P69	N.C.			
P70	N.C.			
P71	AV1 L_OUT	4.5V		
P72	AV1 R_OUT	4.5V		
P73	AV2 L_OUT	4.5V		

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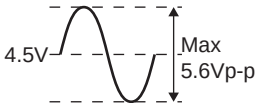
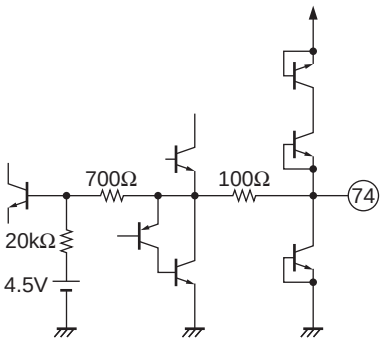
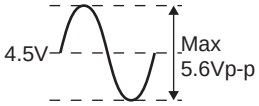
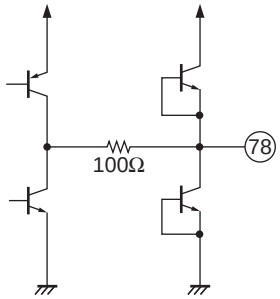
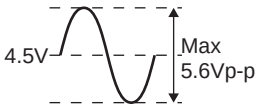
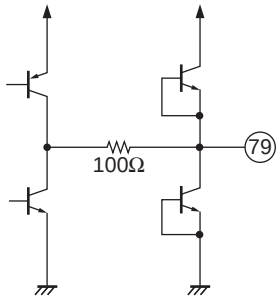
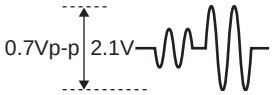
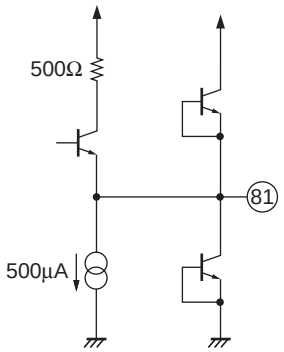
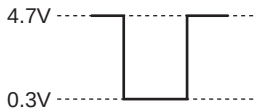
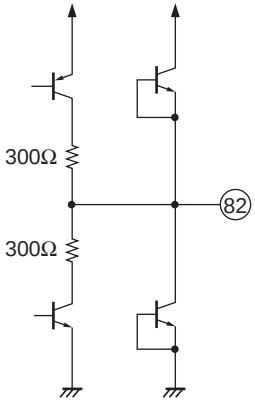
Pin No.	Pin name	DC voltage	Signal wave form	In put/Out put form
P74	AV2 R_OUT	4.5V		
P75	GND_AR	0V	DC	
P76	N.C.			
P77	N.C.			
P78	A_DAC L_OUT	4.5V		
P79	A_DAC R_OUT	4.5V		
P80	GND_AL			
P81	DAC C_OUT	2.1V		
P82	V_SYNC_OUT			

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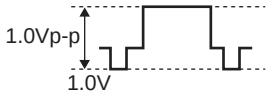
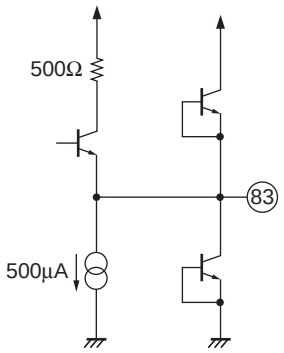
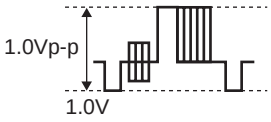
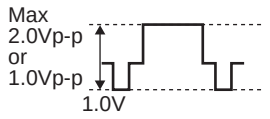
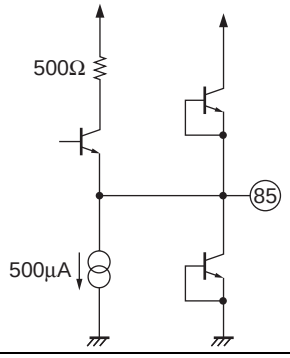
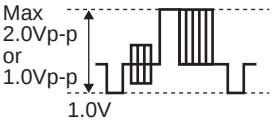
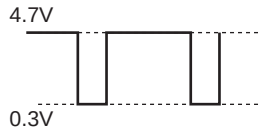
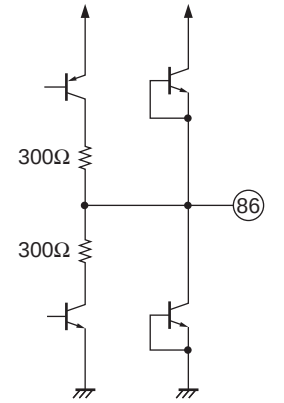
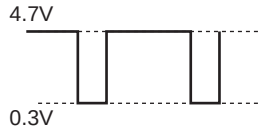
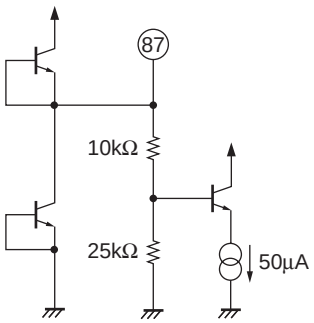
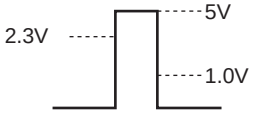
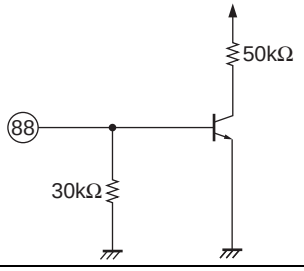
Pin No.	Pin name	DC voltage	Signal wave form	In put/Out put form
P83	DAC V/Y_OUT	1.0V Y		
		1.0V Video		
P84	V_{CC} 5V_VSW			
P85	Slicer_OUT	1.0V Y		
		1.0V Video		
P86	C_CYNC_OUT			
P87	V_DET_IN			
P88	SCL_IN			

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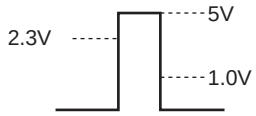
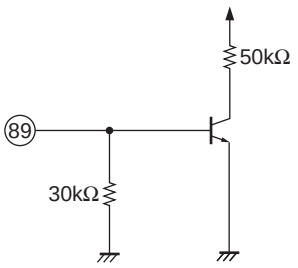
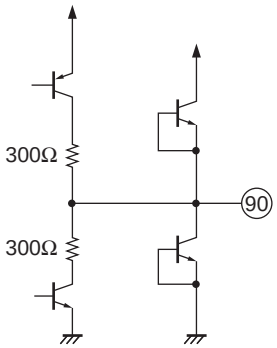
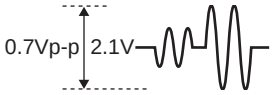
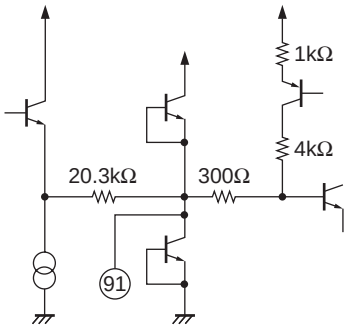
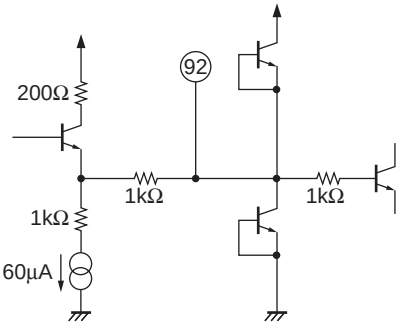
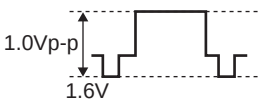
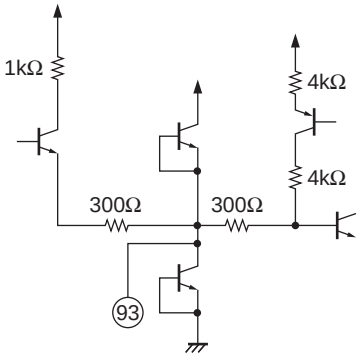
Pin No.	Pin name	DC voltage	Signal wave form	In put/Out put form
P89	SDL_IN			
P90	V_DET_OUT	4.7V with signal 0V without signal	DC	
P91	ENC. C_IN	2.1V Chroma		
P92	V_DET_FIL		DC	
P93	ENC. Y_IN	1.6V Y		
P94	V_{CC}_LOGIC			

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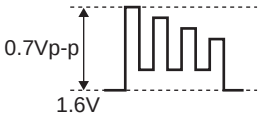
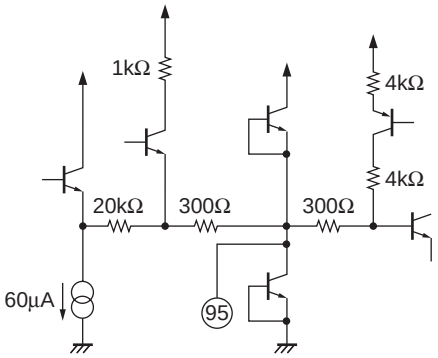
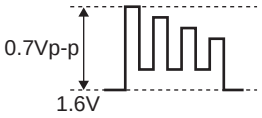
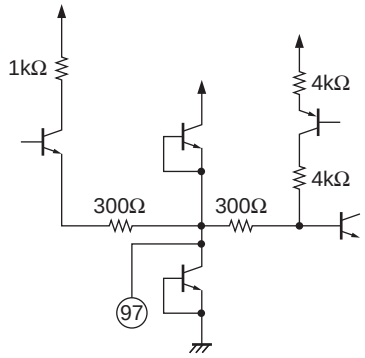
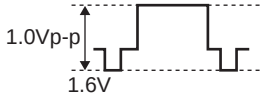
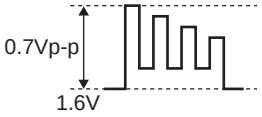
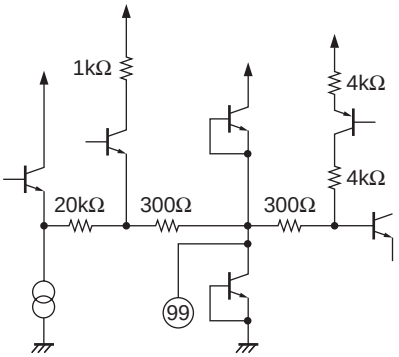
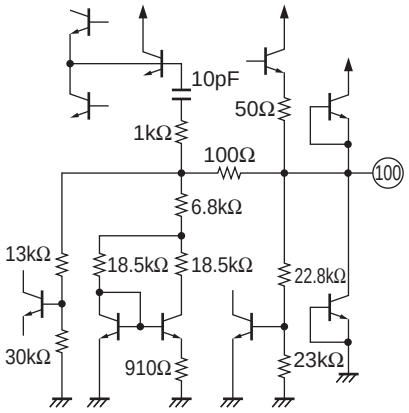
Pin No.	Pin name	DC voltage	Signal wave form	In put/Out put form
P95	ENC. R/ R-Y_IN	1.6V R		
		2.1V R-Y		
P96	GND_LOGIC			
P97	ENC. G/Y_IN	1.6V G		
		1.6V Y		
P98	GND_VSW			
P99	ENC. B/ B-Y_IN	1.6V B		
		2.1V B-Y		
P100	REG 2.5V	2.5V	DC	

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