MOS INTEGRATED CIRCUIT

M 106

TV MICROPROCESSOR INTERFACE

- 6 PWM D/A CONVERTERS, WITH 64 STEP RESOLUTION, FOR ANALOGUE CONTROLS
- 13 BIT (8192 STEP) PULSE WIDTH-RATE MULTIPLIER D/A CONVERTER FOR TUNING VOLTAGE. BUILT IN ANALOGUE SWITCH.
- CRT DISPLAY SECTION BASED ON A 64 x 64 FULLY PROGRAMMABLE MATRIX, UNDER SOFTWARE CONTROL, WORKS WITH ANY TV STANDARD
- OPEN DRAIN OUTPUTS RATED UP TO 13.2V
- MAIN 5V POWER SUPPLY (12V USED FOR BIAS)
- STANDARD 40 PIN PLASTIC PACKAGE

The M 106 is a programmable LSI device for microprocessor controlled applications in TV and industrial control fields. The M 106 uses state-of-the-art N-Channel MOS Silicon gate technology, with a single +5V power supply and TTL compatible inputs and outputs. A +12V supply is used for bias of the analogue switch circuit built on the chip.
The microprocessor interface includes a single phase clock input, a bidirectional 8 bit system bus, two strobe inputs and an interrupt request output. A total of 7 variable duty cycle output signals are available. After simple RC filtering these signals become the analogue outputs of the system. One blanking and three colour outputs are provided to display alphanumeric or graphic data on a CTV screen. Eight general purpose digital outputs are provided with open-drain configuration.
The M 106 is available in a standard 40 pin dual-in-line plastic package.

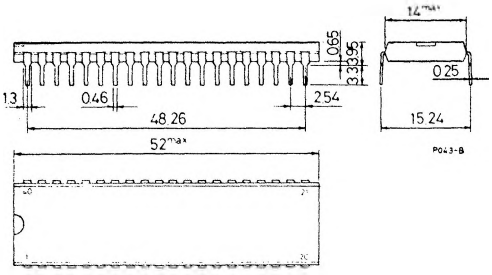
ABSOLUTE MAXIMUM RATINGS*

V_{DD} **	Supply voltage	-0.3 to 7	V
V_{ref}	Reference voltage	-0.3 to 7	V
V_{GG}	Bias voltage	-0.3 to 14	V
V_I	Input voltage	-0.3 to 7	V
$V_{O(off)}$	Off-state output voltage: P0 to P6; Q0 to Q7	-0.3 to 14	V
	all other outputs	-0.3 to 7	V
I_O	Output current: all outputs except pins 25, 26, 27, 28	max. 5	mA
	pins 25, 26, 27, 28	max. 15	mA
P_{tot}	Total package power dissipation	0.8	W
T_{op}	Operating temperature	0 to 70	°C
T_{stg}	Storage temperature	-65 to 150	°C

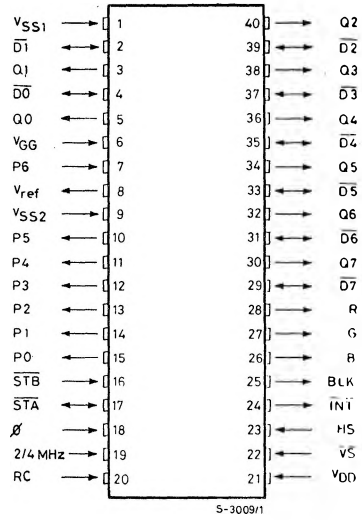
* Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
** All voltage are referred to $V_{SS1} = V_{SS2}$.

ORDERING NUMBER : M 106 B1

MECHANICAL DATA (dimensions in mm)



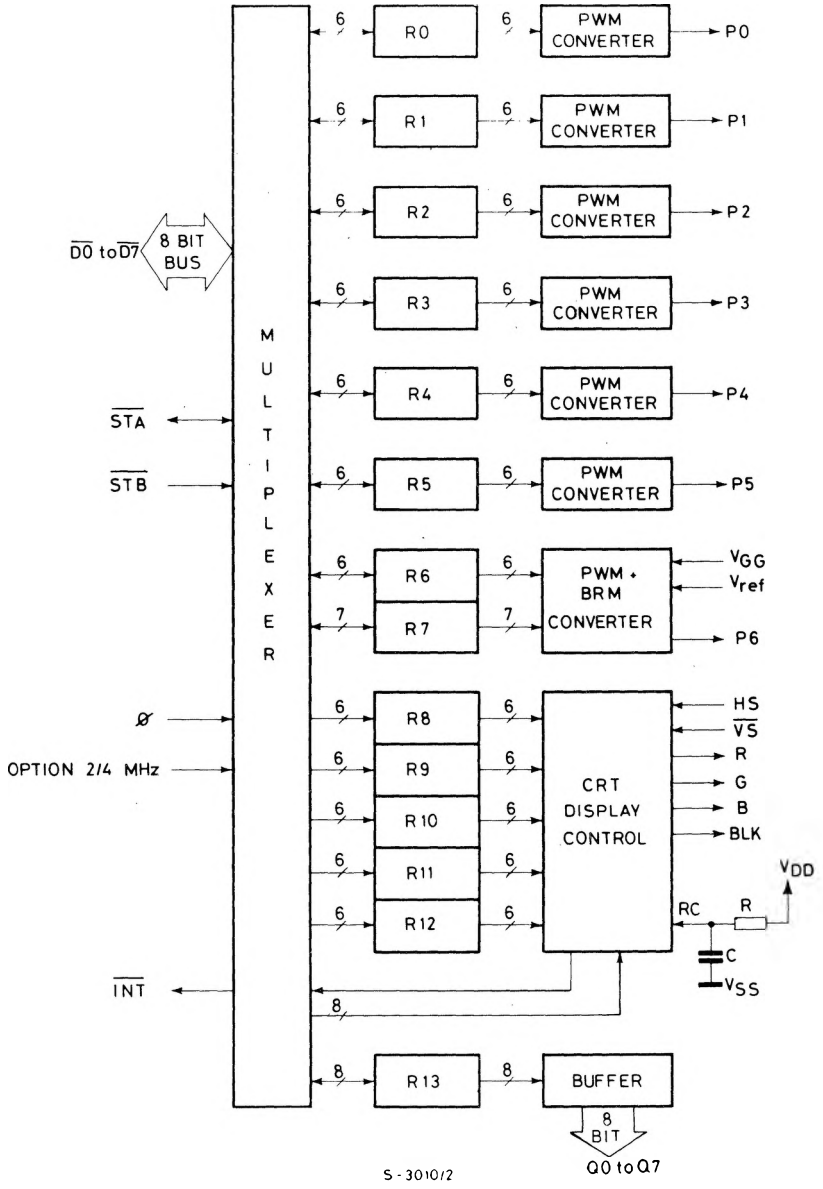
PIN CONNECTIONS



RECOMMENDED OPERATING CONDITIONS

V_{DD}	Supply voltage	4.5 to 5.5	V
V_{ref}	Reference voltage	5 to 6	V
V_{GG}	Bias voltage	10.8 to 13.2	V
V_I	Input voltage	0 to V_{DD}	V
$V_{O(off)}$	Output off voltage: P0 to P6; Q0 to Q7	max 13.2	V
	all other outputs	max V_{DD}	V
I_O	Output current: all outputs except pins 25, 26, 27, 28	max 2	mA
	pins 25, 26, 27, 28	max 8	mA
ϕ	Clock frequency (selectable)	(pin 19 at V_{DD}) 2	MHz
		(pin 19 at V_{SS}) 4	MHz
f	Oscillator frequency	3.2	MHz
R	Resistance of the clock oscillator	2.2 to 10	kΩ
C	Capacitance of the clock oscillator	10 to 30	pF
T_{op}	Operating temperature	0 to 70	°C

BLOCK DIAGRAM



STATIC ELECTRICAL CHARACTERISTICS (Over recommended operating conditions
Typ. values are at T_{amb}= 25°C, V_{DD}= 5V; V_{Ref}= 5V; V_{GG}= 12V)

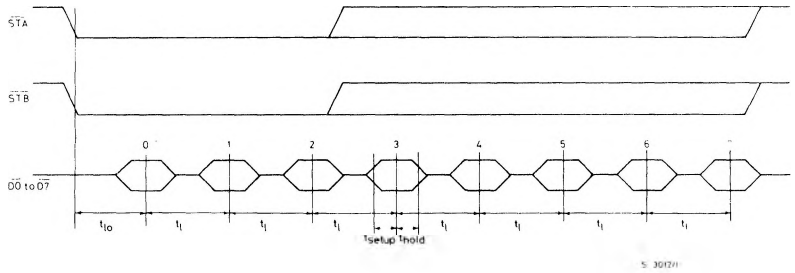
Parameter			Test conditions	Values			Unit
				Min.	Typ.	Max.	
V_{IH}	Input high voltage	All input pins except 22-23 (H_s-$\overline{V}_s$)		2.5		V_{DD}	V
		pins 22-23 (H_s-$\overline{V}_s$)		3		V_{DD}	
V_{IL}	Input low voltage	All inputs excepts pins 22-23 (H_s-$\overline{V}_s$))		0		0.8	V
		pins 22-23 (H_s-$\overline{V}_s$)		0		0.4	
I_I	Input leakage current	All inputs except pin 18	V_I = 0 to 5.5V			10	μA
I_ϕ	Input bias current	pin 18	V_ϕ = 5.5V	10		70	μA
V_{OL}	Output low voltage	All outputs except pins 25-26-27-28-7	I_{OL}= 1.6 mA			0.4	V
		pins 25-26-27-28	I_{OL}= 8 mA			1	V
		pin 7	I_{OL}= 0.25 mA		30	45	mV
V_{OH}	Output high voltage	pin 7	I_{OH}= -0.25 mA		V_{DD}-30	V_{DD}-45	mV
$I_{O(off)}$	Leakage current	All output except pins 3-5-25-26-27-28 30-32-34-36-38-40	$V_{O(off)}$= 5.5V			10	μA
		pins 3-5-25-26-27-28 30-32-34-36-38-40	$V_{O(off)}$= 13.2V			50	μA
I_{DD}	Supply current	pins 3-5-25-26-34	V_{DD}= 5.5V			60	mA
I_{GG}	Bias current		V_{GG}= 13.2V			300	μA

Note: The $\overline{V}_s$ and H_s inputs have Schmitt-trigger action for accepting slow transition time signals.

DYNAMIC ELECTRICAL CHARACTERISTICS

Parameter		Test conditions	Values			Unit
			Min.	Typ.	Max.	
t_{l0}	Loading time of the first byte from the strobe display command (STA and STB both low)	see fig. 1		26		μs
t_l	Loading time of any successive byte from the end of the previous load time			24		μs
t_{setup}	Setup time			4		μs
t_{hold}	Hold time			4		μs

Fig. 1



DESCRIPTION

ϕ - System clock

The ϕ input (pin 18) must be connected to the microprocessor clock, or to the clock oscillator pin in the case where the microprocessor has a built in clock generator.
The clock signal can be 2 or 4 MHz. Pin 19 must be connected to V_{DD} if the frequency is 2 MHz, to V_{SS} if it is 4 MHz.

Internal registers load and read operations

M 106 can be fully programmed by loading a set of internal registers.
Table 1 shows the binary address code and function of each internal register.
The loading of each register, as shown by fig. 2, is performed in two steps: in the first phase, the four bit address code ($\overline{D0}$ to $\overline{D3}$) is sent on the bus, and latched by the $\overline{STA}$ strobe signal; in the second phase the bus carries the 6 to 8 bit register content which is transferred to the addressed register by the $\overline{STB}$ strobe signal.
When both $\overline{STA}$ and $\overline{STB}$ are in the HIGH state, the content of the addressed register will be read back to the bus. The read operation is not allowed for registers 8 to 12.

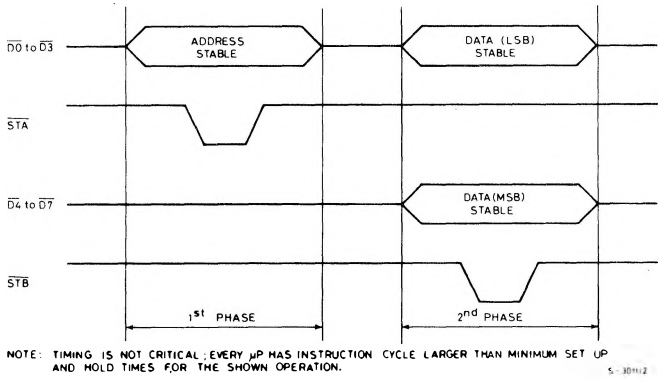
Table 1 - Summary of the internal registers

N°	ADDRESS $\overline{D3}$	$\overline{D2}$	$\overline{D1}$	$\overline{D0}$	Number of bit	Function
0	H	H	H	H	6	Converter n. 0 (PWM)
1	H	H	H	L	6	Converter n. 1 (PWM)
2	H	H	L	H	6	Converter n. 2 (PWM)
3	H	H	L	L	6	Converter n. 3 (PWM)
4	H	L	H	H	6	Converter n. 4 (PWM)
5	H	L	H	L	6	Converter n. 5 (PWM)
6	H	L	L	H	6	Converter n. 6 MSB (PWM)
7	H	L	L	L	7	Converter n. 7 LSB (BRM)
8	L	H	H	H	6	Window upper side position
9	L	H	H	L	6	Window lower side position
10	L	H	L	H	6	Window left side position
11	L	H	L	L	6	Window right side position
12	L	L	H	H	6	CRT display control
13	L	L	H	L	8	Open drain digital outputs
14	L	L	L	H	–	Reset (only for testing)
15	L	L	L	L	–	Not used

Table 2 - Loading and reading of the internal registers

$\overline{STA}$	$\overline{STB}$	Function
H	H	the content of the addressed register is read back (except for R8 to R12)
L	H	address loading
H	L	data loading
L	L	pattern loading for CRT display

Fig. 2



D/A converters for analogue controls

The 6 bit contents of registers 0 to 5, after a pulse-width conversion and external filtering, are used for analogue commands as volume, brightness, colour saturation, contrast, tone and fine tuning.
The pulse width modulated output has a fixed period of 64 microseconds and variable width. The output is open drain, can be filtered by a simple RC network and can be varied from 0V to the reference voltage (13.2V max) in $2^6 = 64$ steps.

Tuning voltage D/A converter

Registers 6 and 7 may be considered as a single 13 bit register. The corresponding outputs value is normally used as a tuning voltage for a varicap tuner. The conversion uses a double modulation system, in order to minimize the ripple after the filter. The 6 most significant bits (register 6) are converted using the same pulse width modulation technique as registers 0 to 5.
The 7 least significant bits (register 7) generate a series of pulses with variable width and frequency (bit rate multiplier).
This approach greatly reduces the amplitude of the low frequency components in the output voltage, and allows an easier and more efficient filtering.
The converter's output, P6, uses an internal analogue switch, operating in a push-pull mode, and switches a very precise reference voltage, which is connected to the V_{ref} pin.
The 0 volt level, in order to minimize the ground noise, is supplied through a dedicated pin V_{SS2}, that is externally connected to ground.
A 12V bias voltage must be connected to the V_{GG} pin in order to operate the output stage in the push-pull mode.

On screen display

The on-screen display interface uses a vertical sync signal applied to the $\overline{V}_S$ input and horizontal sync signal applied to the H_S input.
A "vertical clock" is internally generated by dividing the line frequency H_S by a number N which defines the height of the matrix element.
Assigning to N a value of 4/5/6 the height of the corresponding matrix element becomes 4/5/6 lines.
The choice of one of these values of N will adapt the M 106 to display on any video standard.
An internal RC oscillator, synchronized by the H_S input, gives a "horizontal clock", whose period

DESCRIPTION (continued)

defines the width of the matrix element. The frequency must be adjusted in order to have a width equal to 1/64th of the actual width of the screen.

The data to be displayed on the screen is normally contained in a rectangular "window". Inside the window the BLK output generates a blanking signal, thus creating a black rectangular background for the image. Position, height and width of the window are programmable by loading in registers 8-9-10-11 a 6 bit position value of each side of the window. The value is calculated in terms of the number of vertical or horizontal clock pulses from an origin.

The origin (0, 0) corresponds to the trailing edge of the $\overline{V}_S$ and H_S pulses and is therefore located in the upper left corner of the screen.

Inside the M 106, a dual 64 bit shift register synchronized by the horizontal clock, repeats the same pattern over N lines using the first shift register, while the μP can load the second one with the new pattern to be used in the next lines. Afterwards the new pattern content is transferred in parallel into the first register. The loading of the second shift register is synchronized by the ϕ clock. This takes 8 sequential bytes, with the timing shown in fig. 1. The loading time for each byte is 24 microseconds.

The loading begins when both $\overline{STA}$ and $\overline{STB}$ go LOW. The corresponding state is decoded as a "strobe display" command.

If the "strobe display" state is terminated by the μP before the internal shift register is completely loaded, the remaining bits are zero-filled.

The display control register (12) defines the start and the end of the display function, the combination of the colour outputs enabled (and therefore the colour of the image) and the timing signals used during the load operation.

Table 3 shows the function of each bit of the display control register.

No timing signals are used if the pattern doesn't change from line to line of the display (vertical or horizontal bands). In this case the pattern can be loaded asynchronously only at the beginning, and will be automatically repeated until the window is completely scanned.

The timing signals must be enabled for displaying character, because the line pattern is variable and must be loaded in synchronism with the screen scan. The $\overline{STA}$ pin, normally used as a strobe input, becomes bidirectional and generates for each frame a single pulse, negative going, and approximately 45 microseconds long, N lines before the beginning of the window.

This signal is used by μP to initiate the first load operation.

The $\overline{INT}$ gives a series of pulses for each frame, with a period of N lines, starting N lines before the beginning of the window and stopping N lines before the end of the window.

During the $\overline{STA}$ output pulse no control register loading is permitted and only the "strobe display" state is accepted.

Table 3 - CRT display control register (N° 12)

Bit	Function	Logic level L	Logic level H
0	Output R (Red)	disabled	enabled
1	Output B (Blue)	disabled	enabled
2	Output G (Green)	disabled	enabled
3	Nr. of lines each dot	5 (4*)	6
4	Timing outputs $\overline{INT}$-$\overline{STA}$	disabled	enabled
5	Display control	stop	start

* Available with metal option (contact local SGS-ATES sales office).