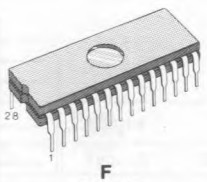
SGS-THOMSON MICROELECTRONICS

M27512

512K (64K x 8) NMOS UV ERASABLE PROM

PRELIMINARY DATA

- FAST ACCESS TIME: 200ns MAX M27512-2F1
- 0 TO +70°C STANDARD TEMPERATURE RANGE
- SINGLE +5V POWER SUPPLY
- LOW STANDBY CURRENT (40mA MAX)
- TTL COMPATIBLE
- FAST PROGRAMMING
- ELECTRONIC SIGNATURE



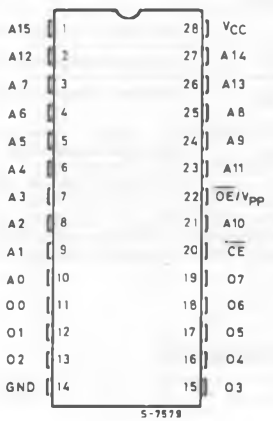
F
DIP-28
(Ceramic Bull's Eye)

(Ordering Information at the end of the datasheet)

DESCRIPTION

The M27512 is a 524,288-bit ultraviolet erasable and electrically programmable read only memory (EPROM). It is organized as 65,536 words by 8 bits and manufactured using SGS-THOMSON' NMOS-E3 process. The M27512 with its single +5V power supply and with an access time of 200ns, is ideal for use with high performance +5V microprocessor allowing full speed operation without the addition of performance-degrading WAIT states. The M27512 has an important feature which is to separate the output control, Output Enable ($\overline{OE}/V_{PP}$) from the Chip Enable control ($\overline{CE}$). The $\overline{OE}/V_{PP}$ control eliminates bus contention in multiple bus microproces sor systems. The M27512 also features a standby mode which reduces the power dissipation without increasing access time. The active current is 125mA while the maximum standby current is only 40 mA, a 70% saving. The standby mode is achieved by applying a TTL-high signal to the $\overline{CE}$ input. The M27512 enables implementation of new, advanced systems with firmware intensive architectures. The combination of the M27512s high density, and new advanced microprocessors having megabit addressing capability provides designers with opportunities to engineer user-friendly, high reliability, high-performance systems. The M27512 large storage capability enables it to function as a high density software carrier. Entire operating systems, diagnostics, high-level language programs and specialized application software can reside in a M27512 directly on a system's memory bus. This permits immediate microprocessor access and execution of software and eliminates the need for time consuming disk accesses and downloads. The M27512 has an "Electronic Signature" that allows programmers to automatically identify device type and pinout. The M27512 is available in a 28-lead dual in-line ceramic package glass lens (frit seal).

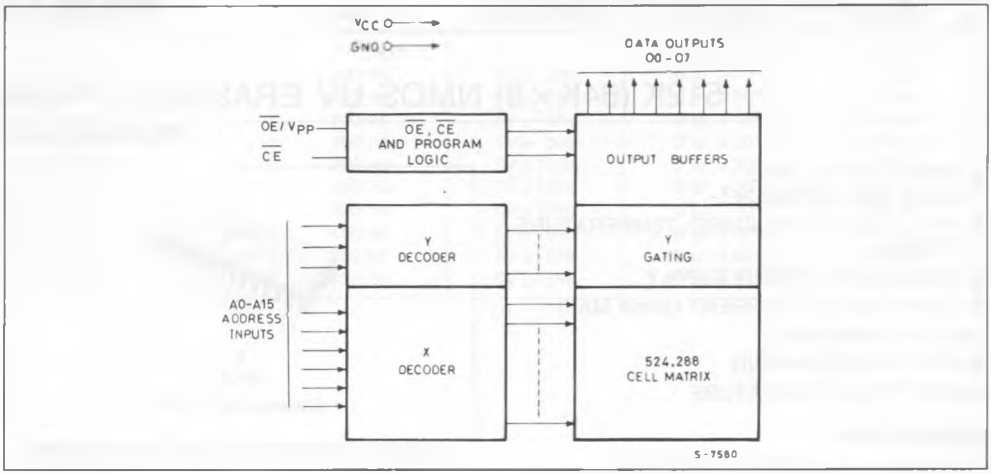
PIN CONNECTIONS



PIN NAMES

A0-A15	ADDRESS INPUT
$\overline{CE}$	CHIP ENABLE INPUT
$\overline{OE}/V_{PP}$	OUTPUT ENABLE INPUT
O0-O7	DATA INPUT/OUTPUT

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_I	All Input or Output voltages with respect to ground	+ 6.5 to − 0.6	V
V_{PP}	Supply voltage with respect to ground	+14 to − 0.6	V
T_{amb}	Ambient temperature under bias /F1 /F6	−10 to + 80 −50 to + 95	°C °C
T_{stg}	Storage temperature range	−65 to +125	°C
	Voltage on pin 24 with respect to ground	+13.5 to −0.6	V

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING MODES

MODE \ PINS	$\overline{CE}$ (20)	$\overline{OE}/V_{PP}$ (22)	A9 (24)	A0 (10)	V_{CC} (28)	OUTPUTS (11-13, 15-19)
READ	V_{IL}	V_{IL}	X	X	V_{CC}	D_{OUT}
OUTPUT DISABLE	V_{IL}	V_{IH}	X	X	V_{CC}	HIGH Z
STANDBY	V_{IH}	X	X	X	V_{CC}	HIGH Z
PROGRAM	V_{IL}	V_{PP}	X	X	V_{CC}	D_{IN}
PROGRAM INHIBIT	V_{IH}	V_{PP}	X	X	V_{CC}	HIGH Z
ELECTRONIC SIGNATURE	V_{IL} V_{IL}	V_{IL} V_{IL}	V_H V_H	V_{IL} V_{IH}	V_{CC} V_{CC}	MAN.CODE DEV.CODE

NOTE: X can be V_{IH} or V_{IL} V_H = 12V ±0.5V

READ OPERATION

DC AND AC CONDITIONS

Selection Code	F1/ – 2F1/ – 3F1/	– 25F1/ – 30F1	F6
Operating Temperature Range	0 to 70°C	0 to 70°C	– 40 to 85°C
V_{CC} Power Supply (1,2)	5V ±5%	5V ±10%	5V ±5%
V_{PP} Voltage (2)	$V_{PP} = V_{CC}$	$V_{PP} = V_{CC}$	$V_{PP} = V_{CC}$

DC AND OPERATING CHARACTERISTICS

Symbol	Parameter	Test Conditions	Values			Unit
			Min.	Typ. (2)	Max.	
I_{LI}	Input Load Current	$V_{IN} = 5.5V$			10	µA
I_{LO}	Output Leakage Current	$V_{OUT} = 5.5V$			10	µA
I_{CC1}	V_{CC} Current Standby	$\overline{CE} = V_{IH}$		20	40	mA
I_{CC2}	V_{CC} Current Active	$\overline{CE} = \overline{OE}/V_{PP} = V_{IL}$		90	125	mA
V_{IL}	Input Low Voltage		– 0.1		+ 0.8	V
V_{IH}	Input High Voltage		2.0		V_{CC} + 1	V
V_{OL}	Output Low Voltage	$I_{OL} = 2.1$ mA			0.45	V
V_{OH}	Output High Voltage	$I_{OH} = -400$ µA	2.4			V

AC CHARACTERISTICS

Symbol	Parameter	V_{CC} ± 5%	27512-2		27512		27512-3		Unit
		V_{CC} ± 10%			27512-25		27512-30		
		Test Conditions	Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay	$\overline{CE} = \overline{OE}/V_{PP} = V_{IL}$		200		250		300	ns
t_{CE}	$\overline{CE}$ to Output Delay	$\overline{OE}/V_{PP} = V_{IL}$		200		250		300	ns
t_{OE}	$\overline{OE}/V_{PP}$ to Output Delay	$\overline{CE} = V_{IL}$		75		100		120	ns
t_{DF}(3)	$\overline{OE}$ High to Output Float	$\overline{CE} = V_{IL}$	0	55	0	60	0	105	ns
t_{OH}	Output Hold from Address $\overline{CE}$ or $\overline{OE}$ Whichever Occurred First	$\overline{CE} = \overline{OE}/V_{PP} = V_{IL}$	0		0		0		ns

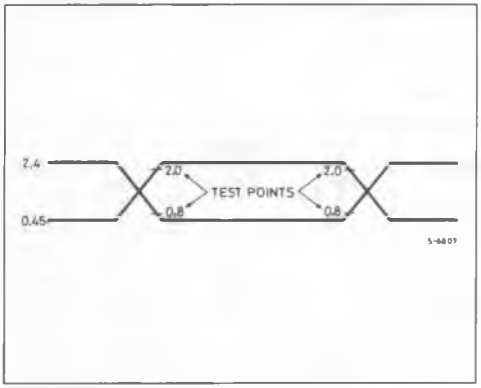
CAPACITANCE(4) (T_{amb} = 25°C, f = 1 MHz)

Symbol	Parameter	Test Conditions	Min.	Typ. (2)	Max.	Unit
C_{IN}	Input Capacitance	$V_{IN} = 0V$		4	6	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0V$		8	12	pF

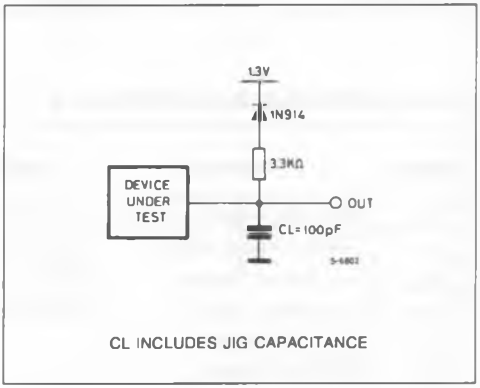
Notes: 1. V_{CC} must be applied simultaneously or before $\overline{OE}/V_{PP}$ and removed simultaneously or after $\overline{OE}/V_{PP}$.
2. Typical values are for T_{amb} = 25°C and nominal supply voltages.
3. This parameter is only sampled and not 100% tested. Output Float is defined as the point where data is no longer driven-see timing diagram.
4. This parameter is only sampled and not 100% tested.

AC TEST CONDITIONS
Output Load: 100pF + 1TTL Gate
Input Rise and Fall Times: ≤20ns
Input Pulse Levels: 0.45 to 2.4V
Timing Measurement Reference Levels: Inputs 0.8 and 2V
Outputs 0.8 and 2V

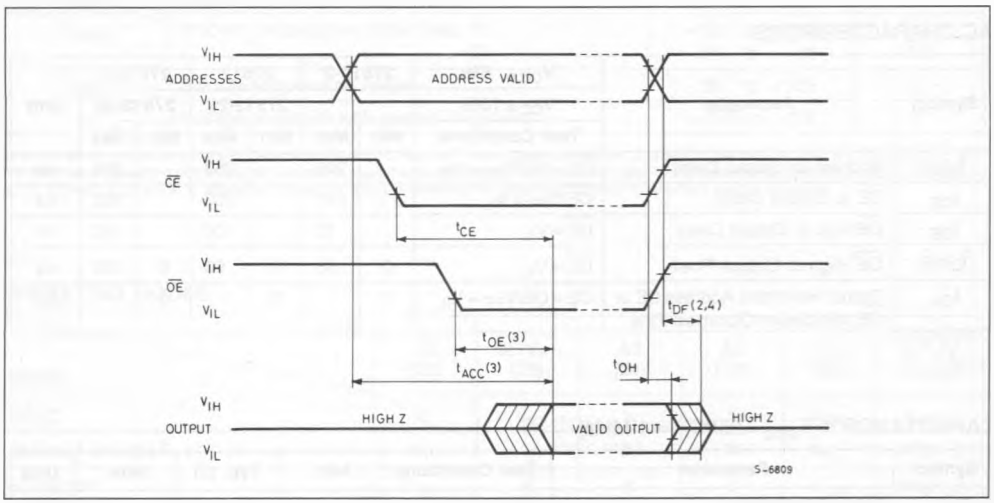
AC TESTING INPUT/OUTPUT WAVEFORM



AC TESTING LOAD CIRCUIT



AC WAVEFORMS



Notes: 1. Typical values are for T_{amb} = 25°C and nominal supply voltage.
2. This parameter is only sampled and not 100% tested.
3. $\overline{OE}/V_{PP}$ may be delayed up to t_{CE} - t_{OE} after the falling edge $\overline{CE}$ without impact on t_{CE}.
4. t_{DF} is specified from $\overline{OE}/V_{PP}$ or $\overline{CE}$ whichever occurs first.

DEVICE OPERATION

The six modes of operations of the M27512 are listed in the Operating Modes. A single 5V power supply is required in the read mode. All inputs are TTL levels except for $\overline{OE}/V_{PP}$ and 12V on A9 for Electronic Signature.

READ MODE

The M27512 has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}/V_{PP}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, the address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs after delay of t_{OE} from the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least t_{ACC}-t_{OE}.

STANDBY MODE

The M27512 has a standby mode which reduces the maximum active power current from 125 mA to 40 mA. The M27512 is placed in the standby mode by applying a TTL high signal to the $\overline{CE}$ input. When in the standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}/V_{PP}$ input.

TWO LINE OUTPUT CONTROL

Because EPROMs are usually used in larger memory arrays, the product features a 2 line control function which accommodates the use of multiple memory connection. The two line control function allows:

a) the lowest possible memory power dissipation
b) complete assurance that output bus contention will not occur.

For the most efficient use of these two control lines, $\overline{CE}$ should be decoded and used as the primary device selecting function, while $\overline{OE}/V_{PP}$ should be made a common connection to all devices in the array and connected to the $\overline{READ}$ line from the system control bus. This assures that all deselected memory devices are in their low power standby mode and that the output pins are only active when data is desired from a particular memory device.

SYSTEM CONSIDERATIONS

The power switching characteristics of NMOS-E3 EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer: the standby current level, the active current level, and transient current peaks that are produced by the falling and rising edges of $\overline{CE}$. The magnitude of this transient current peaks is dependent on the output capacitive and inductive loading of the device. The associated transient voltage peaks can be suppressed by complying with the two line output control and by properly selected decoupling capacitors. It is recommended that a 1 μF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor of low inherent inductance and should be placed as close to the device as possible. In addition, a 4.7 μF bulk electrolytic capacitor should be used between V_{CC} and GND for every eight devices. The bulk capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of PCB traces.

PROGRAMMING

Caution: exceeding 14V on pin 22 ($\overline{OE}/V_{PP}$) will permanently damage the M27512.

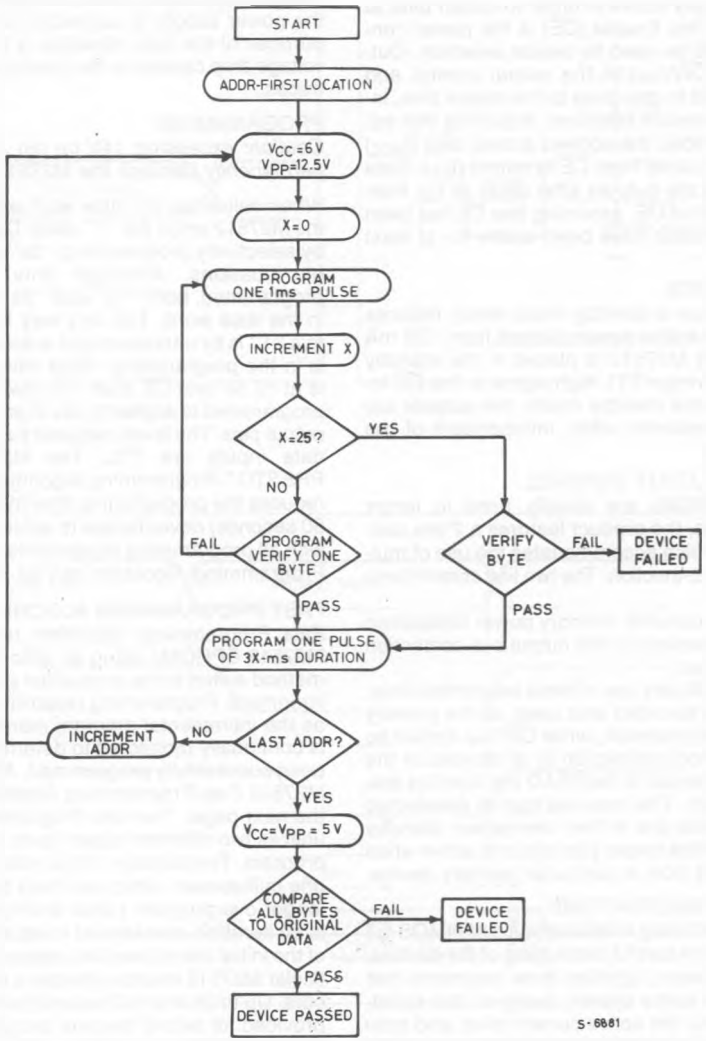
When delivered, and after each erasure, all bits of the M27512 are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be present in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure. The M27512 is in the programming mode when $\overline{OE}/V_{PP}$ input is at 12.5V and $\overline{CE}$ is at TTL-low. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL. The M27512 can use PRESTO* Programming Algorithm that drasticaly reduces the programming time (typically less than 50 seconds) nevertheless to achieve compatibility with all programming equipments, standard FAST Programming Algorithm can be used as well.

FAST PROGRAMMING ALGORITHM

Fast Programming Algorithm rapidly programs M27512 EPROMs using an efficient and reliable method suited to the production programming environment. Programming reliability is also ensured as the incremental program margin of each byte is continually monitored to determine when it has been successfully programmed. A flowchart of the M27512 Fast Programming Algorithm is shown in the next page. The Fast Programming Algorithm utilizes two different pulse types: initial and over-program. The duration of the initial $\overline{CE}$ pulse (s) is one millisecond, which will then be followed by a longer overprogram pulse of length 3X msec. (X is an iteration counter and is equal to the number of the initial one millisecond pulses applied to a particular M27512 location), before a correct verify occurs. Up to 25 one-millisecond pulses per byte are provided for before the over program pulse is applied. The entire sequence of program pulses is performed at V_{CC} = 6V and $\overline{OE}/V_{PP}$ = 12.5V (byte verifications at V_{CC} = 6V and $\overline{OE}/V_{PP}$ = V_{IL}). When the Fast Programming cycle has been completed, all bytes should be compared to the original data with V_{CC} = 5V.

DEVICE OPERATIONS (Continued)

FAST PROGRAMMING ALGORITHM FLOW CHART



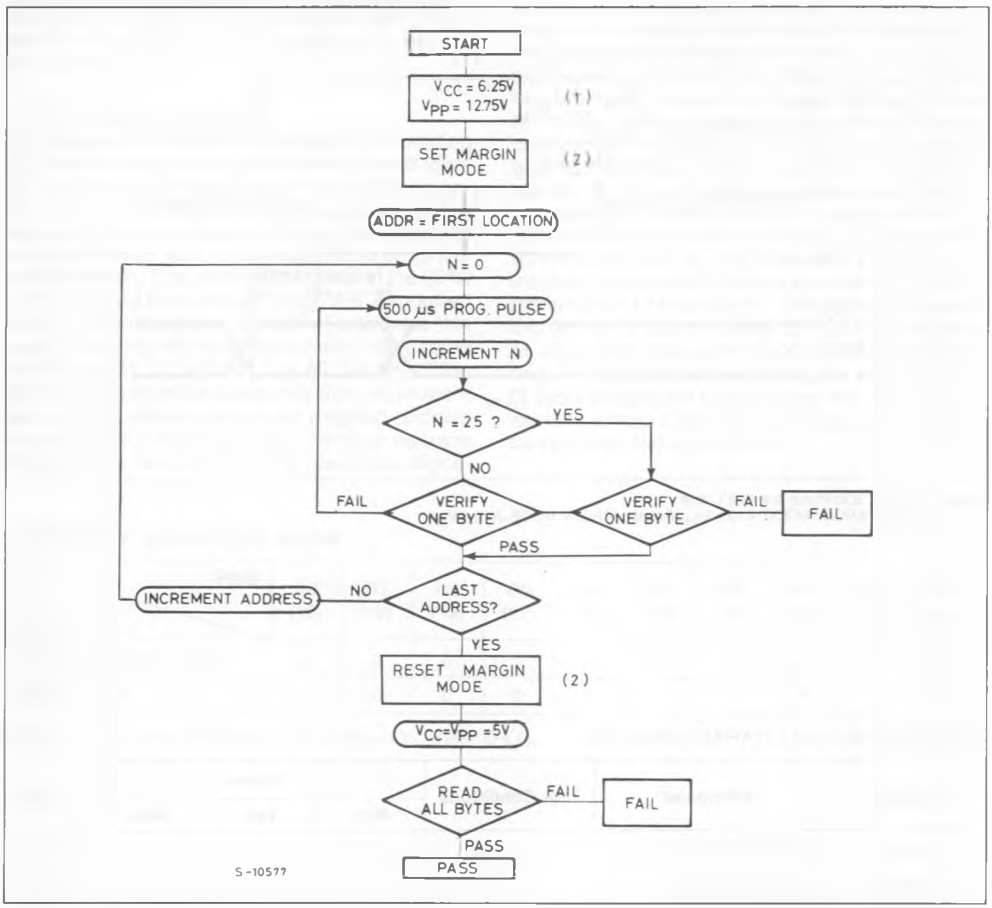
DEVICE OPERATION (Continued)

PRESTO PROGRAMMING ALGORITHM

PRESTO Programming Algorithm allows to programm the whole array with a guaranteed margin, in a typical time of less than 50 seconds (to be compared with 283 seconds for the Fast algorithm). This can be achieved with SGS-THOMSON M27512 due to several design innovations described in next paragraph to improve programming efficiency and to bring adequate margin for reliability. Before starting the programming the internal MARGIN MODE* circuit is set in order to guarantee that each cell is programmed with enough margin. Then a sequence of 500 microseconds program pulses are applied to each byte until a correct verify occurs. No overprogram pulses are applied since the verify in MARGIN MODE provides the necessary margin to each programmed cell. PRESTO programming algorithm is supported on the full line of DATA I/O programmers,for the most popular production equipments the firmware revision are:

- Series 1000: revision V08.1
- Mode 120 A and 121A: revision V14.1

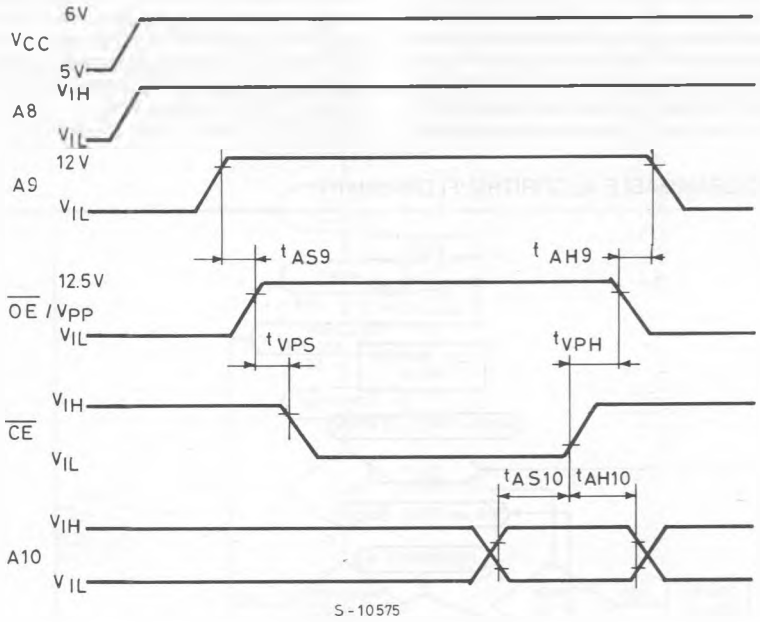
PRESTO PROGRAMMABLE ALGORITHM FLOW CHART



Notes: 1. V_{CC} must be mantained at 6V during the whole programming algorithm between set and reset MARGIN MODE operations. A drop of V_{CC} below 4V could reset the internal MARGIN MODE flip-flop giving place to insufficient programming margins.
2. See MARGIN MODE set and reset waveforms.

DEVICE OPERATION (Continued)

MARGIN MODE SET AND RESET WAVEFORMS



Notes: 1. Other addresses are don't care
2. Set MARGIN MODE A10 = V_{IH}, Reset MARGIN MODE A10 = V_{IL}

MARGIN MODE AC CHARACTERISTICS

Symbol	Parameter	Test Conditions	Values			Unit
			Min.	Typ.	Max.	
t_{AS10}	A10 Set Up Time		1			µs
t_{AH10}	A10 Hold Time		1			µs
t_{VPH}	V_{PP} Hold Time		2			µs
t_{VPS}	V_{PP} Set Up Time		2			µs
t_{AS9}	A9 Set up Time		2			µs
t_{AH9}	A9 Hold Time		2			µs

DEVICES OPERATION (Continued)

PROGRAM INHIBIT

Programming of multiple M27512s in parallel with different data is also easily accomplished. Except for $\overline{CE}$, all like inputs (including $\overline{OE}/V_{PP}$) of the parallel M27512 may be common. A TTL low level pulse applied to a M27512's $\overline{CE}$ input, with $\overline{OE}/V_{PP}$ at 12.5V, will program that M27512. A high level $\overline{CE}$ input inhibits the other M27512s from being programmed.

PROGRAM VERIFY

A verify (read) should be performed on the programmed bits to determine that they were correctly programmed. The verify is accomplished with $\overline{OE}/V_{PP}$ and $\overline{CE}$ at V_{IL}. Data should be verified t_{DV} after the falling edge of $\overline{CE}$.

ELECTRONIC SIGNATURE

The Electronic Signature mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ±5°C ambient temperature range that is required when programming the M27512. To activate this mode, the programming equipment must force 11.5V to 12.5V on address line A9 (pin 24) of the M27512. Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 (pin 10) from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during Electronic Signature mode, except for A14 and A15 which should be held high. Byte 0 ($A0 = V_{IL}$) represents the manufacturer code and byte 1 ($A0 = V_{IH}$) the device identifier code. For the SGS M27512, these two identifier bytes are given here below. All identifiers for manufacturer and device codes will possess odd parity, with the MSB (07) defined as the parity bit.

ERASURE OPERATION

The erasure characteristic of the M27512 is such that erasure begins when the cells are exposed to light with wavelengths shorter than approximately 4000 Angstrom Å. It should be noted that sunlight and some type of fluorescent lamps have wavelengths in the 3000-4000 A range. Data shows that constant exposure to room level fluorescent lighting could erase a typical M27512 in about 3 years, while it would take approximately 1 week to cause erasure when expose to direct sunlight. If the M27512 is to be exposed to these types of lighting conditions for extended periods of time, it is suggested that opaque labels be put over the M27512 window to prevent unintentional erasure. The recommended erasure procedure for the M27512 is exposure to short wave ultraviolet light which has wavelength 2537 Å. The integrated dose (i.e. UV intensity x exposure time) for erasure should be a minimum of 15 W-sec/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with 12000 uW/cm^2 power rating. The M27512 should be placed within 2.5 cm (1 inch) of the lamp tubes during the erasure. Some lamps have a filter on their tubes which should be removed before erasure.

ELECTRONIC SIGNATURE MODE

PINS / IDENTIFIER	A0 (10)	O7 (19)	O6 (18)	O5 (17)	O4 (16)	O3 (15)	O2 (13)	O1 (12)	O0 (11)	Hex Data
MANUFACTURER CODE	V_{IL}	0	0	1	0	0	0	0	0	20
DEVICE CODE	V_{IH}	0	0	0	0	1	1	0	1	0D

Note: A9 = 12V ±0.5V; A1-A8, A10-A13, $\overline{CE}$, $\overline{OE}/V_{PP} = V_{IL}$; A14, A15 = V_{IH}

PROGRAMMING OPERATION (T_{amb} = 25°C ±5°C, V_{CC}(1) = 6V ±0.25V, $\overline{OE}/V_{PP}$(1) = 12.5V ±0.5V)

DC AND OPERATING CHARACTERISTIC:

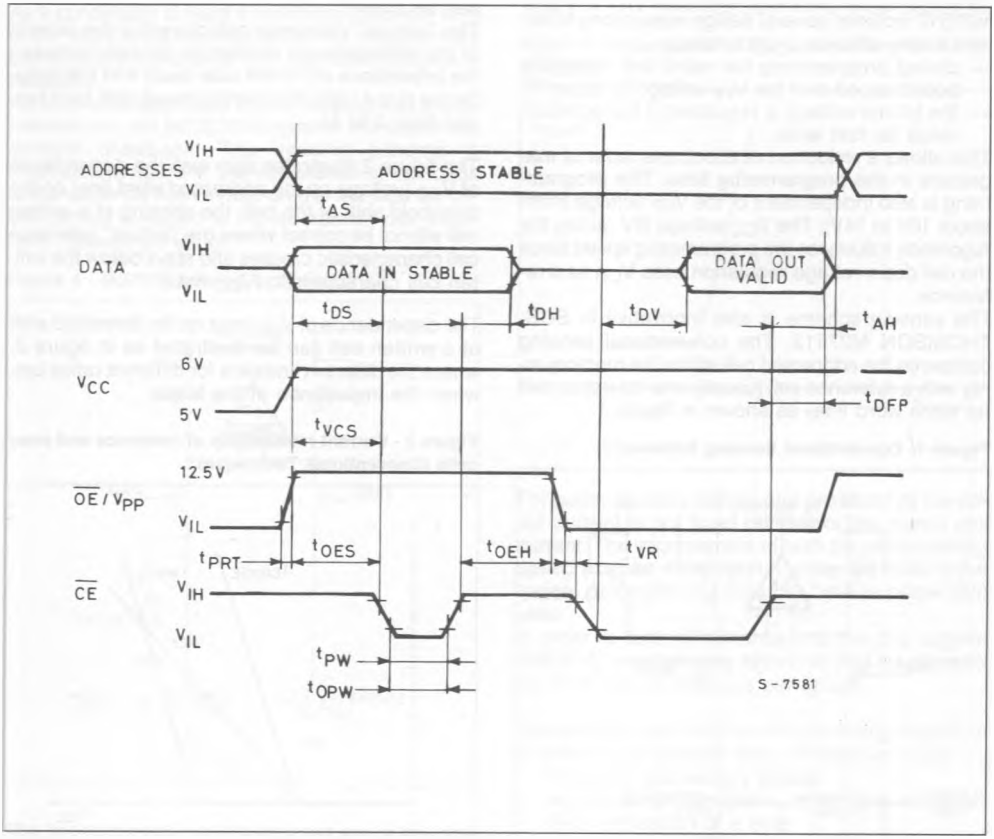
Symbol	Parameter	Test Conditions (See note 1)	Values			Unit
			Min.	Typ.	Max.	
I_{LI}	Input Current (All Inputs)	$V_{IN} = V_{IL}$ or V_{IH}			10	µA
V_{IL}	Input Low Level (All Inputs)		−0.1		0.8	V
V_{IH}	Input High Level		2.0		V_{CC}+1	V
V_{OL}	Output Low Voltage During Verify	I_{OL} = 2.1 mA			0.45	V
V_{OH}	Output High Voltage During Verify	I_{OH} = −400 µA	2.4			V
I_{CC2}	V_{CC} Supply Current				150	mA
I_{PP2}	V_{PP} Supply Current (Program)	$\overline{CE} = V_{IL}$			50	mA
V_{ID}	A9 Electronic Signature Voltage		11.5		12.5	V

AC CHARACTERISTICS

Symbol	Parameter	Test Conditions (See note 1)	Values			Unit
			Min.	Typ.	Max.	
t_{AS}	Address Setup Time		2			µs
t_{OES}	$\overline{OE}/V_{PP}$ Setup Time		2			µs
t_{OEH}	$\overline{OE}/V_{PP}$ Hold Time		2			µs
t_{DS}	Data Setup Time		2			µs
t_{AH}	Address Hold Time		0			µs
t_{DH}	Data Hold Time		2			µs
t_{DFP}(4)	Output Enable Output Float Delay		0		130	ns
t_{VCS}	V_{CC} Setup Time		0			µs
t_{PW}(3)	$\overline{CE}$ Initial Program Pulse Width		0.95	1.0	1.05	ms
t_{OPW}(2)	$\overline{CE}$ Overprogram Pulse Width		2.85		78.75	ms
t_{DV}	Data Valid from $\overline{CE}$				1	ns
t_{VR}	$\overline{OE}/V_{PP}$ Recovery Time		2			µs
t_{PRT}	$\overline{OE}/V_{PP}$ Pulse Rise Time During Programming		50			ns

Notes:
1. V_{CC} must be applied simultaneously or before $\overline{OE}/V_{PP}$ and removed simultaneously or after $\overline{OE}/V_{PP}$.
2. The length of the overprogram pulse may vary from 2.85msec to 78.75msec as a function of the iteration counter value X.
3. Initial Program Pulse width tolerance is 1msec ±5%.
4. This parameter is only sampled and not 100% tested.
   Output Float is defined as the point where data is no longer driven (see timing diagram).

PROGRAMMING WAVEFORMS



Notes: 1. The input timing reference level is 0.8V for a V_{IL} and 2V for a V_{IH}.

2. t_{OE} and t_{DFP} are characteristics of the device but must be accommodated by the programmer.

M27512 DESIGN INNOVATIONS FOR AN EFFICIENT PROGRAMMING PRESTO

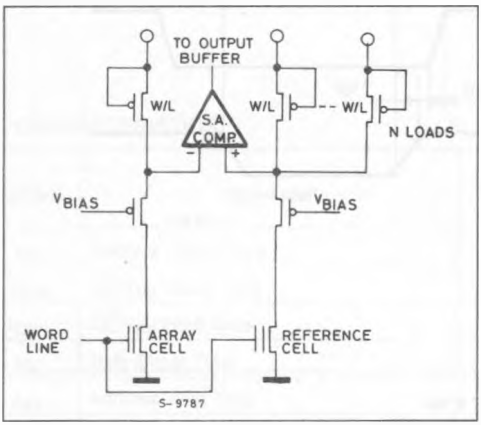
M27512 includes several design innovations to obtain a very efficient programming:

— during programming the word line voltage is bootstrapped over the V_{PP} voltage by about 2V
— the bit line voltage is regulated at the optimum value for fast write.

This allows a reduction of about one order of magnitude in the programming time. The programming is also independent of the V_{PP} voltage (from about 10V to 14V). The V_{CC} voltage (6V during the Algorithm) influences the programming speed since the cell drain voltage regulation uses V_{CC} as a reference.

The sensing scheme is also innovative in SGS-THOMSON M27512. The conventional sensing compares the addressed cell within the memory array with a reference cell (usually one reference cell for each word line) as shown in figure 1.

Figure 1. Conventional Sensing Schematic



If the addressed cell is erased its current is the same as the reference cell's current and the imbalance at the inputs of the comparator (higher voltage on right side = 1) is obtained by connecting lower impedence load on the right side than on the left.

If the addressed cell is written (no current) the left input to the comparator will have a higher voltage than the right side (0 state).

The above approach has proven to be efficient and reliable but still shows a drawback that is the dependance of the V_{CC} operating range (at high V_{CC}) on the threshold shift of the written cell. This can be easily understood by looking at the cell transcharacteristics diagram: together with the characteristics of the erased and the written cell in the memory array the "virtual" reference cell current can be drawn.

The "virtual" reference cell current is the current of the reference cell divided by the ratio between the impedence of the left side loads and the impedence of the right side loads (usually the ratio ranges from 2 to 5).

The figure 2 illustrates very well the dependance of V_{CC} (voltage on the addressed word line) on the threshold shift of the cell: the sensing of a written cell will not be correct where the "virtual" reference cell characteristic crosses and stays below the written cell characteristic (V_{CC} max).

The dependance of V_{CC} max on the threshold shift of a written cell can be illustrated as in figura 3, where the different lines are for different ratios between the impedance of the loads.

Figure 2 - Current relationship of reference and array cells (Conventional Technique)

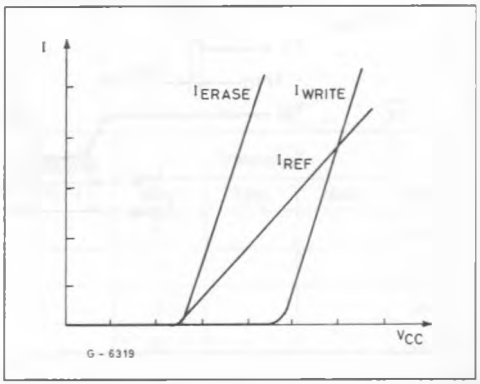
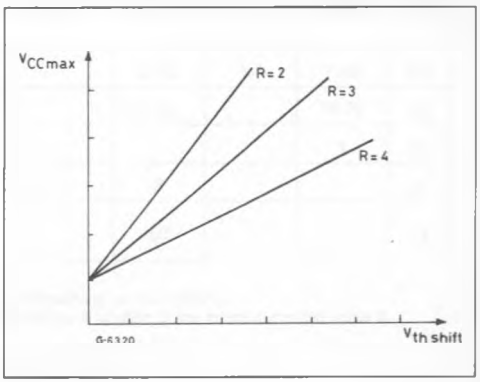


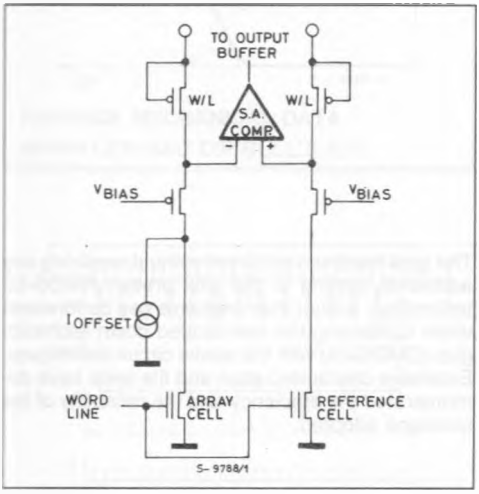
Figure 3 - Dependance of V_{CC} max on threshold shift (R = Loads impedance ratios) (conventional techniques)



M27512 DESIGN INNOVATIONS FOR AN EFFICIENT PROGRAMMING PRESTO (Continued)

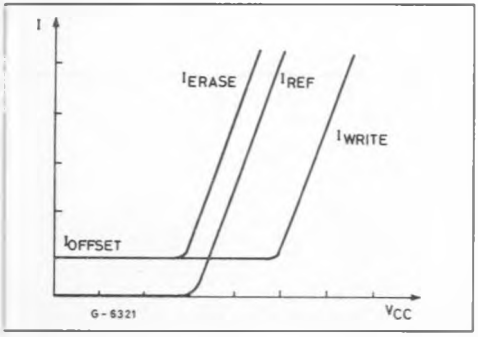
As a conclusion at least a minimum threshold shift of 2V to 3V must be required to the programmed cell to guarantee a wide V_{CC} operation range and reliability.
An innovative approach for the sensing was implemented into the M27512 to remove the above described drawback. The sensing scheme is illustrated in figure 4: the impedance of the loads is the same on both sides; on the left side an offset current is added to the addressed cell's current - (patent pending).

Figure 4 - M27512 sensing schematic



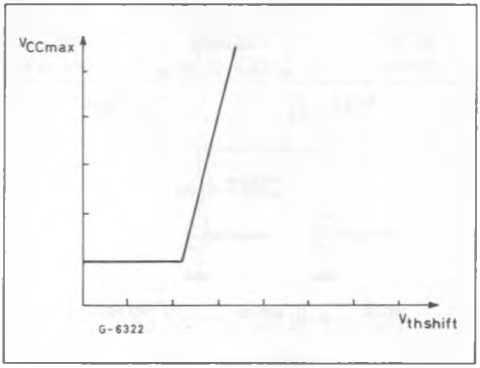
The improvement is easily pointed out in the diagram of the cell transcharacteristics (figure 5) the difference in slope between the written cell and the reference cell are drastically reduced.

Figure 5 - Current relemention ship of reference and array cells (New Technique)



The final result is that a threshold shift of about 1V for a written cell is enough to allow a proper sensing in a very wide V_{CC} operating range (figure 6).

Figure 6 - Dependance of V_{CC} max on threshold Shift (M27512)



For better process margin and producibility the offset current is not fixed but tracks the matrix cell current. The improvement of both the programming speed and the sensing efficiency will reduce the typical programming time per byte to below 200 μsec.
In order to take full advantage of this the original PRESTO programming algorithm was developped as illustrated in previous paragraph.

The similarity with the Fast Programming Algorithm is evident but several main differences exist:
— 500 μsec elementary pulses
— no overprogram pulses are applied after correct verification of a byte
— the existence of a sufficient margin for the written cells is guaranteed by making the program verify in a special test mode called MARGIN MODE*...

Reading a cell in MARGIN MODE requires to the written cell a threshold shift of about 2V: 1V margin above the threshold shift required for a correct operation with wide V_{CC} range in normal operating modes. The circuit arrangement that allows to guarantee the margin is illustrated in figure 7.
The result in the transcharacteristic plane helps to understand the MARGIN MODE feature (figure 8).
The threshold shift margin has been carefully tuned in order to guarantee that the V_{CC} operating range and the access time performance would not be reduced by a cell marginally written; taking into account the temperature range, noise conditions, and data retention (intrinsic charge loss).
The MARGIN MODE is set before starting the programming algorithm and reset after the completion.

Figure 7 - M27512 Sensing schematic with activated margin mode

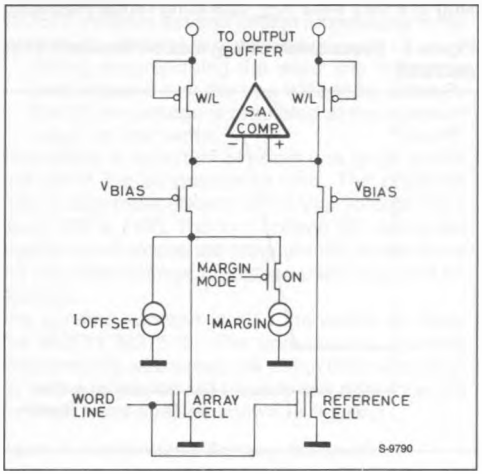
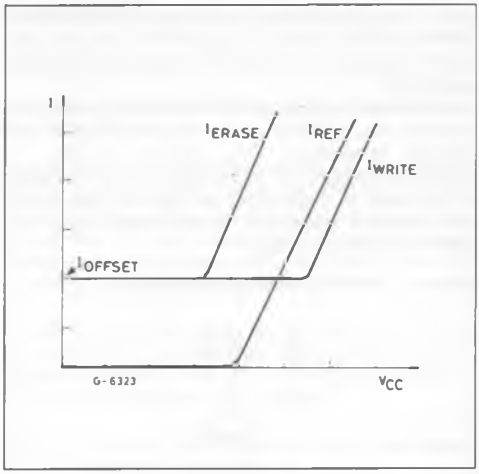


Figure 8 - Current relationship of reference and array cells with margin mode activated



CONCLUSION

M27512 has succesfully achieved the goal of drastically reducing the programming time by:

— improving the programming efficiency
— implementing an improved sensing scheme
— guaranteing by an innovative hardware approach an adequate margin for reliability

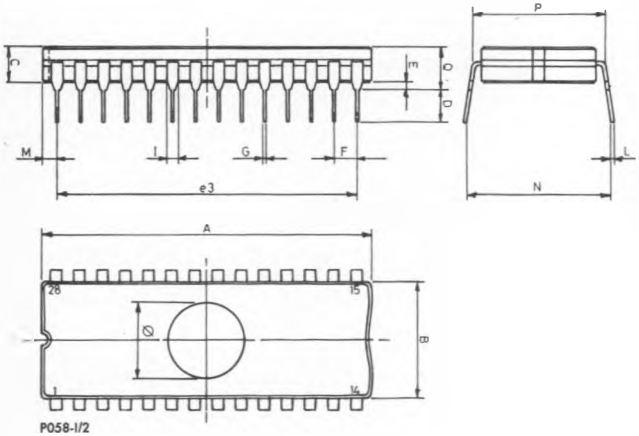
The goal has been achieved without requiring any additional scaling to the well proven NMOS-E3 technology: further improvements can be foreseen when combining the new scaled down technologies (CMOS-E4) with the above circuit techniques. Extensive characterization and life tests have demonstrated the efficiency and the reliability of the solutions adopted.

ORDERING INFORMATION

Part Number	Access Time	Supply Voltage	Temp. Range	Package
M27512-2F1	200 ns	5V ± 5%	0 to +70°C	DIP-28
M27512F1	250 ns	5V ± 5%	0 to +70°C	DIP-28
M27512-3F1	300 ns	5V ± 5%	0 to +70°C	DIP-28
M27512-25F1	250 ns	5V ± 10%	0 to +70°C	DIP-28
M27512-30F1	300 ns	5V ± 10%	0 to +70°C	DIP-28
M27512F6	250 ns	5V ± 5%	−40 to +85°C	DIP-28

PACKAGE MECHANICAL DATA

28-PIN CERAMIC DIP BULL'S EYE



P058-I/2

Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A			38.10			1.500
B	14.50		14.90	0.571		0.587
C	3.90		5.08	0.154		0.200
D	3.00			0.118		
E	0.50		1.78	0.020		0.070
e 3		33.02			1.300	
F	2.29		2.79	0.090		0.110
G	0.40		0.55	0.016		0.022
I	1.17		1.42	0.046		0.056
L	0.22		0.31	0.009		0.012
M	1.52		2.49	0.060		0.098
N	16.51		18.00	0.650		0.709
P	15.40		15.80	0.606		0.622
Q			5.71			0.225
Ø	8.64		9.14	0.340		0.360