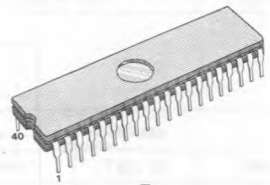
SGS-THOMSON MICROELECTRONICS

M27C1024

1024K (64K x 16) CMOS UV ERASABLE PROM

PRELIMINARY DATA

- FAST ACCESS TIME:
  120ns MAX M27C1024-12XF1/M27C1024-12F1
  150ns MAX M27C1024-15XF1/M27C1024-15F1/ M27C1024-15XF6
  200ns MAX M27C1024-20XF1/M27C1024-20F1/ M27C1024-20XF6
  250ns MAX M27C1024-25XF1/M27C1024-25F1/ M27C1024-25XF6
- 0 TO +70°C STANDARD TEMPERATURE RANGE
- SINGLE +5V POWER SUPPLY
- LOW STANDBY CURRENT (1mA MAX)
- TTL PROGRAMMING
- VERY FAST AND RELIABLE PROGRAMMING ALGORITHM
- ELECTRONIC SIGNATURE



F
DIP-40
(Ceramic Bull's Eye)

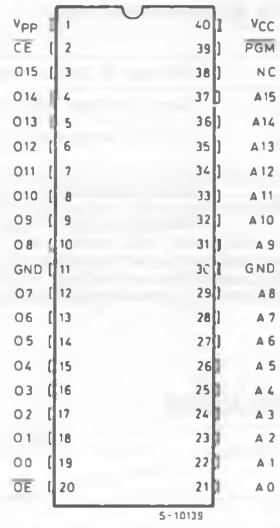
(Ordering Information at the end of the datasheet)

DESCRIPTION

The M27C1024 is a 1,048,576-bit ultraviolet erasable and electrically programmable read only memory (EPROM). It is organized as 65,536 words by 16 bits and manufactured using SGS-THOMSON' CMOS-E4 process. The M27C1024 with its single +5V power supply and with an access time of 120ns, is ideal for use in 16 bit microprocessor system allowing full speed operation without WAIT states. In high performance CPU's (10MHz), the M27C1024 has an important feature which is to separate the output control, Output Enable ($\overline{OE}$) from the Chip Enable control ($\overline{CE}$). The $\overline{OE}$ control eliminates bus contention in multiple bus microprocessor systems. The M27C1024 also features a standby mode which reduces the power dissipation without increasing access time. The active current is 50mA while the maximum standby current is only 1 mA. The standby mode is achieved by applying a TTL-high signal to the $\overline{CE}$ input. The M27C1024 enables implementation of new, advanced systems with firmware intensive architectures.

The combination of the M27C1024s high density, and new advanced microprocessors having megabit addressing capability provides designers with opportunities to engineer user-friendly, high reliability, high-performance systems. The M27C1024 large storage capability enables it to function as a high density software carrier. The M27C1024 has an "Electronic Signature" that allows programmers to automatically identify device type and pinout.

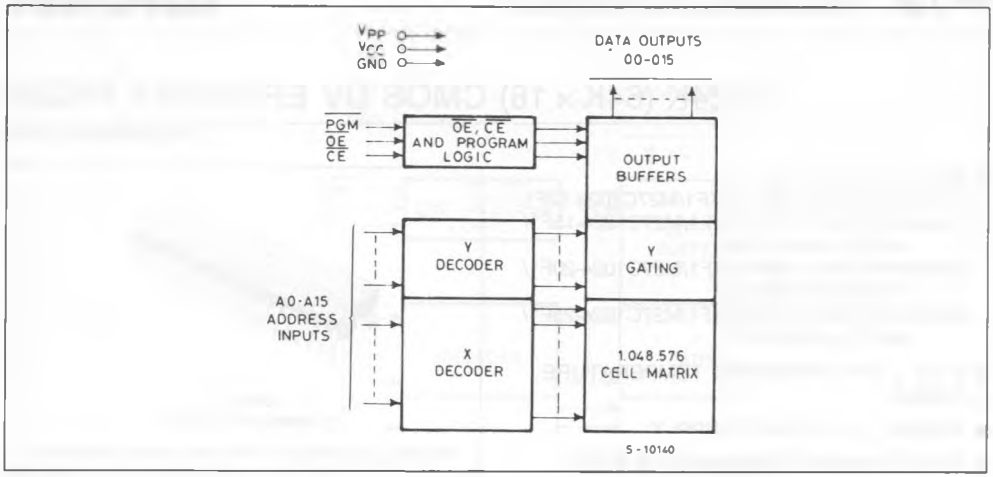
PIN CONNECTIONS



PIN NAMES

A0-A15	ADDRESS INPUT
$\overline{CE}$	CHIP ENABLE INPUT
$\overline{OE}$	OUTPUT ENABLE
$\overline{PGM}$	PROGRAM
O0-O15	DATA INPUT/OUTPUT
NC	NON CONNECTED

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_I	All Input or Output voltages with respect to ground	+ 6.5 to − 0.6	V
V_{PP}	Supply voltage with respect to ground	+14 to − 0.6	V
T_{amb}	Ambient temperature under bias /F1 /F6	−10 to +80 −50 to +95	°C °C
T_{stg}	Storage temperature range	−65 to +125	°C
	Voltage on pin 31 with respect to ground	+13.5 to −0.6	V

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING MODES

MODE \ PINS	$\overline{CE}$ (2)	$\overline{OE}$ (20)	A9 (31)	$\overline{PGM}$ (39)	V_{PP} (1)	OUTPUTS
READ	L	L	X	H	V_{CC}	D_{OUT}
OUTPUT DISABLE	L	H	X	H	V_{CC}	HIGH Z
STANDBY	H	X	X	X	V_{CC}	HIGH Z
PROGRAM	L	X	X	L	V_{PP}	D_{IN}
PROGRAM VERIFY	L	L	X	H	V_{PP}	D_{OUT}
PROGRAM INHIBIT	H	X	X	X	V_{PP}	HIGH Z
ELECTRONIC SIGNATURE	L	L	V_H	H	V_{CC}	CODE

NOTE: X = DON'T CARE; V_H = 12V ±0.5V; H = HIGH; L = LOW

READ OPERATION

DC AND AC CONDITIONS

Selection Code	–12XF1/–15XF1 –20XF1/–25XF1	–12F1/–15F1 –20F1/–25F1	–15XF6/–20XF6 –25XF6
Operating Temperature Range	0 to 70°C	0 to 70°C	–40 to 85°C
V_{CC} Power Supply (1,2)	5V ±5%	5V ±10%	5V ±5%
V_{PP} Voltage (2)	$V_{PP} = V_{CC}$	$V_{PP} = V_{CC}$	$V_{PP} = V_{CC}$

DC AND OPERATING CHARACTERISTICS

Symbol	Parameter	Test Conditions	Values			Unit
			Min.	Typ. (2)	Max.	
I_{LI}	Input Load Current	$V_{IN} = 5.5V$			10	µA
I_{LO}	Output Leakage Current	$V_{OUT} = 5.5V$			10	µA
I_{CC1}	V_{CC} Current Standby	$\overline{CE} = V_{IH}$			1	mA
I_{CC2}	V_{CC} Current Active	$\overline{CE} = \overline{OE} = V_{IL}$ @f = 8MHz		20	50	mA
V_{IL}	Input Low Voltage		–0.1		+0.8	V
V_{IH}	Input High Voltage		2.0		V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	$I_{OL} = 2.1$ mA			0.45	V
V_{OH}	Output High Voltage	$I_{OH} = -400$ µA	2.4			V

AC CHARACTERISTICS

Symbol	Parameter	$V_{CC} \pm 10\%$ $V_{CC} \pm 5\%$	27C1024-12/ 27C1024-12X		27C1024-15/ 27C1024-15X		27C1024-20/ 27C1024-20X		27C1024-25/ 27C1024-25X		Unit
		Test Condition	Min	Max	Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay	$\overline{CE} = \overline{OE} = V_{IL}$		120		150		200		250	ns
t_{CE}	$\overline{CE}$ to Output Delay	$\overline{OE} = V_{IL}$		120		150		200		250	ns
t_{OE}	$\overline{OE}$ to Output Delay	$\overline{CE} = V_{IL}$		60		60		75		75	ns
$t_{DF(3)}$	$\overline{OE}$High to Output Float	$\overline{CE} = V_{IL}$	0	60	0	60	0	90	0	90	ns
t_{OH}	Output Hold from Address $\overline{CE}$ or $\overline{OE}$ Whichever Occurred First	$\overline{CE} = \overline{OE} = V_{IL}$	0		0		0		0		ns

CAPACITANCE(4) (T_{amb} = 25°C, f = 1 MHz)

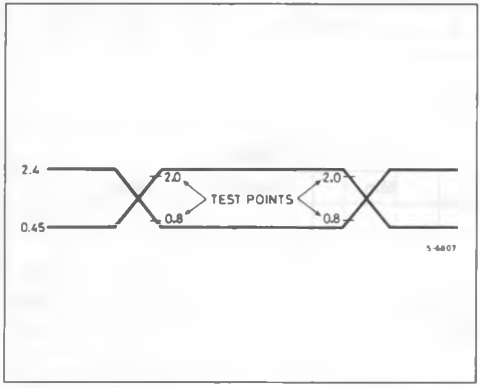
Symbol	Parameter	Test Conditions	Min.	Typ. (2)	Max.	Unit
C_{IN}	Input Capacitance	$V_{IN} = 0V$		4	6	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0V$		8	12	pF

Notes: 1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. Typical values are for T_{amb} = 25°C and nominal supply voltages.
3. This parameter is only sampled and not 100% tested. Output Float is defined as the point where data is no longer driven-see timing diagram.
4. This parameter is only sampled and not 100% tested.

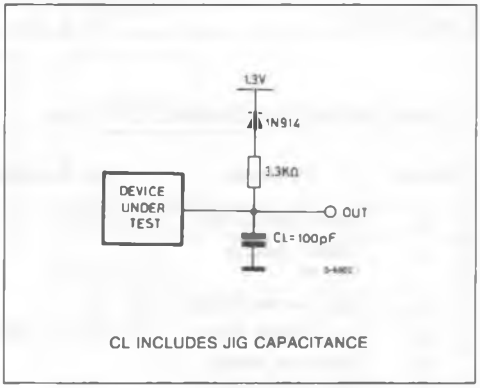
AC TEST CONDITIONS

Output Load: 100pF + 1TTL Gate
Input Rise and Fall Times: ≤ 20ns
Input Pulse Levels: 0.45 to 2.4V
Timing Measurement Reference Levels: Inputs 0.8 and 2V
Outputs 0.8 and 2V

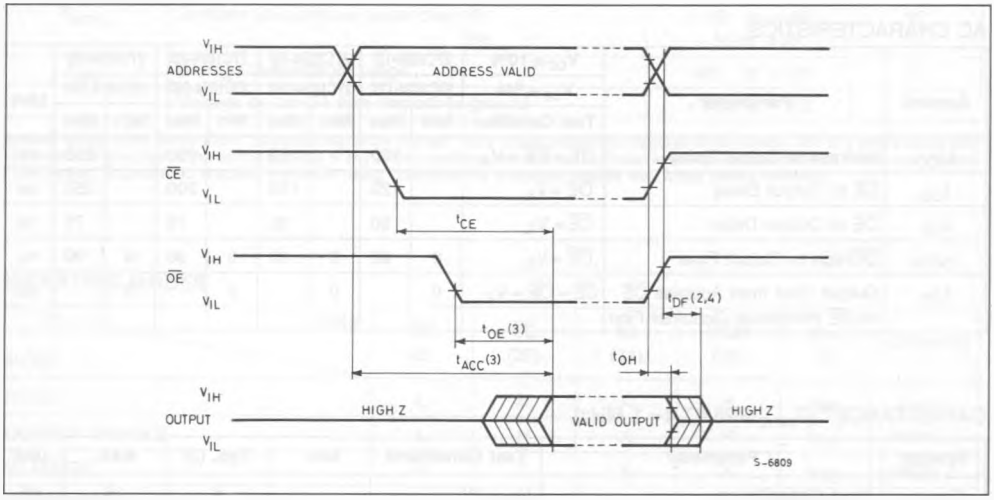
AC TESTING INPUT/OUTPUT WAVEFORM



AC TESTING LOAD CIRCUIT



AC WAVEFORMS



Notes: 1. Typical values are for T_{amb} = 25°C and nominal supply voltage.
2. This parameter is only sampled and not 100% tested.
3. $\overline{OE}$ may be delayed up to $t_{CE} - t_{OE}$ after the falling edge $\overline{CE}$ without impact on t_{CE}.
4. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first.

DEVICE OPERATION

The modes of operations of the M27C1024 are listed in the Operating Modes. A single 5V power supply is required in the read mode. All inputs are TTL levels except for 12V on A9 for Electronic Signature.

READ MODE

The M27C1024 has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, the address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs after delay at t_{OE} from the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least t_{ACC}-t_{OE}.

STANDBY MODE

The M27C1024 has a standby mode which reduces the maximum active power current from 50 mA to 1 mA. The M27C1024 is placed in the standby mode by applying a TTL high signal to the $\overline{CE}$ input. When in the standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

TWO LINE OUTPUT CONTROL

Because EPROMs are usually used in larger memory arrays, the product features a 2 line control function which accommodates the use of multiple memory connection. The two line control function allows:

a) the lowest possible memory power dissipation
b) complete assurance that output bus contention will not occur.

For the most efficient use of these two control lines, $\overline{CE}$ should be decoded and used as the primary device selecting function, while $\overline{OE}$ should be made a common connection to all devices in the array and connected to the $\overline{READ}$ line from the system control bus. This assures that all deselected memory devices are in their low power standby mode and that the output pins are only active when data is desired from a particular memory device.

SYSTEM CONSIDERATIONS

The power switching characteristics of CMOS-E4 EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer: the standby current level, the active current level, and transient current peaks that are produced by the falling and rising edges of $\overline{CE}$. The magnitude of this transient current peaks is dependent on the output capacitive and inductive loading of the device. The associated transient voltage peaks can be suppressed by complying with the two line output control and by properly selected decoupling capacitors. It is recommended that a 1 μF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor of low inherent inductance and should be placed as close to the device as possible. In addition, a 4.7 μF bulk electrolytic capacitors should be used between V_{CC} and GND for every eight devices. The bulk capacitor should be located near where the power supply is connected to the array.
The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of PCB traces.

PROGRAMMING

Caution: exceeding 14V on V_{PP} pin will permanently damage the M27C1024.

When delivered, and after each erasure, all bits of the M27C1024 are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be present in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure. The M27C1024 is in the programming mode when V_{PP} input is at 12.5V and $\overline{CE}$ and $\overline{PGM}$ are at TTL-low. The data to be programmed is applied 16 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL. V_{CC} is specified to be 6.25V ± 0.25V.

VERY FAST AND RELIABLE PROGRAMMING ALGORITHM = PRESTO II

PRESTO II programming algorithm, available for the M27C1024 is an enhancement of the PRESTO algorithm used for the M27512.
During programming and verify operation a MARGIN MODE™ Circuit is automatically activated. It provides adequate margin on threshold voltage of programmed cells, thus writing margin is independent from V_{CC} in verify mode and over program pulse is not necessary, reducing programming time down to a theoretical value of 6 seconds.

PROGRAM INHIBIT

Programming of multiple M27C1024s in parallel with different data is also easily accomplished. Except for $\overline{CE}$, all like inputs of the parallel M27C1024 may be common. A TTL low level pulse applied to a M27C1024's $\overline{CE}$ input, with V_{PP} at 12.5V, will program that M27C1024. A high level $\overline{CE}$ input inhibits the other M27C1024s from being programmed. V_{CC} is specified to be 6.25V ± 0.25V.

PROGRAM VERIFY

A verify (read) should be performed on the programmed bits to determine that they were correctly programmed. The verify is accomplished with $\overline{OE}$ and $\overline{CE}$ at V_{IL}, $\overline{PGM}$ at V_{IH}, V_{PP} at 12.5V and V_{CC} at 6.25V ± 0.25V.

ELECTRONIC SIGNATURE

The Electronic Signature mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ± 5°C ambient temperature range that is required when programming the M27C1024. To activate this mode, the programming equipment must force 11.5V to 12.5V on address line A9 (pin 31) of the M27C1024. Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 (pin 21) from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during Electronic Signature mode, except for A14 and A15 which should be held high. Byte 0 (A0 = V_{IL}) represents the manufacturer code and byte 1 (A0 = V_{IH}) the device identifier code. For the SGS-THOMSON M27C1024, these two identifier bytes are given here below, and can be read-out on outputs O0 to O7 while outputs O_8 to O_{15} are don't care.

ERASURE OPERATION

The erasure characteristic of the M27C1024 is such that erasure begins when the cells are exposed to light with wavelengths shorter than approximately 4000 Angstrom Å. It should be noted that sunlight and some type of fluorescent lamps have wavelengths in the 3000-4000 A range. Data shows that constant exposure to room level fluorescent lighting could erase a typical M27C1024 in about 3 years, while it would take approximately 1 week to cause erasure when expose to direct sunlight. If the M27C1024 is to be exposed to these types of lighting conditions for extended periods of time, it is suggested that opaque labels be put over the M27C1024 window to prevent unintentional erasure. The recommended erasure procedure for the M27C1024 is exposure to short wave ultraviolet light which has wavelength 2537 Å. The integrated dose (i.e. UV intensity x exposure time) for erasure should be a minimum of 15 W-sec/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with 12000 uW/cm^2 power rating. The M27C1024 should be placed within 2.5 cm (1 inch) of the lamp tubes during the erasure. Some lamps have a filter on their tubes which should be removed before erasure.

ELECTRONIC SIGNATURE MODE

PINS / IDENTIFIER	A0 (21)	O7 (12)	O6 (13)	O5 (14)	O4 (15)	O3 (16)	O2 (17)	O1 (18)	O0 (19)	Hex Data
MANUFACTURER CODE	V_{IL}	0	0	1	0	0	0	0	0	20
DEVICE CODE	V_{IH}	1	0	0	0	1	1	0	0	8C

Note: A9 = 12V ±0.5V; A1-A8, A10-A13, $\overline{CE}$, $\overline{OE}$ = V_{IL}; A14, A15 = V_{IH}

PROGRAMMING OPERATION (T_{amb} = 25°C ±5°C, V_{CC}(1) = 6.25V ±0.25V, V_{PP}(1) = 12.5V ±0.5V)

DC AND OPERATING CHARACTERISTIC:

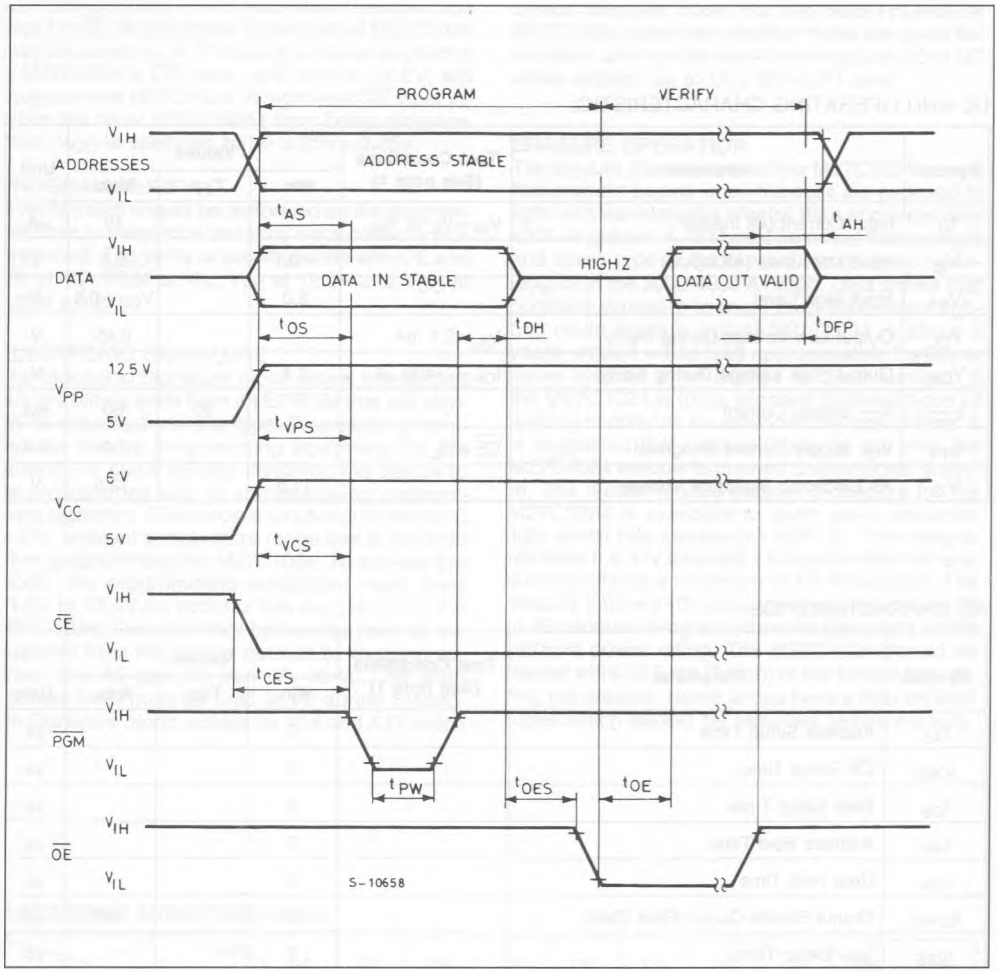
Symbol	Parameter	Test Conditions (See note 1)	Values			Unit
			Min.	Typ.	Max.	
I_{LI}	Input Current (All Inputs)	$V_{IN} = V_{IL}$ or V_{IH}			10	µA
V_{IL}	Input Low Level (All Inputs)		−0.1		0.8	V
V_{IH}	Input High Level		2.0		V_{CC} + 0.5	V
V_{OL}	Output Low Voltage During Verify	I_{OL} = 2.1 mA			0.45	V
V_{OH}	Output High Voltage During Verify	I_{OH} = −400 µA	2.4			V
I_{CC2}	V_{CC} Supply Current			20	50	mA
I_{PP2}	V_{PP} Supply Current (Program)	$\overline{CE} = V_{IL}$			50	mA
V_{ID}	A9 Electronic Signature Voltage		11.5		12.5	V

AC CHARACTERISTICS

Symbol	Parameter	Test Conditions (See note 1)	Values			Unit
			Min.	Typ.	Max.	
t_{AS}	Address Setup Time		2			µs
t_{OES}	$\overline{OE}$ Setup Time		2			µs
t_{DS}	Data Setup Time		2			µs
t_{AH}	Address Hold Time		0			µs
t_{DH}	Data Hold Time		2			µs
t_{DFP}(2)	Output Enable Output Float Delay		0		130	ns
t_{VPS}	V_{PP} Setup Time		2			µs
t_{VCS}	V_{CC} Setup Time		2			µs
t_{CES}	$\overline{CE}$ Setup Time		2			µs
t_{PW}	$\overline{PGM}$ Initial Program Pulse Width		95	100	105	µs
t_{OE}	Data Valid from $\overline{OE}$				100	ns

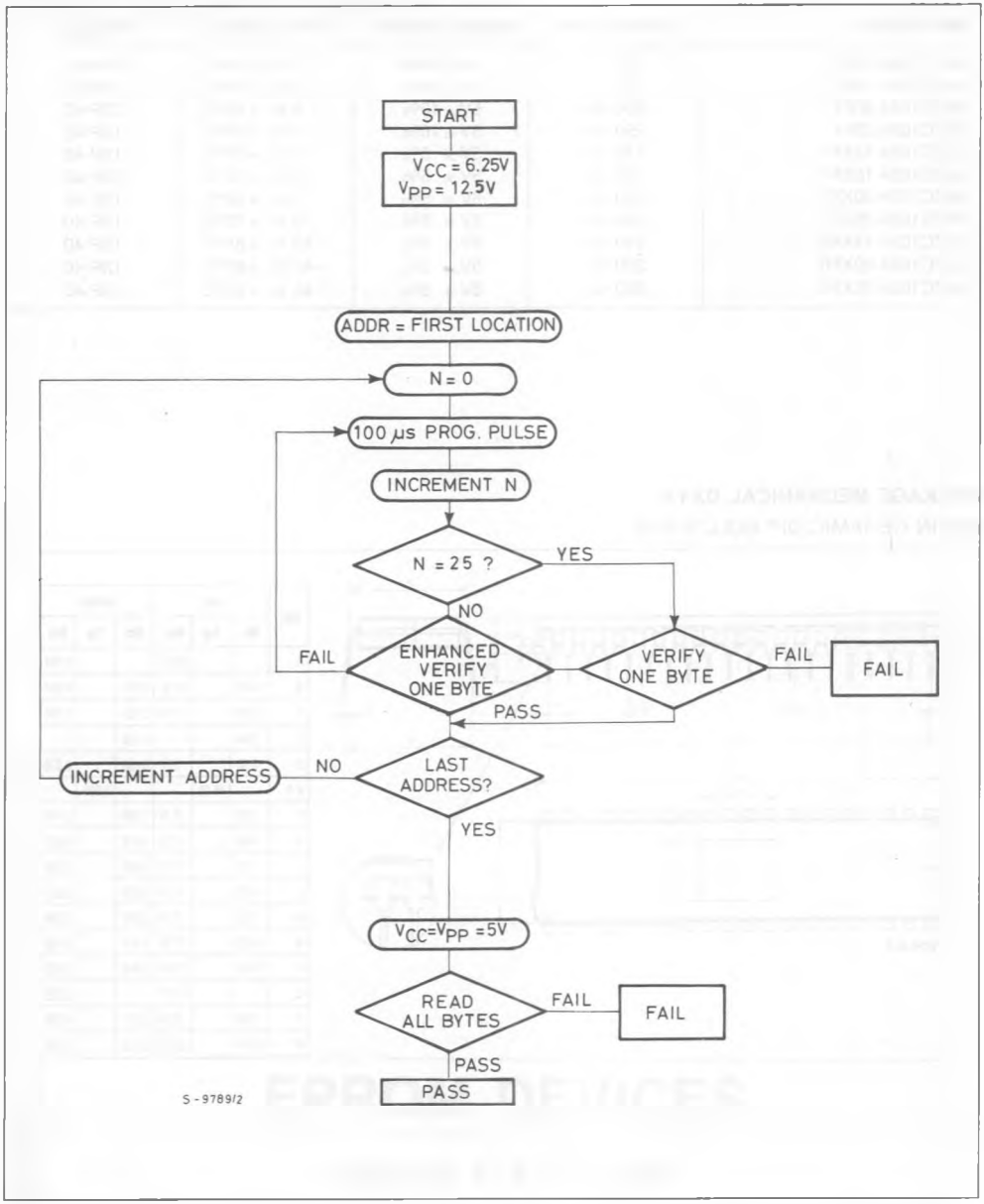
Notes:
1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. This parameter is only sampled and not 100% tested.
   Output Float is defined as the point where data is no longer driven (see timing diagram).

PROGRAMMING WAVEFORMS



Notes:
1. The input timing reference level is 0.8V for a V_{IL} and 2V for a V_{IH}.
2. t_{OE} and t_{DPF} are characteristics of the device but must be accommodated by the programmer.
3. When programming the M27C1024 a 0.1µF capacitor is required across V_{PP} and GROUND to suppress spurious voltage transients which can damage the device.

PRESTO II PROGRAMMING ALGORITHM

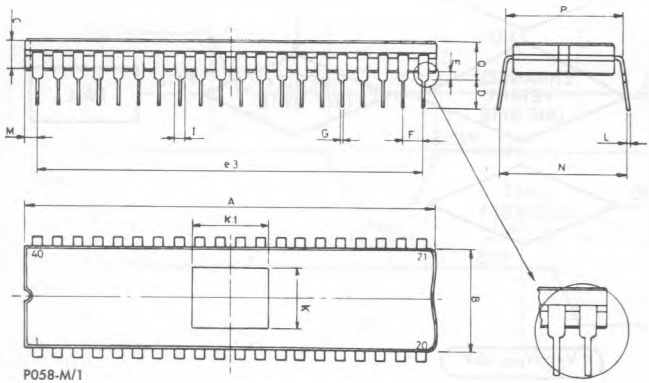


ORDERING INFORMATION

Part Number	Access Time	Supply Voltage	Temp. Range	Package
M27C1024-12F1	120 ns	5V ± 10%	0 to +70°C	DIP-40
M27C1024-15F1	150 ns	5V ± 10%	0 to +70°C	DIP-40
M27C1024-20F1	200 ns	5V ± 10%	0 to +70°C	DIP-40
M27C1024-25F1	250 ns	5V ± 10%	0 to +70°C	DIP-40
M27C1024-12XF1	120 ns	5V ± 5%	0 to +70°C	DIP-40
M27C1024-15XF1	150 ns	5V ± 5%	0 to +70°C	DIP-40
M27C1024-20XF1	200 ns	5V ± 5%	0 to +70°C	DIP-40
M27C1024-25XF1	250 ns	5V ± 5%	0 to +70°C	DIP-40
M27C1024-15XF6	150 ns	5V ± 5%	−40 to +85°C	DIP-40
M27C1024-20XF6	200 ns	5V ± 5%	−40 to +85°C	DIP-40
M27C1024-25XF6	250 ns	5V ± 5%	−40 to +85°C	DIP-40

PACKAGE MECHANICAL DATA

40-PIN CERAMIC DIP BULL'S EYE



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A			53.40			2.102
B	14.50		14.90	0.571		0.587
C	3.90		5.08	0.154		0.200
D	3.40			0.134		
E	0.50		1.78	0.020		0.070
e 3		48.26			1.900	
F	2.29		2.79	0.090		0.110
G	0.40		0.55	0.016		0.022
I	1.27		1.52	0.050		0.060
L	0.22		0.31	0.009		0.012
M	1.52		2.49	0.060		0.098
N	15.62		17.78	0.615		0.700
P	15.40		15.80	0.606		0.622
Q			5.71			0.225
K	7.90		8.38	0.311		0.330
K1	10.41		10.92	0.410		0.430