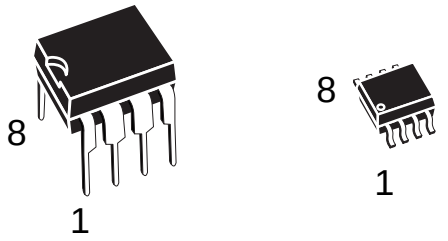
M34S32

32K Serial I^2C Bus EEPROM With User-Defined Read-Only Block and 32-Byte OTP Page

PRELIMINARY DATA - DATA BRIEFING

- TWO WIRE I^2C SERIAL INTERFACE, SUPPORTS 400kHz PROTOCOL
- COMPATIBLE WITH I^2C EXTENDED ADDRESSING
- 1 MILLION ERASE/WRITE CYCLES
- 40 YEARS DATA RETENTION
- SINGLE SUPPLY VOLTAGE
- HARDWARE WRITE CONTROL
- USER-DEFINED READ-ONLY BLOCK
- 32 BYTES OTP PAGE
- BYTE and PAGE WRITE (up to 32 BYTES)
- BYTE, RANDOM and SEQUENTIAL READ MODES
- SELF TIMED PROGRAMING CYCLE
- AUTOMATIC ADDRESS INCREMENTING
- ENHANCED ESD and LATCH-UP PERFORMANCES

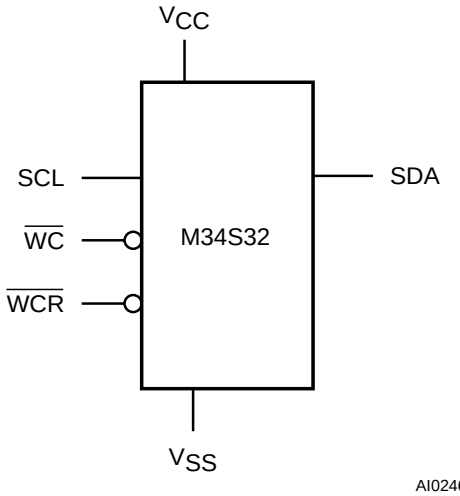
Figure 1. Delivery Forms



PSDIP8 (BN)
0.25 mm Frame

S08 (MN)
150 mil Width

Figure 2. Logic Diagram



DESCRIPTION

The M34S32 is a 32K bit electrically erasable programmable memory (EEPROM), organized as 4096 x 8 bits.

Table 1. Signal Names

SDA	Serial Data Address Input/Output
SCL	Serial Clock
$\overline{WC}$	Write Control
$\overline{WCR}$	Write Control of Control Register
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 3. DIP Pin Connections

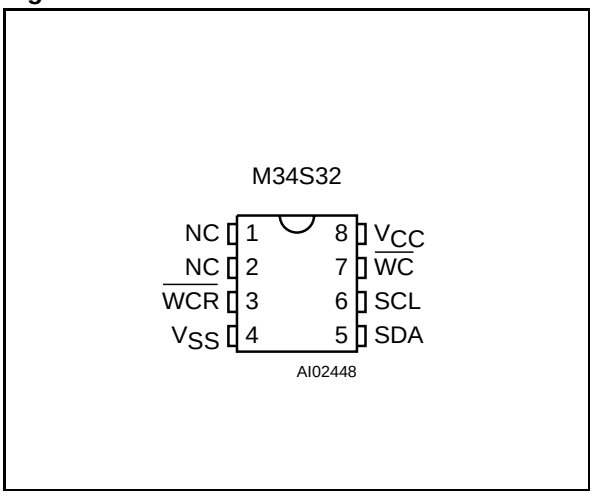
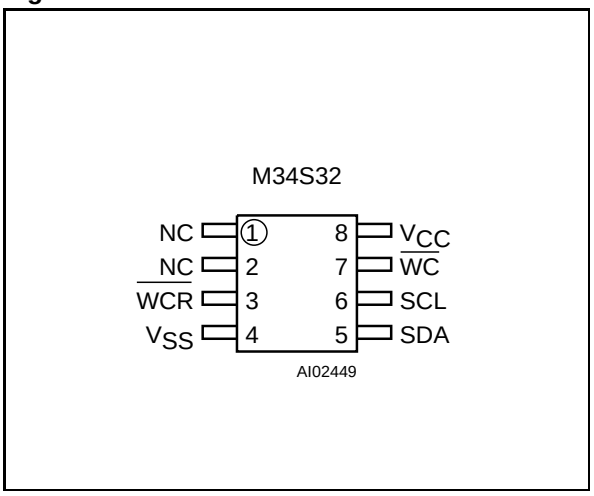


Figure 4. SO Pin Connections



DESCRIPTION (cont'd)

The memory is compatible with the I^2C extended addressing standard, two wire serial interface which uses a bi-directional data bus and serial clock. The memory carries a built-in 4 bit, unique device identification code (1010) corresponding to the I^2C bus definition. The memory behaves as slave devices in the I^2C protocol with all memory operations synchronized by the serial clock. Read and write operations are initiated by a START condition generated by the bus master. The START condition is followed by the Device Select Byte. This is a stream of 4 bits (the identification code 1010), then 3 bits of memory block access input, plus one read/write bit. The byte is finally terminated by an acknowledge bit.

The M34S32 contains three memory blocks: the OTP page, the EEPROM block and the ROM block. The OTP (One Time Programmable) page is a page of 32 bytes, written once by the user. The OTP page is not located within the 32 Kbits EEPROM area. Once written, the OTP page cannot be modified by further write instructions. The ROM block resides inside the 32 Kbit EEPROM area. The size of the ROM block is defined (by the user) with the help of the Control Register.

The OTP page is accessed with the Device Select Byte 1010001x, the EEPROM and ROM blocks are accessed with the Device Select Byte 1010000x. The control register is accessed with the Device Select Byte 1010100x.

ORDERING INFORMATION SCHEME

Devices are shipped from the factory with the memory content set at all "1"s (FFh).

For a list of available options, refer to the current *Memory Shortform Catalogue*.

For further information on any aspect of this device, please contact the ST Sales Office nearest to you.

In general, the fields of the product number are made up as follows:

Example: **M34 S 32 - W MN 1 T**

Capacity

32 32 Kbit (4K x 8)

Operating Voltage

blank 4.5 V to 5.5 V

W 2.5 V to 5.5 V

Package

BN PSDIP8 (0.25 mm frame)

MN SO8 (150 mils width)

Temperature Range

1 0 °C to +70 °C (See note 1)

6 -40 °C to +85 °C

5 -20 °C to +85 °C

Option

T Tape & Reel Packing

Note: 1. Temperature range on request only.