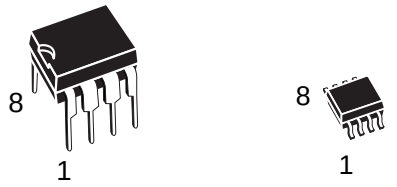
SGS-THOMSON MICROELECTRONICS

M34W02

2Kbit Serial EEPROM with Software Data Protection

PRELIMINARY DATA

- TWO WIRE I^2C SERIAL INTERFACE SUPPORTS 400kHz PROTOCOL
- 1 MILLION ERASE/WRITE CYCLES
- 40 YEARS DATA RETENTION
- SINGLE SUPPLY VOLTAGE:
  - 4.5V to 5.5V for M34W02
  - 2.5V to 5.5V for M34W02-W
  - 1.8V to 5.5V for M34W02-R
- SOFTWARE DATA PROTECTION
- BYTE and PAGE WRITE (up to 16 BYTES)
- BYTE, RANDOM and SEQUENTIAL READ MODES
- SELF TIMED PROGRAMMING CYCLE
- AUTOMATIC ADDRESS INCREMENTING
- ENHANCED ESD and LATCH-UP PERFORMANCES

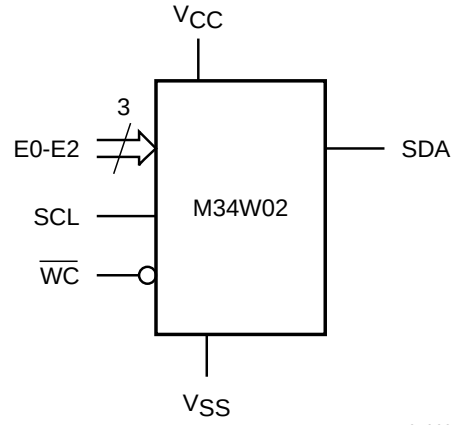


PSDIP8 (BN)
0.25mm Frame

SO8 (MN)
150mil Width

TSSOP8 (DW)
169mil Width

Figure 1. Logic Diagram



DESCRIPTION

The M34W02 is a 2K bit electrically erasable programmable memory (EEPROM), organized as 256 x 8-bits which includes a Software Data Protection feature. This allows Write Protection of a block of memory with a selectable size and location. By sending the device a specific sequence, it is possible to protect the top or the bottom locations of the memory area. The protection is activated when the $\overline{WC}$ pin is held high.

Table 1. Signal Names

E0-E2	Chip Enable Inputs
SDA	Serial Data Address Input/Output
SCL	Serial Clock
$\overline{WC}$	Write Control
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 2A. DIP Pin Connections

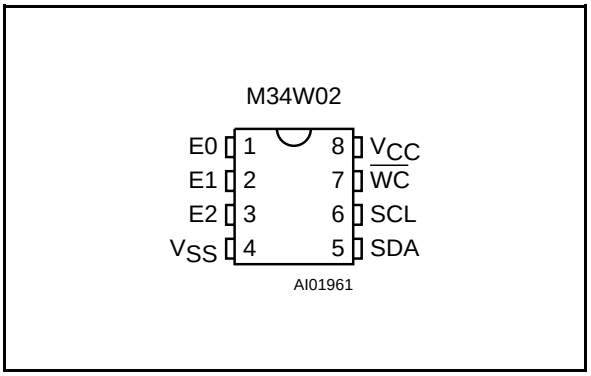


Figure 2B. SO and TSSOP Pin Connections

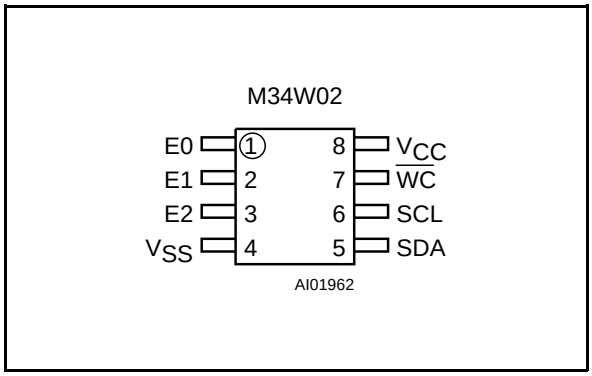


Table 2. Absolute Maximum Ratings (1)

Symbol	Parameter			Value	Unit
T_A	Ambient OperatingTemperature (2)			–40 to 85	°C
T_{STG}	Storage Temperature			–65 to 150	°C
T_{LEAD}	Lead Temperature, Soldering	(PSDIP8 package) (SO8 package) (TSSOP8 package)	10 sec 40 sec t.b.c.	260 215 t.b.c.	°C
V_{IO}	Input or Output Voltages			–0.6 to 6.5	V
V_{CC}	Supply Voltage			–0.3 to 6.5	V
V_{ESD}	Electrostatic Discharge Voltage (Human Body model) (3)			4000	V
	Electrostatic Discharge Voltage (Machine model) (4)			500	V

Notes: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.
2. Depends on range.
3. MIL-STD-883C, 3015.7 (100pF, 1500 Ω).
4. EIAJ IC-121 (Condition C) (200pF, 0 Ω).

DESCRIPTION (cont'd)

The M34W02 is manufactured in SGS-THOMSON's Hi-Endurance Advanced CMOS technology. The memories operate with a power supply value as low as 1.8V for the M34W02-R.

Plastic Dual In-line, Plastic Small Outline and Thin Shrink Small Outline packages are available.

The memory is compatible with the I^2C standard, two-wire serial interface which uses a bi-directional data bus and serial clock. The memories carry two built-in 4-bit device identification codes: '1010' which corresponds to the I^2C bus definition to access the memory area and '0110' to access the additional Protect Register. These codes are used together with 3 chip enable inputs (E2, E1, E0) so that up to eight 2K bit devices may be attached to the I^2C bus and selected individually. The memory behaves as a slave device in the I^2C protocol with all memory operations synchronized by the serial clock. Read and write operations are initiated by a START condition generated by the bus master. The START condition is followed by a stream of 7 bits (identification code '1010' or '0110' followed by the 3 chip enable bits), plus one read/write bit ($\overline{RW}$) and terminated by an acknowledge bit.

When writing data to the memory, it responds to the 8 bits received by asserting an acknowledge bit during the 9th bit time. When data is read by the bus master, it acknowledges the receipt of the data bytes in the same way. Data transfers are terminated with a STOP condition after an Ack for WRITE and after a NoAck for a READ.

Table 3. Device Select Code

	Device Type Identifier				Chip Enable			RW
Bit	b7	b6	b5	b4	b3	b2	b1	b0
Memory Area Device Select Code	1	0	1	0	E2	E1	E0	RW
Protect Register Device Select Code	0	1	1	0	E2	E1	E0	RW

Note: The MSB b7 is sent first.

Table 4. Operating Modes (1)

Mode	RW bit	WC	Bytes	Initial Sequence
Current Address Read	'1'	X	1	START, Device Select, RW = '1'
Random Address Read	'0'	X	1	START, Device Select, RW = '0', Address,
	'1'	X		reSTART, Device Select, RW = '1'
Sequential Read	'1'	X	1 to 256	Similar to Current or Random Mode
Byte Write	'0'	V_{IL} (2)	1	START, Device Select, RW = '0'
Page Write	'0'	V_{IL} (2)	16	START, Device Select, RW = '0'

Notes: 1. X = V_{IH} or V_{IL}

2. WC input level is don't care if the data to modify is in a non-write protected area. Read also the 'Write Protection using the Protect Register paragraph.

Power On Reset: V_{CC} lock out write protect.

In order to prevent any possible data corruption and inadvertent write operations during power up, a Power On Reset (POR) circuit is implemented.

Until the V_{CC} voltage has reached the POR threshold value, the internal reset is active, all operations are disabled and the device will not respond to any command. In the same way, when V_{CC} drops from the operating voltage to below the POR threshold value, all operations are disabled and the device will not respond to any command. A stable V_{CC} must be applied before applying any logic signal.

SIGNAL DESCRIPTIONS

Serial Clock (SCL). The SCL input pin is used to synchronize all data in and out of the memory. A resistor can be connected from the SCL line to V_{CC} to act as a pull up (see Figure 3).

Serial Data (SDA). The SDA pin is bi-directional and is used to transfer data in or out of the memory. It is an open drain output that may be wire-OR'ed with other open drain or open collector signals on the bus. A resistor must be connected from the SDA bus line to V_{CC} to act as pull up (see Figure 3).

Chip Enable (E2 - E0). These chip enable inputs are used to set the 3 least significant bits (b3, b2, b1) of the 7 bit device select code. These inputs may be driven dynamically or tied to V_{CC} or V_{SS} to establish the device select code.

Write Control (WC). A hardware Write Control pin (WC), and a Protect Register, is provided on pin 7 of the M34W02. This feature is useful to protect a part or the entire contents of the memory from any erroneous erase/write cycle. The Write Control signal is used to enable (WC = V_{IL}) or disable (WC = V_{IH}) write instructions to the protected memory area and to the Protect Register. When unconnected, the WC input is internally read as V_{IH} and neither the protected memory area nor the Protect Register will be alterable.

DEVICE OPERATION

I²C Bus Background

The M34W02 supports the I²C protocol. This protocol defines any device that sends data onto the bus as a transmitter and any device that reads the data as a receiver. The device that controls the data transfer is known as the master and the other as the slave. The master will always initiate a data transfer and will provide the serial clock for synchronisation. The M34W02 is always a slave device in all communications.

Start Condition. START is identified by a high to low transition of the SDA line while the clock SCL is stable in the high state. A START condition must precede any command for data transfer. Except during a programming cycle, the M34W02 continuously monitors the SDA and SCL signals for a START condition and will not respond unless a START condition is given.

Stop Condition. STOP is identified by a low to high transition of the SDA line while the clock SCL is stable in the high state. A STOP condition terminates communication between the M34W02 and the bus master. A STOP condition at the end of a Read sequence, after and only after a No-Acknowledge, forces the standby state. A STOP condition at the end of a Write command triggers the internal EEPROM write cycle.

Acknowledge Bit (ACK). An acknowledge signal is used to indicate a successful data transfer. The bus transmitter, either master or slave, will release the SDA bus after sending 8 bits of data. During the 9th clock pulse period the receiver pulls the SDA bus low to acknowledge the receipt of the 8 bits of data.

Data Input. During data input the M34W02 samples the SDA bus signal on the rising edge of the clock SCL. Note that for correct device operation, the SDA signal must be stable during the clock low to high transition and the data must change ONLY when the SCL line is low.

Memory Addressing. To start communication between the bus master and the slave M34W02, the master must initiate a START condition. Following this, the master sends onto the SDA bus line 8 bits (MSB first) corresponding to the device select code (7 bits) and a READ or WRITE bit.

The 4 most significant bits of the device select code are the device type identifier, corresponding to the I²C bus definition. For this memory the 4 bits are fixed as 1010b to access the memory area and as 0110b to access the Protect Register. The following 3 bits identify the specific memory on the bus. They are matched to the external chip enable signals E2, E1, E0. Thus up to eight 2K memories can be connected on the same bus giving a memory capacity total of 16K bits. After a START condition any

Figure 3. Maximum R_L Value versus Bus Capacitance (C_{BUS}) for an I²C Bus, fc = 400KHz

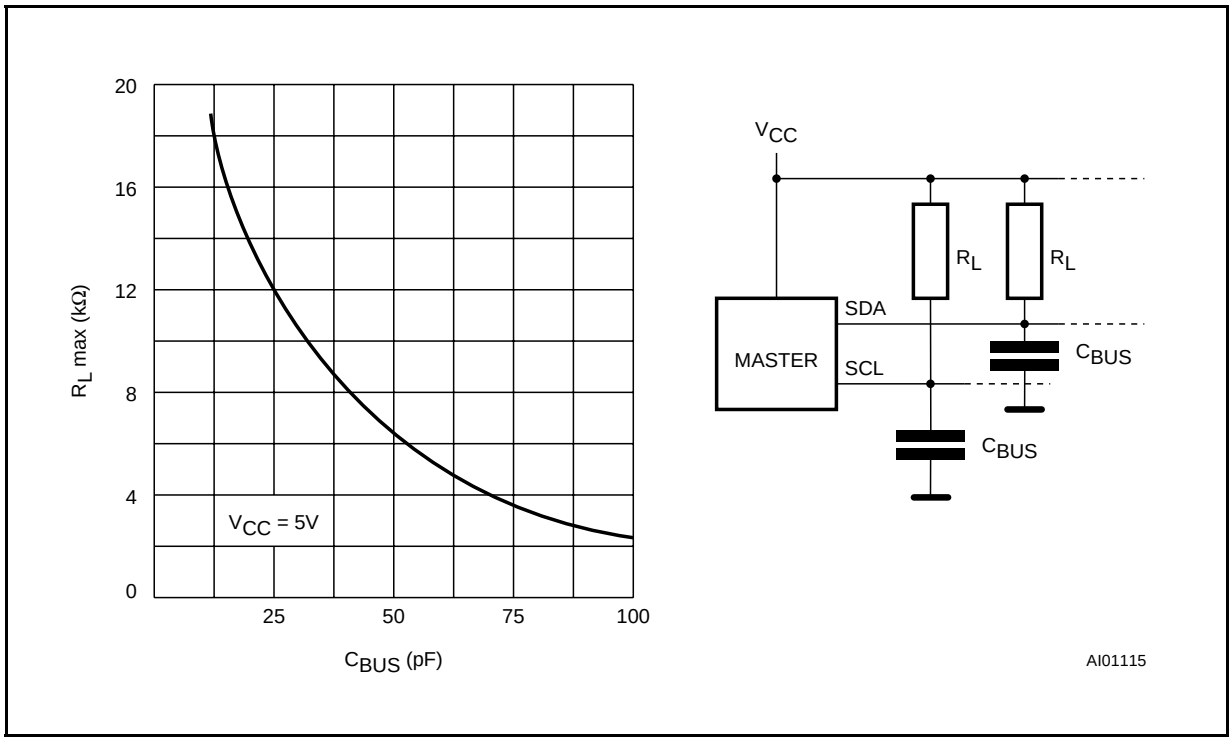


Table 5. Input Parameters (1) (T_A = 25 °C, f = 400 kHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance (SDA)			8	pF
C_{IN}	Input Capacitance (other pins)			6	pF
Z_{WCL}	WP Input Impedance	$V_{IN} < 0.3\ V_{CC}$	5	20	KΩ
Z_{WCH}	WP Input Impedance	$V_{IN} < 0.7\ V_{CC}$	500		KΩ
t_{LP}	Low-pass filter input time constant (SDA and SCL)		200	500	ns

Note: 1. Sampled only, not 100% tested.

Table 6. DC Characteristics
(T_A = 0 to 70°C or –40 to 85°C; V_{CC} = 4.5V to 5.5V, 2.5V to 5.5V or 1.8V to 5.5V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0V \le V_{IN} \le V_{CC}$		±2	µA
I_{LO}	Output Leakage Current	$0V \le V_{OUT} \le V_{CC}$ SDA in Hi-Z		±2	µA
I_{CC}	Supply Current	V_{CC} = 5V, f_C = 400kHz (Rise/Fall time < 10ns)		2	mA
		V_{CC} = 1.8V, f_C = 400kHz		1	mA
I_{CC1}	Supply Current (Standby)	$V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 5V		100	µA
		$V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 5V, f_C = 400kHz		300	µA
I_{CC2}	Supply Current (Standby)	$V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 1.8V		30	µA
		$V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 1.8V, f_C = 400kHz		100	µA
V_{IL}	Input Low Voltage (SCL, SDA)		–0.5	0.3 V_{CC}	V
V_{IH}	Input High Voltage (SCL, SDA)		0.7 V_{CC}	6.5	V
V_{IL}	Input Low Voltage (E0-E2, $\overline{WC}$)		–0.5	0.5	V
V_{IH}	Input High Voltage (E0-E2, $\overline{WC}$)		V_{CC} – 0.5	6.5	V
V_{OL}	Output Low Voltage	I_{OL} = 3mA, V_{CC} = 1.8V		0.4	V

DEVICE OPERATIONS (cont'd)

memory on the bus will identify the device code and compare the following 3 bits to its chip enable inputs E2, E1, E0.

The 8th bit sent is the read or write bit ($R\overline{W}$), this bit is set to '1' for read and '0' for write operations. If a match is found, the corresponding memory will acknowledge the identification on the SDA bus during the 9th bit time. If the memory does not match the device select code, it will self-deselect from the bus and go into standby mode.

Write Operations

Following a START condition the master sends a device select code with the $R\overline{W}$ bit set to '0'. The memory acknowledges it and waits for a byte address, which provides access to the 256 bytes of the memory area. After receipt of the byte address, the memory again responds with an acknowledge and waits for the data byte.

Table 7. AC Characteristics
(T_A = 0 to 70°C or –40 to 85°C; V_{CC} = 4.5V to 5.5V, 2.5V to 5.5V or 1.8V to 5.5V)

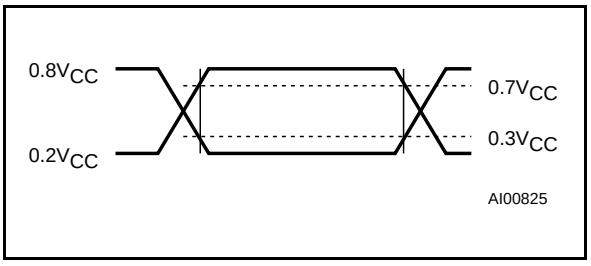
Symbol	Alt	Parameter	Min	Max	Unit
t_{CH1CH2} (1)	t_R	Clock Rise Time		300	ns
t_{CL1CL2} (1)	t_F	Clock Fall Time		300	ns
t_{DH1DH2} (1)	t_R	SDA Rise Time	20	300	ns
t_{DL1DL2} (1)	t_F	SDA Fall Time	20	300	ns
t_{CHDX} (2)	$t_{SU:STA}$	Clock High to Input Transition	600		ns
t_{CHCL}	t_{HIGH}	Clock Pulse Width High	600		ns
t_{DLCL}	$t_{HD:STA}$	Input Low to Clock Low (START)	600		ns
t_{CLDX}	$t_{HD:DAT}$	Clock Low to Input Transition	0		µs
t_{CLCH}	t_{LOW}	Clock Pulse Width Low	1.3		µs
t_{DXCX}	$t_{SU:DAT}$	Input Transition to Clock Transition	100		ns
t_{CHDH}	$t_{SU:STO}$	Clock High to Input High (STOP)	600		ns
t_{DHDL}	t_{BUF}	Input High to Input Low (Bus Free)	1.3		µs
t_{CLQV}	t_{AA}	Clock Low to Next Data Out Valid	200	900	ns
t_{CLQX}	t_{DH}	Data Out Hold Time	200		ns
f_C	f_{SCL}	Clock Frequency		400	kHz
t_W	t_{WR}	Write Time		10	ms

Notes: 1. Sampled only, not 100% tested.
2. For a reSTART condition, or following a write cycle.

Table 8. AC Measurement Conditions

Input Rise and Fall Times	≤ 50ns
Input Pulse Voltages	$0.2V_{CC}$ to $0.8V_{CC}$
Input and Output Timing Ref. Voltages	$0.3V_{CC}$ to $0.7V_{CC}$

Figure 4. AC Testing Input Output Waveforms

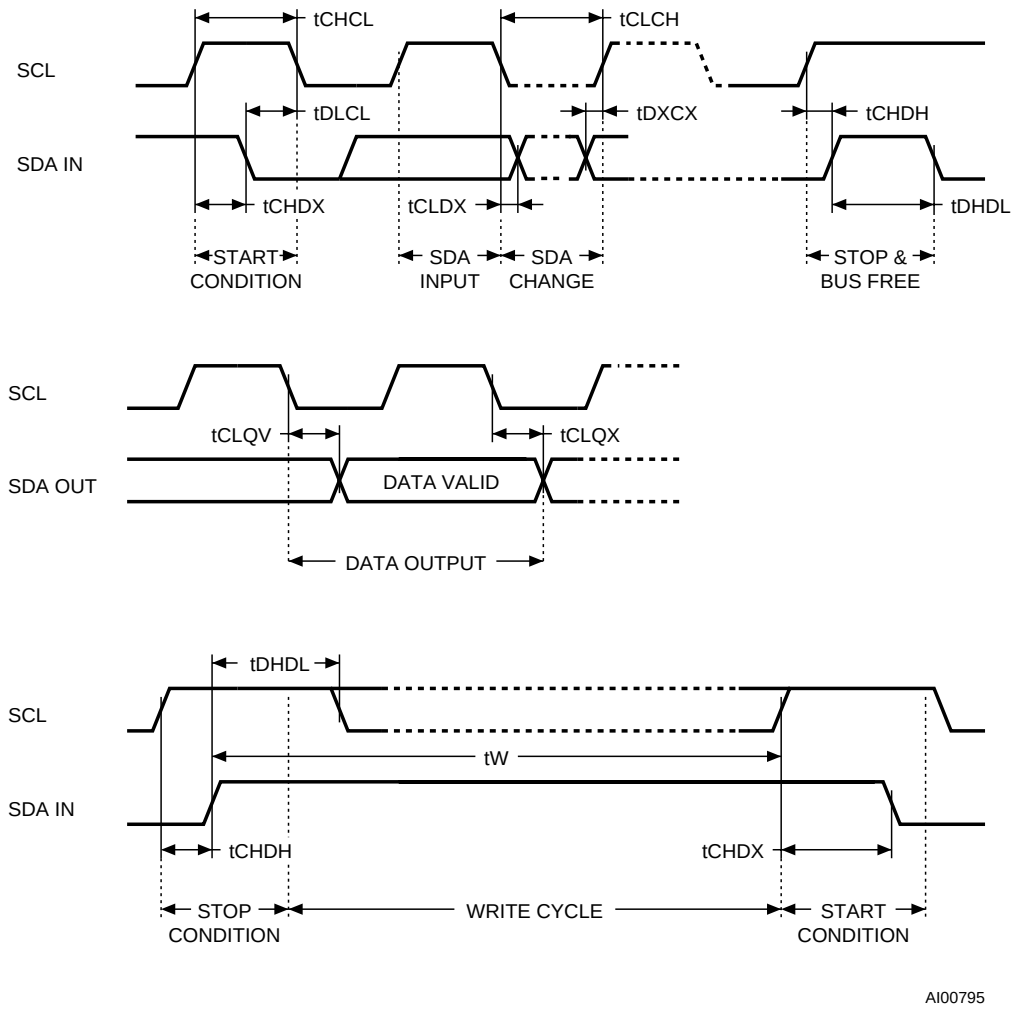


Byte Write. In the Byte Write mode, after the device select code and the address, the master sends one data byte. If the addressed location is in a write protected area, the memory sends a NoACK and the location is not modified. If the addressed location is not write protected, the memory sends an ACK. The master terminates the transfer by generating a STOP condition.

Depending on the 4 MSBs of the device select code, the Byte Write instruction can be used to modify a memory location (device select code 1010b) or can be used to access to the Protect Register contents (device select code 0110b).

Page Write. The Page Write mode allows up to 16 bytes to be written in a single write cycle, provided that they are all located in the same 'row' in the memory: that is the 4 most significant memory address bits (A7-A4) are the same. The master sends from one up to 16 bytes of data, which are

Figure 5. AC Waveforms

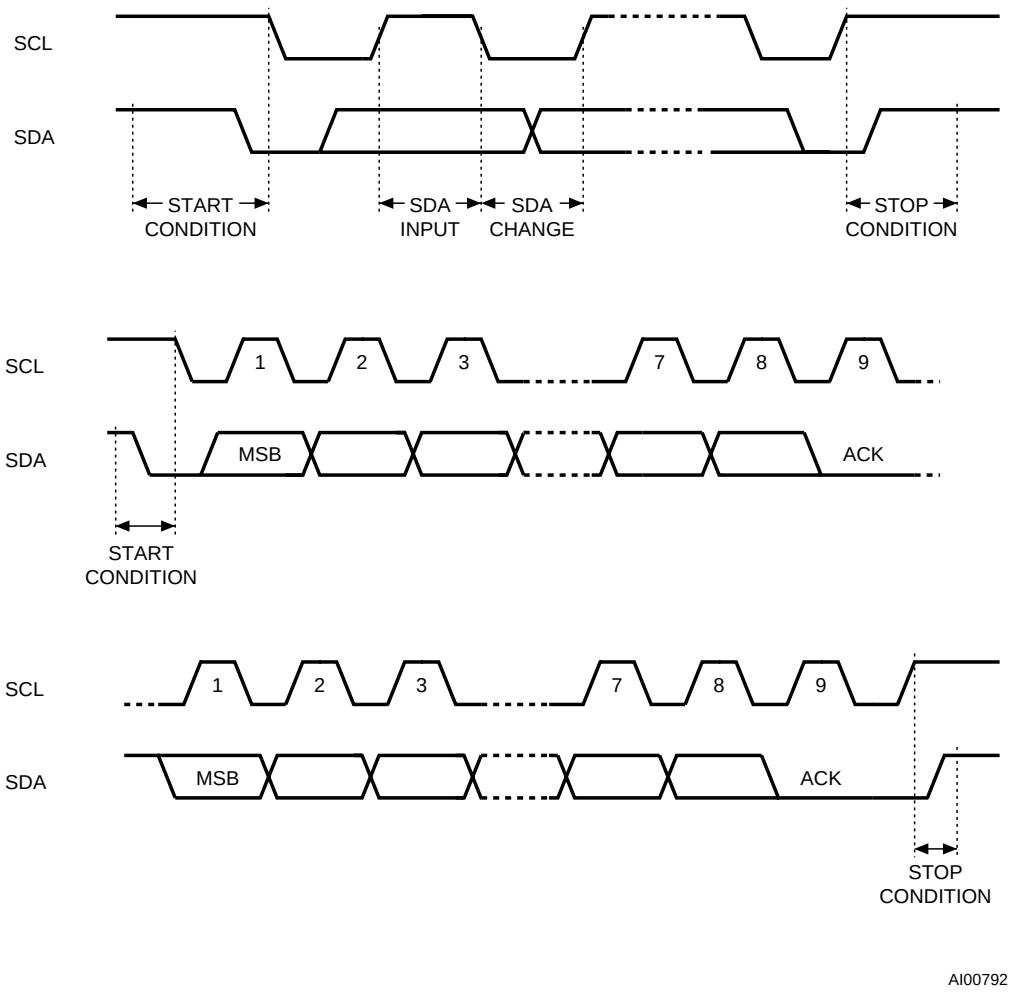


each acknowledged by the memory if the addressed row is not write protected. If the addressed row is write protected, each data byte is followed by a NoACK and the locations will not be modified. After each byte is transferred, the internal byte address counter (4 least significant bits only) is incremented. The transfer is terminated by the master generating a STOP condition.

Care must be taken to avoid address counter 'rollover' which could result in data being overwritten. Note that, for any byte or page write mode, the generation by the master of the STOP condition starts the internal memory program cycle. All inputs are disabled until the completion of this cycle and the memory will not respond to any request.

Minimizing System Delays by Polling On ACK. During the internal write cycle, the memory disconnects itself from the bus in order to copy the data from the internal latches to the memory cells. The maximum value of the write time (t_W) is given in the AC Characteristics table. Since the typical time is shorter, the time seen by the system may be reduced by an ACK polling sequence issued by the master.

Figure 6. I²C Bus Protocol



The sequence is as follows:

– Initial condition: a Write is in progress (see Figure 7).

– Step 1: the master issues a START condition followed by a device select byte (1st byte of the new instruction).

– Step 2: if the memory is busy with the internal write cycle, NoACK will be returned and the master goes back to Step 1. If the memory has terminated the internal write cycle, it will respond with an ACK, indicating that the memory is ready to receive the second part of the incoming instruction (the first byte of this instruction was already sent during Step 1).

Set the Protection using the Protect Register. The M34W02 has a software write protection function, with the use of a Protect Register, that allows a selectable memory area size to be defined as write protected. To activate the write protection feature, an address pointer has to be written into the Protect Register. When write protected by the Protect Register and the $\overline{WC}$ pin, the selected memory area will behave as a ROM area.

The Protect Register is accessed by sending a write command with the 4 device type identifier bits of the device select code set to 0110b (see Figure 9), the E2-E1-E0 bits as applied on the E2-E1-E0 pins and regardless of the state of the $\overline{WC}$ signal.

In this sequence, the address byte value is don't care and the Data byte is programmed in the protect register. The write protection is activated by putting the $\overline{WC}$ pin high (see Figure 9).

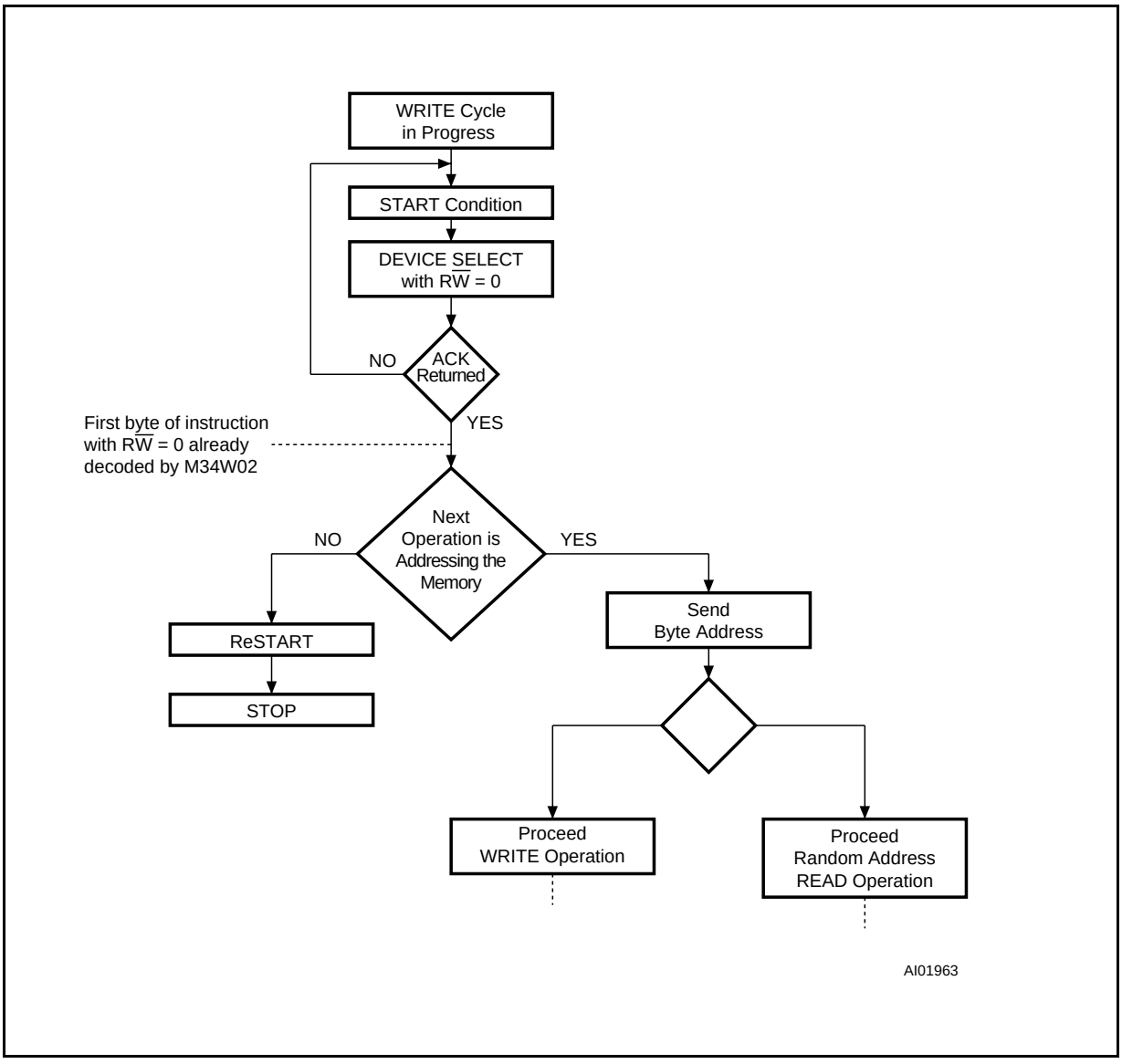
The Protect Register is a 8 bit EEPROM register which contains a 7 bit row pointer (b6-b0) and 1 bit (b7), named Top/Bottom. When using the Protect Register, the EEPROM area will be divided in 2 different zone. The first zone is from location 00h to the pointed row with its 16 bytes included.

The second zone is the rest of the memory to the top. Depending on the value of bit 7 of the Protect Register, it is possible to write protect the first zone (b7=0) or the second zone (b7=1).

As a row is 16 bytes long, it is possible to write protect from 16 bytes up to the entire 256 bytes with a step of 16 bytes (see Figure 9).

The Protect Register contents can be write protected using the $\overline{WC}$ input pin (pin 7). When the $\overline{WC}$ input is read at V_{IH}, it ensures that the Protect Register cannot be modified (device select code 0110xxxx not Acknowledged) and the write protected EEPROM area will behave as a ROM.

Figure 7. Write Cycle Polling using ACK



DEVICE OPERATIONS (cont'd)

b0 to b6: this is the row pointer value which contains the selected row number. This row number is used as a memory pointer which will determine the protected area size.

b7: Top/Bottom: When b7=0 (WC=1), the protected area will be from location 00h to the pointed row (zone 1). When b6-b0 of the protect register are all 0, all the memory locations are not write protected. When b7=1 (WC=1), the protected area will be from the pointed row to the end of the memory (zone 2). When b6-b0 of the protect register are all 0, all the memory locations are write protected.

On delivery, the Protect Register is set to 00h (all bits at '0'). This specific state allows the Protect Register to be programmed once even if the WC input is high. This feature is useful to program the Protect Register with the M34W02 soldered in the application. Pin 7 of the M34W02 can be directly connected to V_{CC}. After and only after programming the Protect Register, even with the value 00h, the WC input (pin 7) will be activated by the M34W02: the Protect Register and the selected memory area will be write protected.

It is possible to modify the write protected area by pulling the WC pin low (see Figure 9).

To modify the Protect Register content, the WC input must be low. At this time, it is possible to modify all the 8 bits of the protect register (bit 7 included). This feature allows you to modify the protected area size and to modify the selected memory zone by changing the value of bit 7.

Read Operations

Read operations are independent from the state of the Protect Register and the WC input pin. On delivery, the memory contents is set at all "1's" (or FFh) and the Protect Register at all "0's" (or 00h).

Current Address Read. The memory has an internal byte address counter. Each time a byte is read, this counter is incremented. For the Current Address Read mode, following a START condition, the master sends a device select code with the RW bit set to '1'. The memory acknowledges this and outputs the byte addressed by the internal byte address counter. This counter is then incremented. The master must NOT acknowledge the byte output and must terminate the transfer with a STOP condition.

It is possible, when the WC input pin is low, to read the contents of the protect register. In this case, after the START condition, the device select code must have the 4 device type identifier bits set to 0110b. When the WC input pin is high, it is not possible to read the protect register.

Random Address Read. A dummy write is performed to load the memory address into the address counter, see Figure 11. This is followed by another START condition from the master and the device select code is repeated with the RW bit set to '1'. The memory acknowledges this and outputs the byte addressed. The master must NOT acknowledge the byte output and must terminate the transfer with a STOP condition.

Figure 8. Protected Area Size

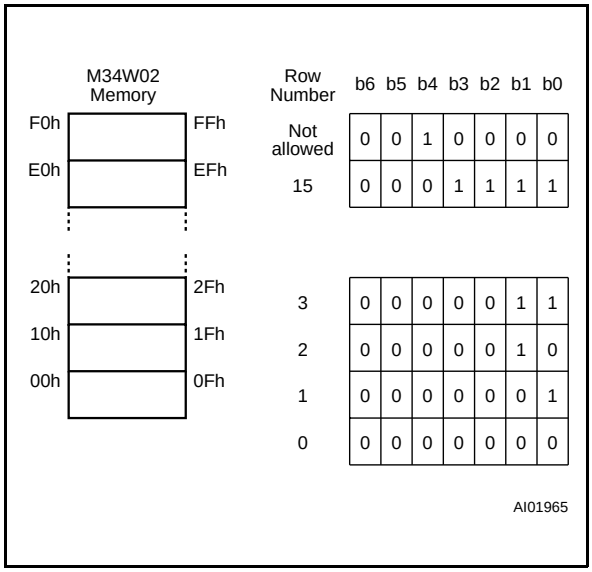


Table 9. Protect Register Bit Value

Bit	Top / Bottom	ROW pointer						
	b7	b6	b5	b4	b3	b2	b1	b0
Protect Register bits	T/B	rp6	rp5	rp4	rp3	rp2	rp1	rp0
Protect Register bits values on delivery	0	0	0	0	0	0	0	0

Figure 9. Memory Protection

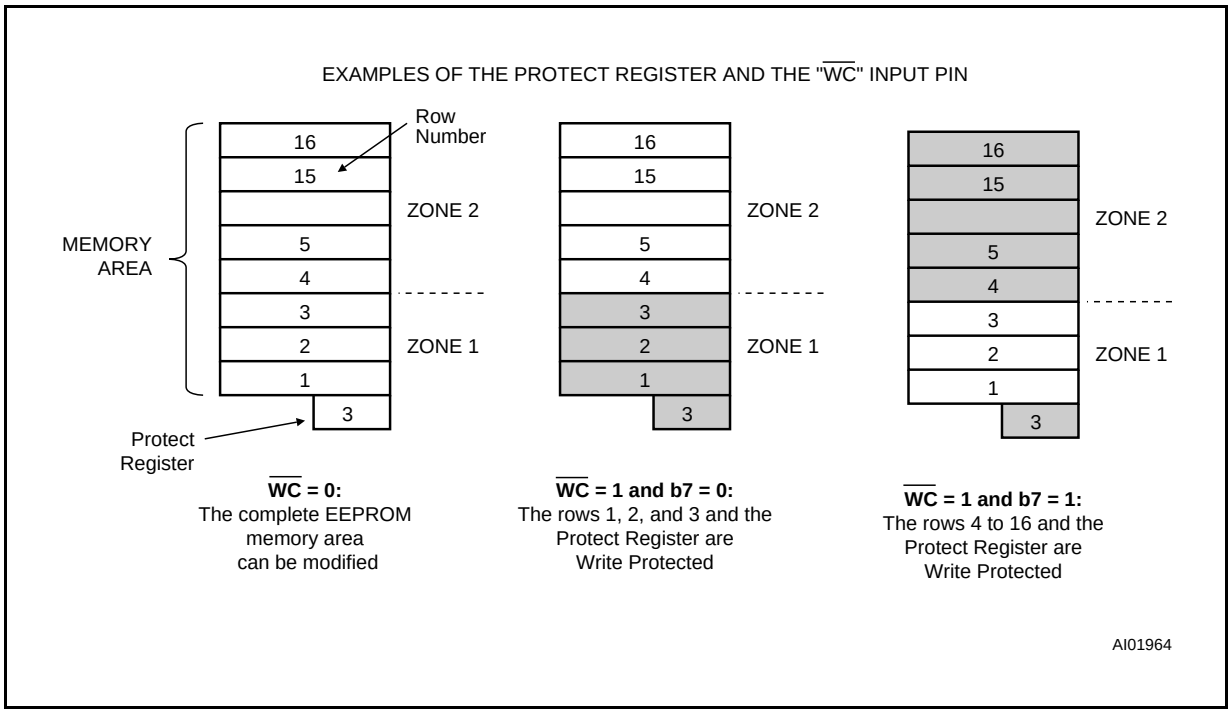


Figure 10. Write Modes Sequence in Non-Write Protected Area

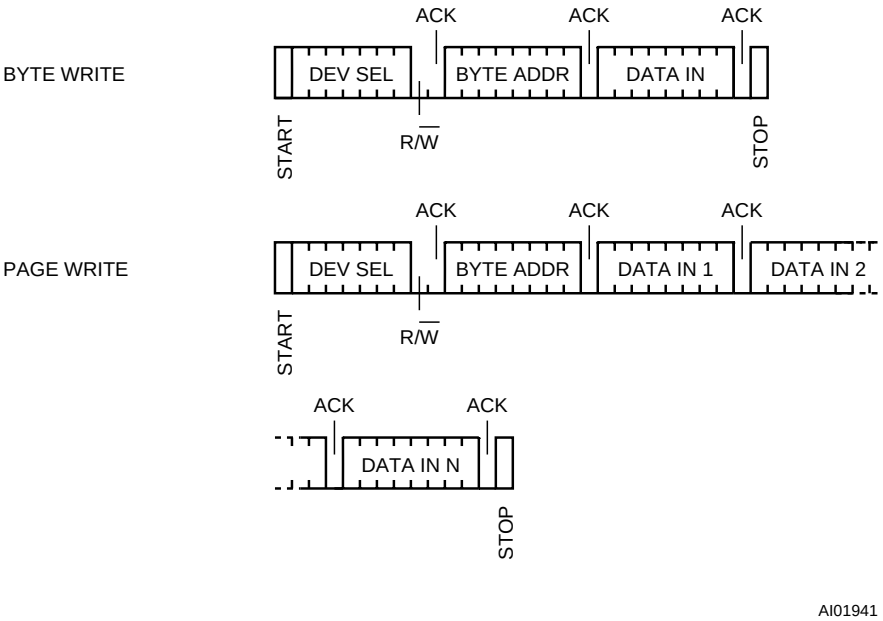
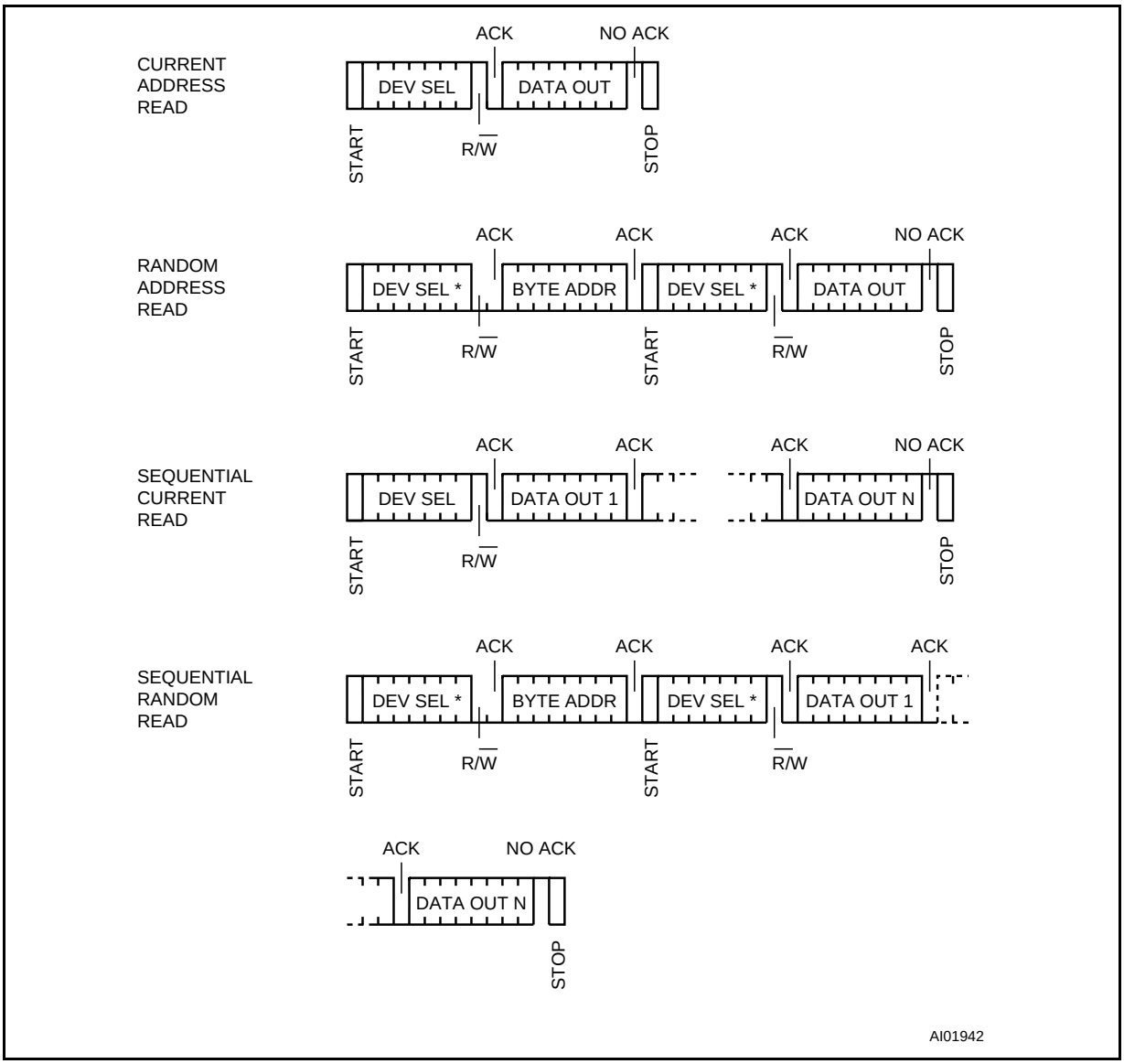


Figure 11. Read Modes Sequence

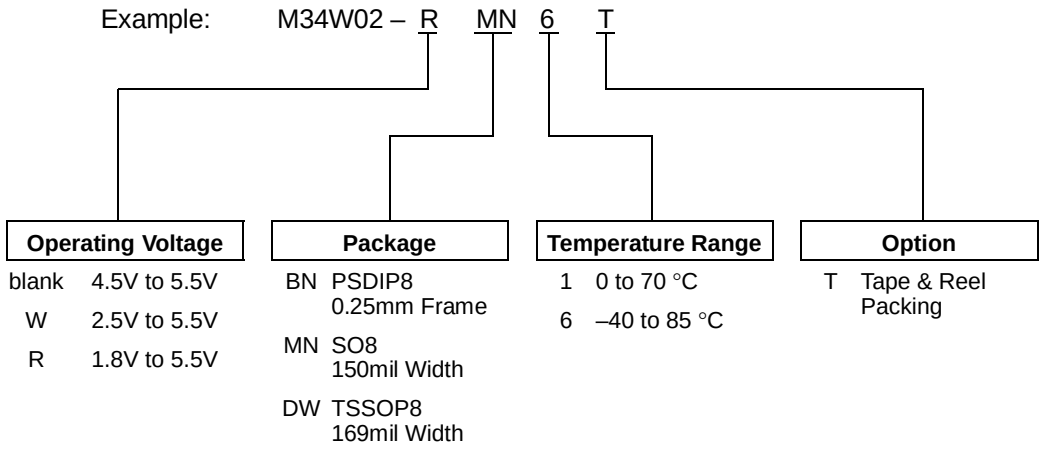


Note: * The 7 Most Significant bits of DEV SEL bytes of a Random Read (1st byte and 3rd byte) must be identical.

Sequential Read. This mode can be initiated with either a Current Address Read or a Random Address Read. However, in this case the master DOES acknowledge the data byte output and the memory continues to output the next byte in sequence. To terminate the stream of bytes, the master must NOT acknowledge the last byte output and MUST generate a STOP condition. The output data is from consecutive byte addresses, with the internal byte address counter automatically incremented after each byte output. After a count giving the last memory address, the address counter will 'roll- over' and the memory will continue to output data.

Acknowledge in Read Mode. In all read modes the M34W02 waits for an acknowledge during the 9th bit time. If the master does not pull the SDA line low during this time, the M34W02 terminates the data transfer and switches to a standby state.

ORDERING INFORMATION SCHEME

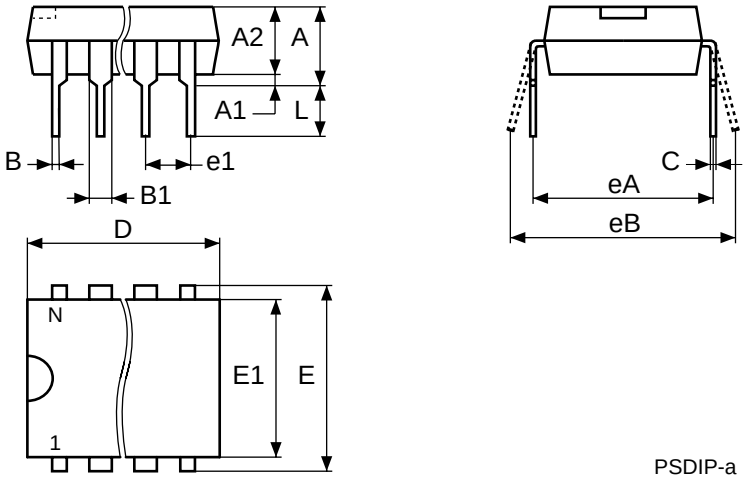


Devices are shipped from the factory with the memory content set at all "1's" (FFh).

For a list of available options (Operating Voltage, Package, etc...) or for further information on any aspect of this device, please contact the SGS-THOMSON Sales Office nearest to you.

PSDIP8 - 8 pin Plastic Skinny DIP, 0.25mm lead frame

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		3.90	5.90		0.154	0.232
A1		0.49	–		0.019	–
A2		3.30	5.30		0.130	0.209
B		0.36	0.56		0.014	0.022
B1		1.15	1.65		0.045	0.065
C		0.20	0.36		0.008	0.014
D		9.20	9.90		0.362	0.390
E	7.62	–	–	0.300	–	–
E1		6.00	6.70		0.236	0.264
e1	2.54	–	–	0.100	–	–
eA		7.80	–		0.307	–
eB			10.00			0.394
L		3.00	3.80		0.118	0.150
N	8			8		

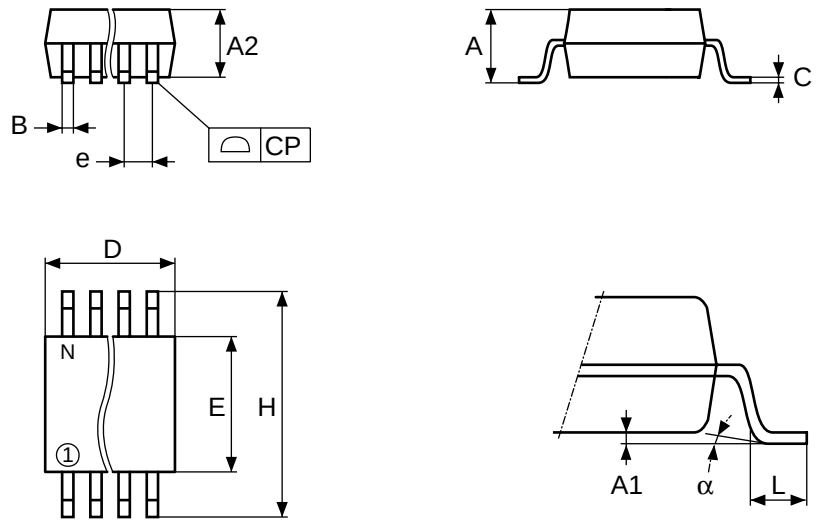


PSDIP-a

Drawing is not to scale.

SO8 - 8 lead Plastic Small Outline, 150 mils body width

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		1.35	1.75		0.053	0.069
A1		0.10	0.25		0.004	0.010
B		0.33	0.51		0.013	0.020
C		0.19	0.25		0.007	0.010
D		4.80	5.00		0.189	0.197
E		3.80	4.00		0.150	0.157
e	1.27	–	–	0.050	–	–
H		5.80	6.20		0.228	0.244
h		0.25	0.50		0.010	0.020
L		0.40	0.90		0.016	0.035
α		0°	8°		0°	8°
N	8			8		
CP			0.10			0.004

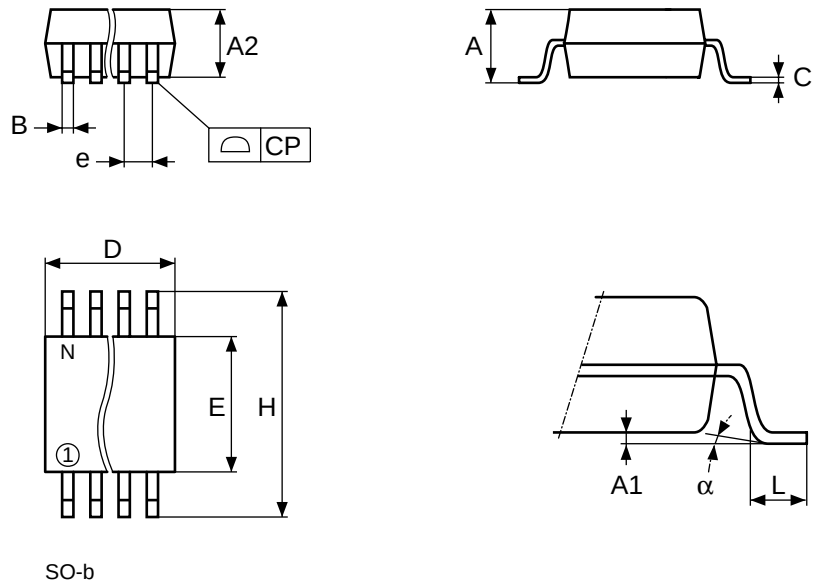


SO-b

Drawing is not to scale.

TSSOP8 - 8 lead Thin Shrink Small Outline

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			1.10			0.043
A1		0.05	0.15		0.002	0.006
A2		0.85	0.95		0.033	0.037
B		0.19	0.30		0.007	0.012
C		0.09	0.20		0.004	0.008
D		2.90	3.10		0.114	0.122
E		4.30	4.50		0.169	0.177
e	0.65	–	–	0.026	–	–
H		6.25	6.50		0.246	0.256
L		0.50	0.70		0.020	0.028
α		0°	8°		0°	8°
N	8			8		
CP			0.08			0.003



SO-b

Drawing is not to scale.