MOS INTEGRATED CIRCUIT

M 36000

PRELIMINARY DATA

64K-BIT READ ONLY MEMORY

- 8K x 8 ORGANIZATION - EDGE ENABLED OPERATION ($\overline{CE}$)
- 250 ns ACCESS TIME, 375 ns CYCLE TIME FOR M36000-4
  300 ns ACCESS TIME, 450 ns CYCLE TIME FOR M36000-5
- SINGLE +5V ±10% POWER SUPPLY
- LOW POWER DISSIPATION: 220 mW MAX ACTIVE
- LOW STANDBY POWER DISSIPATION: 35 mW MAX ($\overline{CE}$ HIGH)
- ON CHIP LATCHES FOR ADDRESSES (CONTROLLED BY $\overline{CE}$ INPUT)
- INPUTS AND THREE-STATE OUTPUTS - TTL COMPATIBLE
- OUTPUT DRIVE 2 TTL LOADS AND 100 pF
- STANDARD 24 PIN DIP (EPROM PIN OUT COMPATIBLE)

The M36000 is a N--channel silicon gate MOS Read Only Memory, organized as 8192 words by 8 bits. This device incorporates advanced circuit techniques designed to provide maximum circuit density and reliability with the highest possible performance, while maintaining low power dissipation and wide operating margins. The M36000 utilizes a static storage cell with clocked control periphery which allows the circuit to be put into an automatic low power standby mode. This is accomplished by maintaining the chip enable ($\overline{CE}$) input at a TTL high level. In this mode, power dissipation is reduced to typically 35 mW, as compared to unclocked devices which draw full power continuously. In system operation, a device is selected by the $\overline{CE}$ input, while all others are in a low power mode, reducing the overall system power. The edge enabled operation means greater system flexibility and an increase in system speed, making this device ideally suited for 8 bit microprocessor systems such as those which utilize the Z80. It can offer significant cost advantages over PROM. The M36000 is available in 24-lead dual in-line plastic or ceramic package.

ABSOLUTE MAXIMUM RATINGS*

V_i	Voltage on any pin with respect to Ground	-1 to +7	V
P_{tot}	Total power dissipation	1	W
T_{stg}	Storage temperature: for ceramic package	-65 to +150	°C
	for plastic package	-55 to +125	°C
T_{op}	Operating temperature	0 to +70	°C

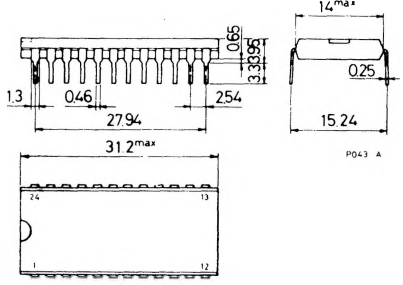
* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating conditions of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING NUMBERS:

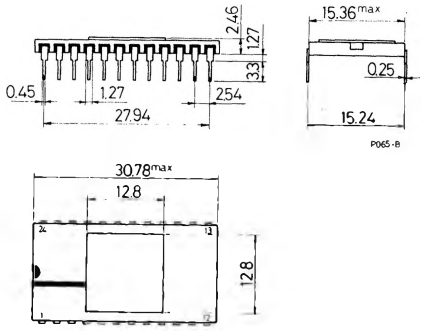
M36000 - 4 B1	for dual in-line plastic package
M36000 - 4 D1	for dual in-line ceramic package
M36000 - 4 F1	for dual in-line ceramic package, frit-seal
M36000 - 5 B1	for dual in-line plastic package
M36000 - 5 D1	for dual in-line ceramic package
M36000 - 5 F1	for dual in-line ceramic package, frit-seal

MECHANICAL DATA (dimensions in mm)

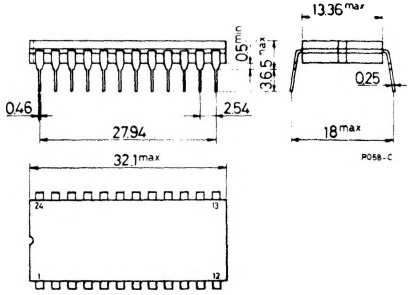
Dual in-line plastic package



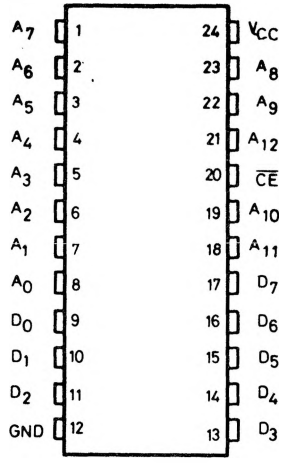
Dual in-line ceramic package



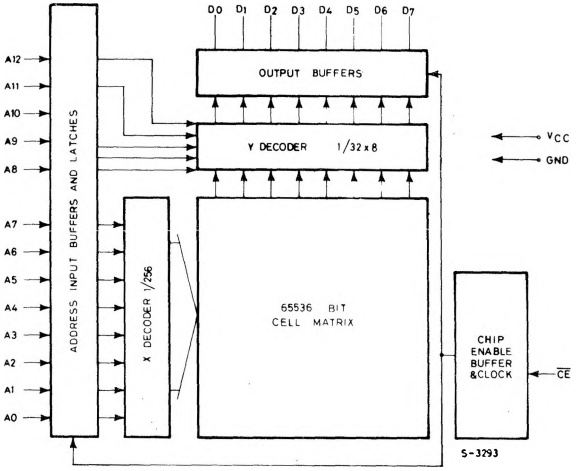
Dual in-line ceramic package, frit-seal



PIN CONNECTIONS



BLOCK DIAGRAM



RECOMMENDED DC OPERATING CONDITIONS[1] (T_{amb} = 0 to 70° C unless otherwise specified)

Parameter		Test conditions	Values			Unit
			Min.	Typ.	Max.	
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	Input high voltage		2		V_{CC}	V
V_{IL}	Input low voltage		-1		0.8	V

STATIC ELECTRICAL CHARACTERISTICS[1] (T_{amb} = 0 to 70°C unless otherwise specified)

Parameter		Test conditions	Values			Unit
			Min.	Typ.	Max.	
V_{OH}	Output high voltage	I_{OH} = -220 μA	2.4			V
V_{OL}	Output low voltage	I_{OL} = 3.3 mA			0.4	V
I_{LI}	Input leakage current	V_I = 0 to 5.5V	-10		10	μA
I_{LO}	Output leakage current	Device unselected; V_o = 0 to 5.5V	-10		10	μA
I_{CC1}	Supply current (active)[2]				40	mA
I_{CC2}	Supply current (standby)	$\overline{CE}$ high			8	mA

DYNAMIC ELECTRICAL CHARACTERISTICS[1] (T_{amb} = 0 to 70°C unless otherwise specified)

Parameter		Test conditions	M36000 - 4		M36000 - 5		Unit
			Min.	Max.	Min.	Max.	
t_C	Cycle time	Output load = 2 TTL gate and 100 pF, transition times = 20 ns	375		450		ns
t_{CE}	$\overline{CE}$ pulse width		250		300		ns
t_{AC}	$\overline{CE}$ access time			250		300	ns
t_{OFF}	Output turn off delay			60		75	ns
t_{AH}	Address hold time		60		75		ns
t_{AS}	Address setup time		0		0		ns
t_P	$\overline{CE}$ precharge time		125		150		ns

Notes:

1) A minimum 100 μs time delay is required after the application of V_{CC} (+5V) before propex device operation is achieved. $\overline{CE}$ must be at V_{IH} for this time period.

2) Current is proportional to cycle rate. I_{CC1} is measured at the specified minimum cycle time.