

1Mb (128K x 8) ZEROPOWER SRAM

DATA BRIEFING

- INTEGRATED LOW POWER SRAM, POWER-FAIL CONTROL CIRCUIT and BATTERY
- CONVENTIONAL SRAM OPERATION; UNLIMITED WRITE CYCLES
- 10 YEARS of DATA RETENTION in the ABSENCE of POWER
- AUTOMATIC POWER-FAIL CHIP DESELECT and WRITE PROTECTION
- WRITE PROTECT VOLTAGES (VPFD = Power-fail Deselect Voltage):
 - $M48Z128: 4.50V \le V_{PFD} \le 4.75V$
 - $M48Z128Y: 4.20V \le V_{PFD} \le 4.50V$
- BATTERY INTERNALLY ISOLATED UNTIL POWER IS APPLIED
- PIN and FUNCTION COMPATIBLE with JEDEC STANDARD 128K x 8 SRAMs

PMDIP32 (PM) Module

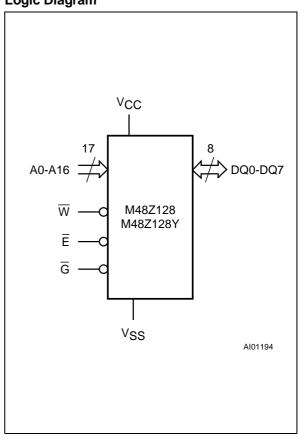
DESCRIPTION

The M48Z128/128Y ZEROPOWER[®] RAM is a non-volatile 1,048,576 bit Static RAM organized as 131,072 words by 8 bits. The device combines an internal lithium battery, a CMOS SRAM and a control circuit in a plastic 32 pin DIP Module.

The ZEROPOWER RAM replaces industry standard SRAMs. It provides the nonvolatility of PROMs without any requirement for special write timing or limitations on the number of writes that can be performed.

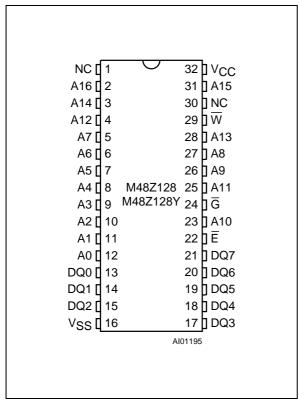
The M48Z128/128Y has its own Power-fail Detect Circuit. The control circuitry constantly monitors the single 5V supply for an out of tolerance condition. When V_{CC} is out of tolerance, the circuit write protects the SRAM, providing a high degree of data security in the midst of unpredictable system operations brought on by low V_{CC} . As V_{CC} falls below approximately 3V, the control circuitry connects the battery which sustains data until valid power returns.

Logic Diagram



B48Z128/801 1/2

DIP Pin Connections



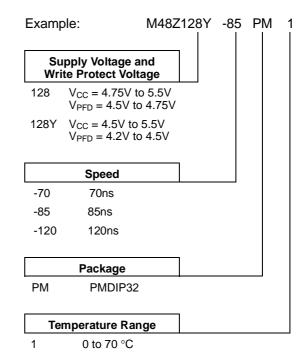
Warning: NC = Not Connected.

Signal Names

| A0-A16 | Address Inputs |
|-----------------|-----------------------|
| DQ0-DQ7 | Data Inputs / Outputs |
| Ē | Chip Enable |
| G | Output Enable |
| W | Write Enable |
| Vcc | Supply Voltage |
| V _{SS} | Ground |

Ordering Information Scheme

For a list of available options or for further information on any aspect of this device, please contact the SGS-THOMSON Sales Office nearest to you.



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