intel®

MILITARY TEMP.

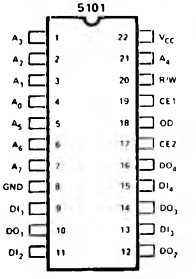
M5101-4, M5101L-4
256 x 4 BIT STATIC CMOS RAM

- **Military Temperature Range: −55°C to +125°C**
- **Ultra Low Standby Current: 200 nA/Bit**
- **Fast Access Time—800ns**
- **Single +5V Power Supply**
- **CE2 Controls Unconditional Standby Mode**
- **Three-State Output**

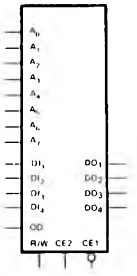
The Intel® M5101 is an ultra-low power 256 X 4 CMOS RAM specified over the −55°C to +125°C temperature range. The RAM uses fully DC stable (static) circuitry and therefore requires no clocks or refreshing to operate. When deselected with CE2 low, the M5101 draws from the single 5-volt supply only 200 microamps at 125°C.

The Intel® M5101 is fabricated with an ion-implanted, silicon gate, Complementary MOS (CMOS) process. This technology allows the design and production of ultra-low power, high performance memories.

PIN CONFIGURATION
5101



LOGIC SYMBOL
5101



PIN NAMES

DI_1 - DI_4 DATA INPUT	OD OUTPUT DISABLE
A_0 - A_7 ADDRESS INPUTS	DO_1 - DO_4 DATA OUTPUT
R/W READ/WRITE INPUT	V_{CC} POWER (+5V)
CE1, CE2 CHIP ENABLE	

Absolute Maximum Ratings *

Ambient Temperature Under Bias . . . -65°C to 135°C
Storage Temperature . . . . . -65°C to +150°C
Voltage On Any Pin
With Respect to Ground . . . . -0.3V to V_{CC} +0.3V
Maximum Power Supply Voltage . . . . . +7.0V
Power Dissipation . . . . . 1 Watt

*COMMENT:

Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D. C. and Operating Characteristics for M5101-4, M5101L-4

T_A = -55°C to 125°C, V_{CC} = 5V ±5% unless otherwise specified.

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
I_{LI}[2]	Input Current		8		nA	V_{IN} = 0 to 5.25V
I_{LOH}[2]	Output High Leakage			2	μA	$\overline{CE1}$=2.2V, V_{OUT} = V_{CC}
I_{LOL}[2]	Output Low Leakage			2	μA	$\overline{CE1}$=2.2V, V_{OUT}=0.0V
I_{CC1}	Operating Current		11	25	mA	V_{IN} = V_{CC} Except $\overline{CE1}$ ≤0.01V Outputs Open
I_{CC2}	Operating Current		20	32	mA	V_{IN} = 2.2V Except $\overline{CE1}$ ≤0.5V Outputs Open
I_{CCL}[2]	Standby Current		2	200	μA	V_{IN} = 0 to V_{CC}, Except CE2 ≤ 0.2V
V_{IL}	Input "Low" Voltage	-0.3		0.5	V	
V_{IH}	Input "High" Voltage	V_{CC}-2.0		V_{CC}	V	
V_{OL}	Output "Low" Voltage			0.4	V	I_{OL} = 2.0mA
V_{OH}	Output "High" Voltage	V_{CC}-2.0			V	I_{OH} = 1.0mA

NOTES: 1. Typical values are T_A = 25°C and nominal supply voltage. 2. Current through all inputs and outputs included in I_{CCL}.

MILITARY TEMP.

Low V_{CC} Data Retention Characteristics (For M5101L-4) T_A = -55°C to 125°C

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions	
V_{DR}	V_{CC} for Data Retention	2.0			V	CE2 ⩽ 0.2V	
I_{CCDR}	Data Retention Current		2	200	μA		V_{DR} = 2.0V
t_{CDR}	Chip Deselect to Data Retention Time	0			ns		
t_R	Operation Recovery Time	t_{RC}[2]			ns		

NOTES: 1. Typical values are T_A = 25°C and nominal supply voltage.
2. t_{RC} = Read Cycle Time.

A.C. Characteristics for M5101-4, M5101L-4

READ CYCLE T_A = -55°C to 125°C, V_{CC} = 5V ±5%, unless otherwise specified.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
t_{RC}	Read Cycle	800			ns	(See below)
t_A	Access Time			800	ns	
t_{CO1}	Chip Enable ($\overline{CE1}$) to Output			700	ns	
t_{CO2}	Chip Enable (CE2) to Output			850	ns	
t_{OD}	Output Disable To Output			350	ns	
t_{DF}	Data Output to High Z State	0		150	ns	
t_{OH1}	Previous Read Data Valid with Respect to Address Change	0			ns	
t_{OH2}	Previous Read Data Valid with Respect to Chip Enable	0			ns	

WRITE CYCLE

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
t_{WC}	Write Cycle	800			ns	(See below)
t_{AW}	Write Delay	150			ns	
t_{CW1}	Chip Enable ($\overline{CE1}$) To Write	550			ns	
t_{CW2}	Chip Enable (CE2) To Write	550			ns	
t_{DW}	Data Setup	400			ns	
t_{DH}	Data Hold	100			ns	
t_{WP}	Write Pulse	400			ns	
t_{WR}	Write Recovery	50			ns	
t_{DS}	Output Disable Setup	150			ns	

A. C. CONDITIONS OF TEST

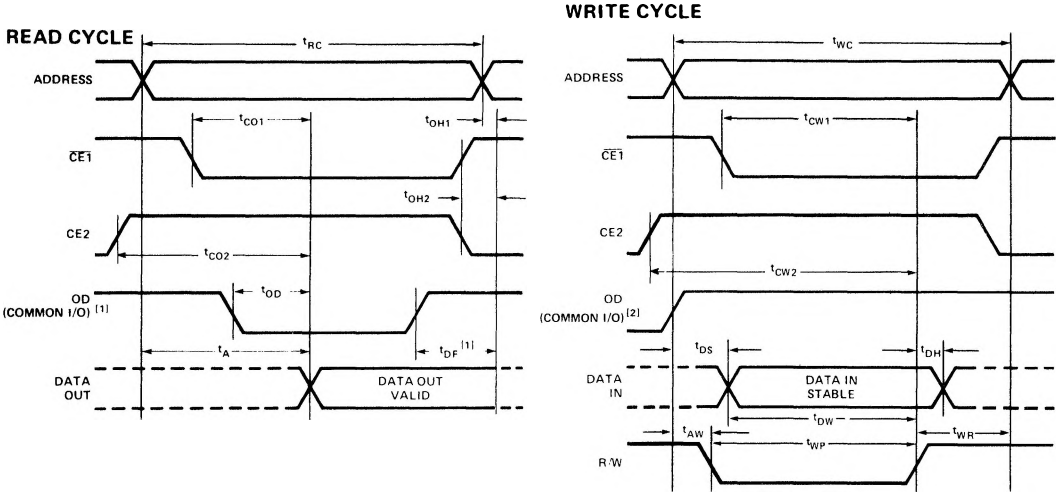
Input Pulse Levels: 0.5 Volt to V_{CC}-2.0 Volt
Input Pulse Rise and Fall Times: 20nsec
Timing Measurement Reference Level: 1.5 Volt
Output Load: 1 TTL Gate and C_L = 100pF

Capacitance[3] T_A = 25°C, f = 1MHz

Symbol	Test	Limits (pF)	
		Typ.	Max.
C_{IN}	Input Capacitance (All Input Pins) V_{IN} = 0V	4	8
C_{OUT}	Output Capacitance V_{OUT} = 0V	8	12

NOTE: 3. This parameter is periodically sampled and is not 100% tested.

Waveforms



NOTES: 1. OD may be tied low for separate I/O operation.
2. During the write cycle, OD is "high" for common I/O and "don't care" for separate I/O operation.

Low V_{CC} Data Retention