M52761SP/FP

PLL-SPLIT VIF/SIF IC

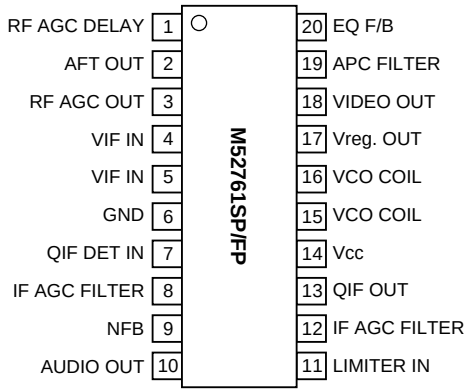
DESCRIPTION

The M52761 is IF signal-processing IC for VCRs and TVs. It enable the PLL detection system despite size as small as that of conventional quasi-synchronous VIF/SIF detector, IF/RF AGC, SIF limiter, FM detector, QIF AGC and EQ AMP.

FEATURES

- Video detection output is $2V_{P-P}$. It has built-in EQ AMP.
- The video detector uses PLL for full synchronous detection circuit. It produces excellent characteristics of DG, DP, 920kHz beat, and cross color.
- Dynamic AGC realizes high speed response with double filter.
- Video IF and sound IF signal processings are separated from each other. VCO output is used to obtain intercarrier. This PLL-SPLIT method and built-in QIF AGC provide good sound sensitivity and reduces buzz.
- As AFT output voltage uses the APC output voltage, VCO coil is not used.
- Audio FM demodulation uses PLL system, so it has wide frequency range with no external parts and no adjustment.
- This IC corresponds to only NTSC system.

PIN CONFIGURATION (TOP VIEW)



Outline 20P4B (SP)
20P2N-A (FP)

APPLICATION

TV sets, VCR tuners

RECOMMENDED OPERATING CONDITION

In case of Vcc and Vreg. out short

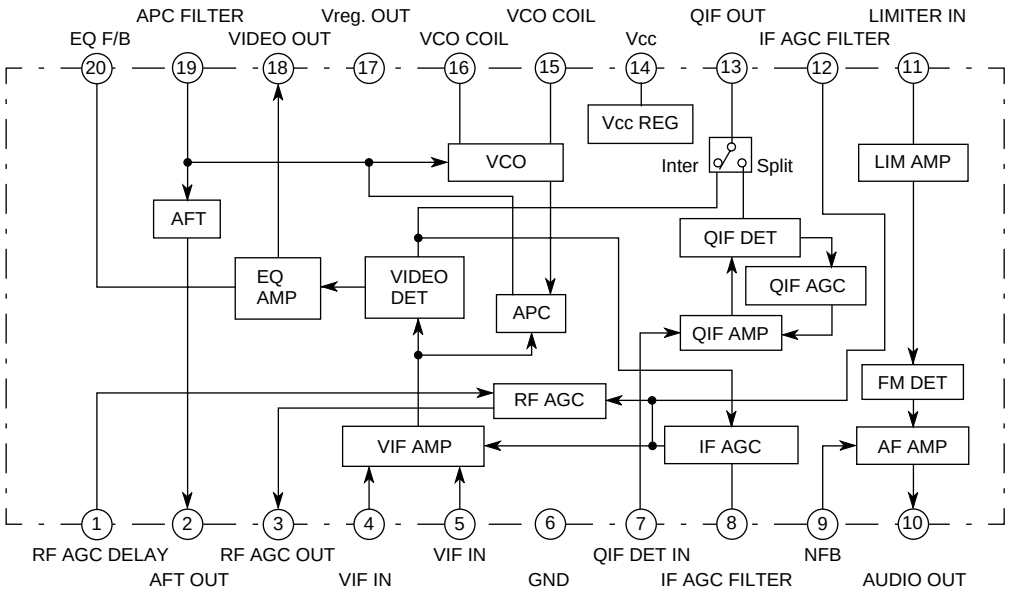
Supply voltage range.....4.75 to 5.25V

Recommended supply voltage.....5.0V

In case of Vreg. out open

Supply voltage range.....8.5 to 12.5V

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Ta=25°C, unless otherwise noted)

Symbol	Parameter	Ratings	Unit	Note
V_{CC}	Supply voltage1	10.5	V	V_{CC} and Vreg. out is not connected to each other
Vreg. OUT	Supply voltage Vreg. OUT	6	V	V_{CC} and Vreg. out is not connected to each other
P_d	Power dissipation	1225	mW	
T_{opr}	Operating temperature	-20 to +85	°C	
T_{stg}	Storage temperature	-40 to +150	°C	
Surge	Surge voltage resistance	±200	V	surge protection capacitance 200pF resistance 0Ω

ELECTRICAL CHARACTERISTICS (V_{CC}=9V, Ta=25°C, unless otherwise noted)

Symbol	Parameter	Test circuit	Test point	Input point	Input SG	Measurement condition	Limits			Unit
						switches set to position 1 unless otherwise indicated	Min.	Typ.	Max.	
VIF section										
V17	Vreg voltage	1	TP17	–	–	SW17=2	4.7	5.0	5.3	V
I_{CC1}	Circuit current	1	A	VIF IN	SG1	SW14=2	31	46	61	mA
V18	Video output DC Voltage	1	TP18A	–	–	SW18=2, V8=0V	3.4	3.7	4.1	V
Vo det	Video output voltage	1	TP18A	VIF IN	SG1		1.8	2.1	2.5	V_{P-P}
Video S/N	Video S/N	1	TP18B	VIF IN	SG2	SW18=2	49	53	–	dB
BW	Video band width	1	TP18A	VIF IN	SG3	SW8=2, V8=variable	7.0	9.0	–	MHz
VIN MIN	Input sensitivity	1	TP18A	VIF IN	SG4		–	48	52	dBμ
VIN MAX	Maximum allowable input	1	TP18A	VIF IN	SG5		101	105	–	dBμ
GR	AGC control range Input	–	–	–	–		50	57	–	dB
V8	IF AGC voltage	1	TP8	VIF IN	SG6		2.6	2.9	3.2	V
V8H	Maximum IF AGC voltage	1	TP8	–	–		4.4	4.8	–	V
V8L	Minimum IF AGC voltage	1	TP8	VIF IN	SG7		2.2	2.4	2.6	V
V3H	Maximum RF AGC voltage	1	TP3	VIF IN	SG6		8.0	8.9	–	V
V3L	Minimum RF AGC voltage	1	TP3	VIF IN	SG7		–	0.2	0.7	V
V3	RF AGC Operation voltage	1	TP3	VIF IN	SG8		89	92	95	dBμ
CL-U	Capture range U	1	TP18A	VIF IN	SG9		0.9	1.7	–	MHz
CL-L	Capture range L	1	TP18A	VIF IN	SG9		1.7	2.4	–	MHz
CL-T	Capture range T	1	–	–	–		3.1	4.1	–	MHz
VCO Δf	VCO SW ON Drift	1	TP18A	VIF IN	SG2	SW8=2, V8=0V	±0	+20	+40	kHz
μ	AFT sensitivity	1	TP2	VIF IN	SG10		20	30	60	mV/kHz
V2H	AFT maximum voltage	1	TP2	VIF IN	SG10		7.7	8.1	–	V
V2L	AFT minimum voltage	1	TP2	VIF IN	SG10		–	0.7	1.2	V
IM	Inter modulation	1	TP18A	VIF IN	SG11	SW8=2, V8=variable	35	40	–	dB
DG	Differential gain	1	TP18A	VIF IN	SG12		–	2	5	%
DP	Differential phase	1	TP18A	VIF IN	SG12		–	2	5	deg
V18 SYNC	Sync. tip level	1	TP18A	VIF IN	SG2		0.85	1.15	1.45	V
RINV	VIF input resister	2	TP4	–	–		0.7	1.2	1.65	kΩ
CINV	VIF input capacitance	2	TP4	–	–		–	5	10	pF

ELECTRICAL CHARACTERISTICS (cont.)

Symbol	Parameter	Test circuit	Test point	Input point	Input SG	Measurement condition switches set to position 1 unless otherwise indicated	Limits Min.	Limits Typ.	Limits Max.	Unit
SIF section										
QIF1	QIF detection output amplitude 1	1	TP13	VIF IN QIF IN	SG2 SG13		94	100	106	dBμ
QIF2	QIF detection output amplitude 2	1	TP13	VIF IN QIF IN	SG2 SG14		94	100	106	dBμ
Vos	SIF detection output amplitude	1	TP13	VIF IN	SG15	SW7=2, V7=0V	94	100	106	dBμ
V1	AF output DC voltage	1	TP10	SIF IN	SG19	SW8=2, V8=0V	1.7	2.3	2.9	V
VoAF1	AF output	1	TP10	SIF IN	SG16	SW8=2, V8=0V	400	560	800	mVrms
THD AF1	AF output distortion	1	TP10	SIF IN	SG16	SW8=2, V8=0V	–	0.2	0.9	%
LIM1	Limiting sensitivity	1	TP10	SIF IN	SG17	SW8=2, V8=0V	–	42	55	dBμ
AMR1	AM rejection	1	TP10	SIF IN	SG18	SW8=2, V8=0V	55	62	–	dB
AF S/N 1	AF S/N	1	TP10	SIF IN	SG19	SW8=2, V8=0V	55	62	–	dB
RINS	SIF input resister	2	TP7	–	–		0.9	1.5	2.1	kΩ
CINS	SIF input capacitance	2	TP7	–	–		–	4	8	pF
Control section										
C_{QIF}	QIF control	1	TP7	–	–	SW7=2, V7=variable	–	0.7	1.0	V

ELECTRICAL CHARACTERISTICS TEST METHOD

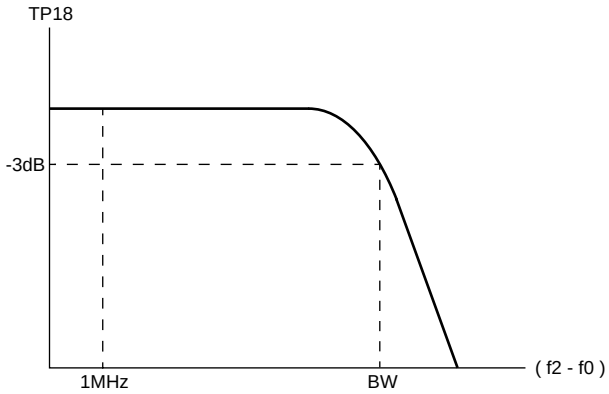
Video S/N

Input SG2 into VIF IN and measure the video out (Pin 18) noise in r.m.s at TP18B through a 5MHz (-3dB) L.P.F.

$$S/N=20 \log \left(\frac{0.7 \times Vo\ det}{NOISE} \right) (dB)$$

BW Video band width

1. Measure the 1MHz component level of EQ output TP18A with a spectrum analyzer when SG3 (f2=57.75MHz) is input into VIF IN. At that time, measure the voltage at TP8 with SW8, set to position 2, and then fix V8 at that voltage.
2. Reduce f2 and measure the value of (f2-f0) when the (f2-f0) component level reaches -3dB from the 1MHz component level as shown below.



VIN MIN Input sensitivity

Input SG4 (Vi=90dBμ) into VIF IN, and then gradually reduce Vi and measure the input level when the 20kHz component of EQ output TP18A reaches -3dB from Vo det level.

VIN MAX Maximum allowable input

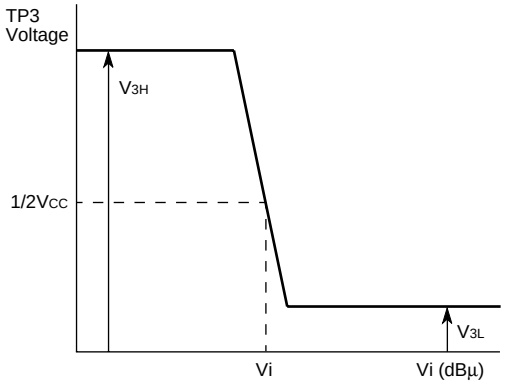
1. Input SG5 (Vi=90dBμ) into VIF IN, and measure the level of the 20kHz component of EQ output.
2. Gradually increase the Vi of SG and measure the input level when the output reaches -3dB.

GR AGC Control range

GR=VIN MAX-VIN MIN (dB)

V3 RF AGC operating voltage

Input SG8 into VIF IN and gradually reduce Vi and then measure the input level when RF AGC output TP3 reaches 1/2 V_{CC}, as shown below.



CL-U Capture range

1. Increase the frequency of SG9 until the VCO is out of locked-oscillation.
2. Decrease the frequency of SG9 and measure the frequency fU when the VCO locks.

CL-U=fU-58.75 (MHz)

CL-L Capture range

1. Decrease the frequency of SG9 until the VCO is out of locked-oscillation.
2. Increase the frequency of SG9 and measure the frequency fL when the VCO locks.

CL-L=58.75-fL (MHz)

CL-T Capture range

CL-T=CL-U+CL-L (MHz)

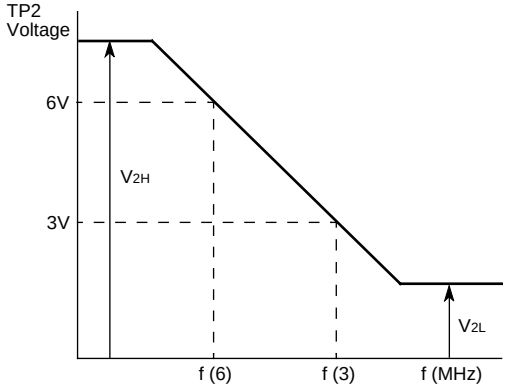
VCO ∆f VCO SW on drift

1. Input SG2 into VIF IN .
2. Turn on SW14 (Vcc), and adjust VCO coil so that AFT OUT voltage TP2 equal 1/2 Vcc in 10 seconds.
3. Put VIF IN input in a non-input state and ground AGC filter at TP8.
4. Measure the VCO free-run frequency 10 seconds after SW ON (f1), and one minutes after (f2).

VCO ∆f (kHz) =f2 (MHz) -f1 (MHz)

μ AFT sensitivity, V_{2H} Maximum AFT voltage, V_{2L} Minimum AFT voltage

1. Input SG10 into VIF IN , and set the frequency of SG10 so that the voltage of AFT output TP19 is 6V. This frequency is named f (6).
2. Set the frequency of SG10 so that the AFT output voltage is 3V. This frequency is named f (3)
3. IN the graph, maximum and minimum DC voltage are V_{2H} and V_{2L}, respectively.



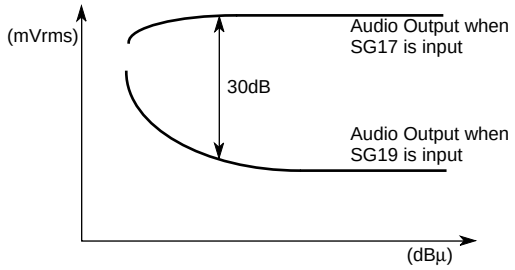
$$\mu = \frac{1000\ (mV)}{f\ (3) - f\ (6)\ (kHz)} (mV/kHz)$$

IM Intermodulation

1. Input SG11 into VIF IN, and measure EQ output TP18A with an oscilloscope.
2. Adjust AGC filter voltage V8 so that the minimum DC level of the output waveform is 1.0V.
3. At this time, measure TP18A with a spectrum analyzer . The intermodulation is defined as a difference between 0.92MHz and 3.58MHz frequency components.

LIM Limiting sensitivity

1. Input SG17 (Vi=90dBμ) into SIF input, and measure the 400Hz component level of AF output TP10.
2. Input SG19 (Vi=90dBμ) into SIF input, and measure the 400Hz component level of AF output TP10.
3. Measure the input level of SG17 and SG19 when a ratio of the two VoAF level is 30dB. This input level is named $V_{IN\ MIN}$.



AMR AM rejection

1. Input SG18 into SIF input, and measure the output level of AF output TP10. This level is named VAM.
2. AMR is;

$$AMR=20\log\left(\frac{VoAF\ (mVr.m.s)}{VAM\ (mVr.m.s)}\right)(dB)$$

AF S/N

1. Input SG19 into SIF input, and measure the output noise level of AF output TP10. This level is named VN.
2. S/N is;

$$S/N=20\log\left(\frac{VoAF\ (mVr.m.s)}{VN\ (mVr.m.s)}\right)(dB)$$

C_{QIF} QIF control

Decrease the voltage of V7, and measure V7 when the DC voltage of TP13 changes.

THE NOTE IN THE SYSTEM SETUP

M52761FP has 2 power supply pins of Vcc (pin 14) and Vreg.OUT (pin 17) .

Pin 14 is for AFT output, RF AGC output circuits and 5V regulated power supply circuit and Pin 17 is for the other circuit blocks.

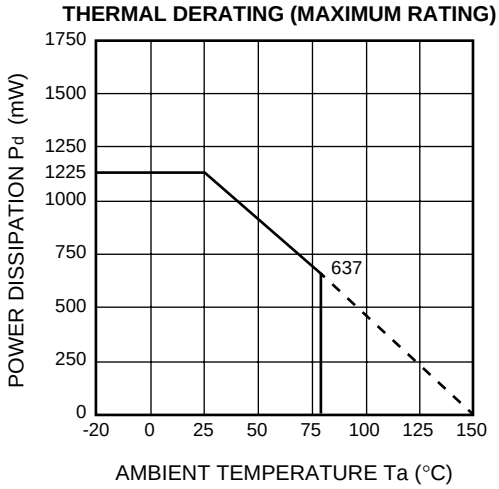
In case M52761FP is used together with other ICs like VIF operating at more than 5V, the same supply voltage as that of connected ICs is applied to Vcc and Vreg.Out is opened. The other circuit blocks, connected to Vreg.OUT are powered by internal 5V regulated power supply.

In case the connecting ICs are operated at 5V, 5V is supplied to both Vcc and Vreg.OUT.

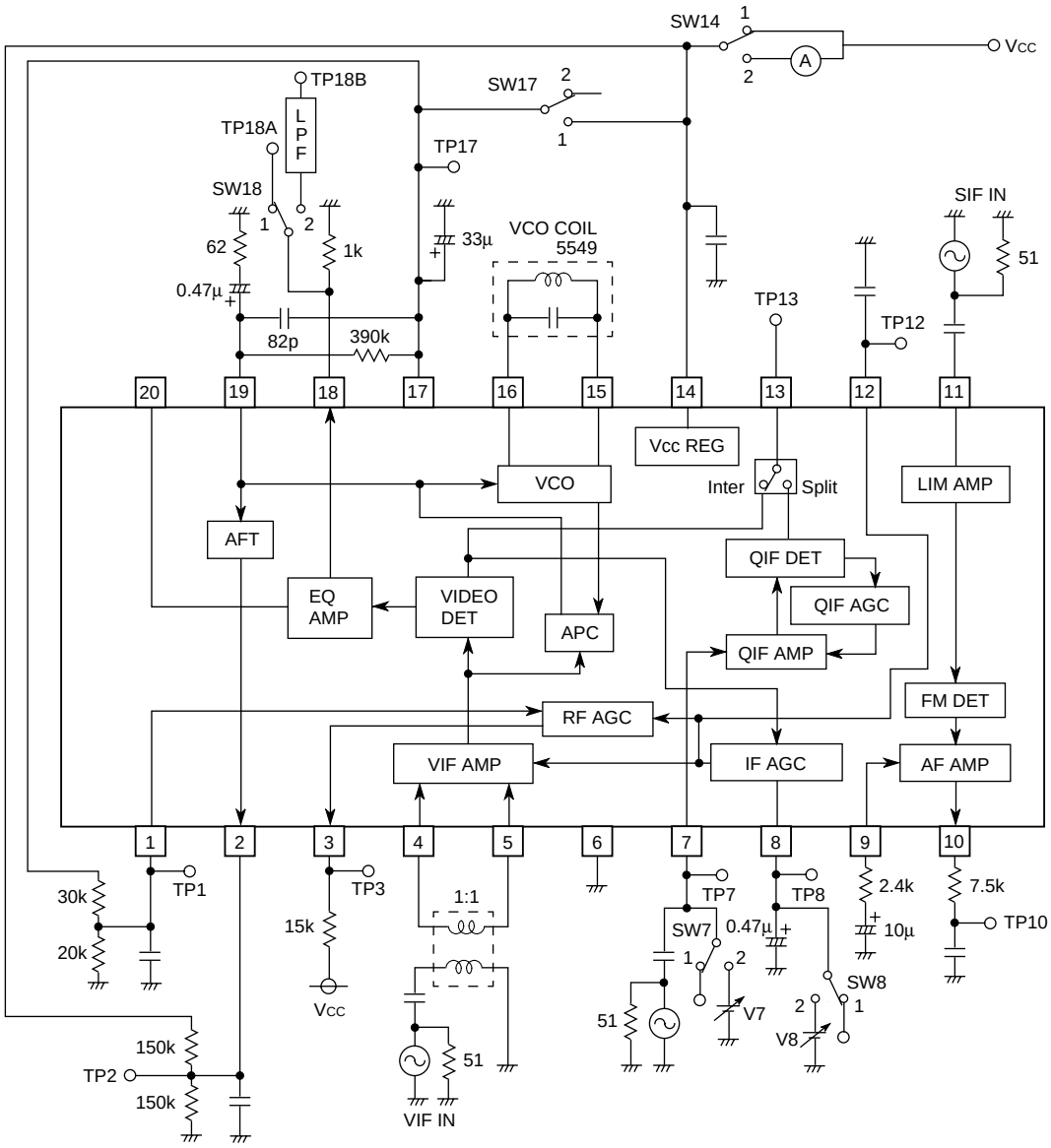
INPUT SIGNAL

SG No.	Signals (50Ω termination)
1	f_0=58.75MHz AM20kHz 77.8% 90dBμ
2	f_0=58.75MHz 90dBμ CW
3	f_0=58.75MHz 90dBμ CW (Mixed signal) f_2=Frequency variable 70dBμ CW (Mixed signal)
4	f_0=58.75MHz AM20kHz 77.8% level variable
5	f_0=58.75MHz AM20kHz 14.0% level variable
6	f_0=58.75MHz 80dBμ CW
7	f_0=58.75MHz 110dBμ CW
8	f_0=58.75MHz CW level variable
9	f_0=Variable AM20kHz 77.8% 90dBμ
10	f_0=Variable 90dBμ CW
11	f_1=58.75MHz 90dBμ CW (Mixed signal) f_2=55.17MHz 80dBμ CW (Mixed signal) f_3=54.25MHz 80dBμ CW (Mixed signal)
12	f_0=58.75MHz 87.5% TM modulation ten-step waveform sync tip level 90dBμ
13	f_1=54.25MHz 95dBμ CW
14	f_1=54.25MHz 75dBμ CW
15	f_1=58.75MHz 90dBμ CW (Mixed signal) f_2=54.25MHz 70dBμ CW (Mixed signal)
16	f_0=4.5MHz 90dBμ FM400Hz±25kHz dev
17	f_0=4.5MHz level variable FM400Hz±25kHz dev
18	f_0=4.5MHz 90dBμ AM400Hz 30%
19	f_0=4.5MHz 90dBμ CW

TYPICAL CHARACTERISTICS



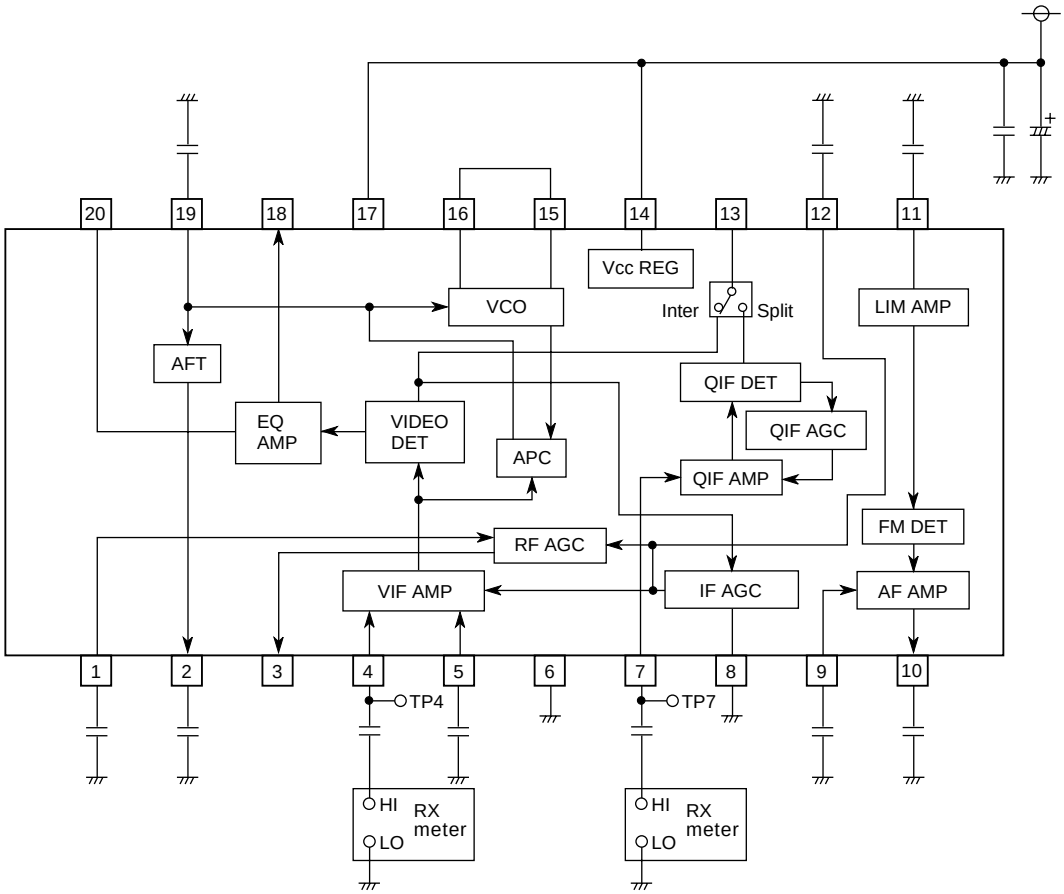
APPLICATION EXAMPLE 1



∗ All capacitor is 0.01µF, unless otherwise specified.
∗ The Measuring Circuit 1 is Mitsubishi standard evaluation fixture.

Units Resistance : Ω
Capacitance : F

APPLICATION EXAMPLE 2



∗ All capacitor is 0.01μF, unless otherwise specified.