LED DISPLAY DRIVERS

- M5450 34 OUTPUTS/15mA SINK
- M5451 35 OUTPUTS/15mA SINK
- CURRENT GENERATOR OUTPUTS (NO EXTERNAL RESISTORS REQUIRED)
- CONTINUOUS BRIGHTNESS CONTROL
- SERIAL DATA INPUT
- ENABLE (ON M5450)
- WIDE SUPPLY VOLTAGE OPERATION
- TTL COMPATIBILITY

Application examples:

- MICROPROCESSOR DISPLAYS
- INDUSTRIAL CONTROL INDICATOR
- RELAY DRIVER
- INSTRUMENTATION READOUTS

The M5450 and M5451 are monolithic MOS integrated circuits produced with an N-channel silicon gate technology. They are available in 40-pin dual in-line plastic packages.

A single pin controls the LED display brightness by setting a reference current through a variable resistor connected to V_{DD} or to a separate supply of 13.2V maximum.

The M5450 and M5451 are pin-to-pin replacements of the NS MM 5450 and MM 5451.
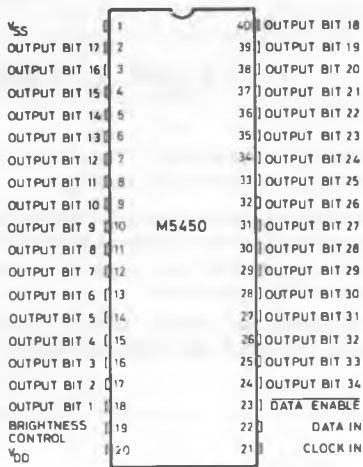

DIP-40 Plastic

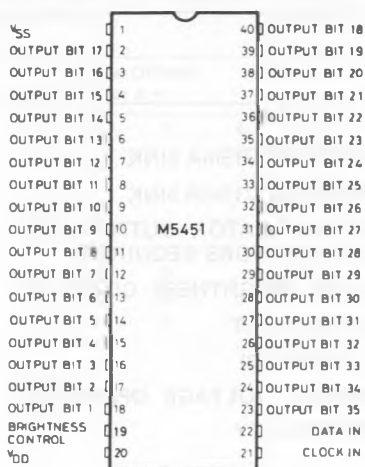**ORDERING NUMBERS:** M5450 B7
M5451 B7
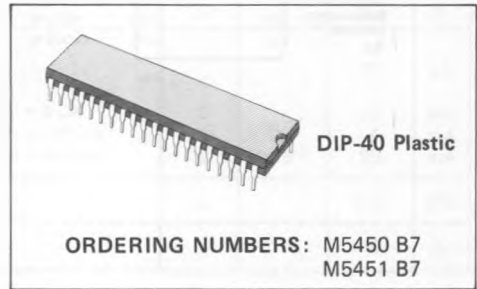
ABSOLUTE MAXIMUM RATINGS

V_{DD}	Supply voltage	–0.3 to 15	V
V_I	Input voltage	–0.3 to 15	V
$V_{O (off)}$	Off state output voltage	15	V
I_O	Output sink current	40	mA
P_{tot}	Total package power dissipation	at 25°C	1W
		at 85°C	560 mW
T_j	Junction temperature	150	°C
T_{op}	Operating temperature range	–25 to 85	°C
T_{stg}	Storage temperature range	–65 to 150	°C

Stresses above those listed under "Absolute Maximum Ratings" may causes permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
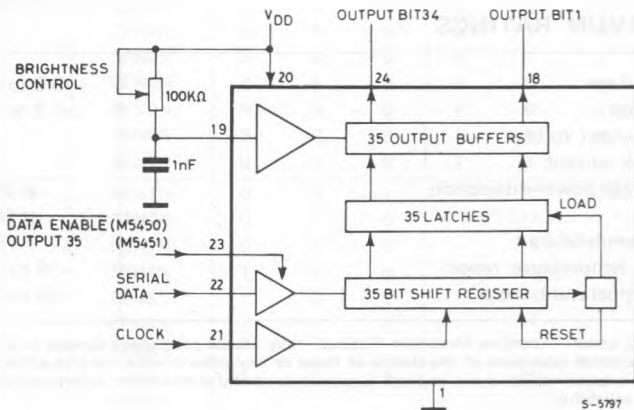
CONNECTION DIAGRAMS

	M5450	
Vss ▯ 1		40 ▯ OUTPUT BIT 18
OUTPUT BIT 17 ▯ 2		39 ▯ OUTPUT BIT 19
OUTPUT BIT 16 ▯ 3		38 ▯ OUTPUT BIT 20
OUTPUT BIT 15 ▯ 4		37 ▯ OUTPUT BIT 21
OUTPUT BIT 14 ▯ 5		36 ▯ OUTPUT BIT 22
OUTPUT BIT 13 ▯ 6		35 ▯ OUTPUT BIT 23
OUTPUT BIT 12 ▯ 7		34 ▯ OUTPUT BIT 24
OUTPUT BIT 11 ▯ 8		33 ▯ OUTPUT BIT 25
OUTPUT BIT 10 ▯ 9		32 ▯ OUTPUT BIT 26
OUTPUT BIT 9 ▯ 10	M5450	31 ▯ OUTPUT BIT 27
OUTPUT BIT 8 ▯ 11		30 ▯ OUTPUT BIT 28
OUTPUT BIT 7 ▯ 12		29 ▯ OUTPUT BIT 29
OUTPUT BIT 6 ▯ 13		28 ▯ OUTPUT BIT 30
OUTPUT BIT 5 ▯ 14		27 ▯ OUTPUT BIT 31
OUTPUT BIT 4 ▯ 15		26 ▯ OUTPUT BIT 32
OUTPUT BIT 3 ▯ 16		25 ▯ OUTPUT BIT 33
OUTPUT BIT 2 ▯ 17		24 ▯ OUTPUT BIT 34
OUTPUT BIT 1 ▯ 18		23 ▯ DATA ENABLE
BRIGHTNESS CONTROL ▯ 19		22 ▯ DATA IN
VDD ▯ 20		21 ▯ CLOCK IN

S-5795

	M5451	
Vss ▯ 1		40 ▯ OUTPUT BIT 18
OUTPUT BIT 17 ▯ 2		39 ▯ OUTPUT BIT 19
OUTPUT BIT 16 ▯ 3		38 ▯ OUTPUT BIT 20
OUTPUT BIT 15 ▯ 4		37 ▯ OUTPUT BIT 21
OUTPUT BIT 14 ▯ 5		36 ▯ OUTPUT BIT 22
OUTPUT BIT 13 ▯ 6		35 ▯ OUTPUT BIT 23
OUTPUT BIT 12 ▯ 7		34 ▯ OUTPUT BIT 24
OUTPUT BIT 11 ▯ 8		33 ▯ OUTPUT BIT 25
OUTPUT BIT 10 ▯ 9		32 ▯ OUTPUT BIT 26
OUTPUT BIT 9 ▯ 10	M5451	31 ▯ OUTPUT BIT 27
OUTPUT BIT 8 ▯ 11		30 ▯ OUTPUT BIT 28
OUTPUT BIT 7 ▯ 12		29 ▯ OUTPUT BIT 29
OUTPUT BIT 6 ▯ 13		28 ▯ OUTPUT BIT 30
OUTPUT BIT 5 ▯ 14		27 ▯ OUTPUT BIT 31
OUTPUT BIT 4 ▯ 15		26 ▯ OUTPUT BIT 32
OUTPUT BIT 3 ▯ 16		25 ▯ OUTPUT BIT 33
OUTPUT BIT 2 ▯ 17		24 ▯ OUTPUT BIT 34
OUTPUT BIT 1 ▯ 18		23 ▯ OUTPUT BIT 35
BRIGHTNESS CONTROL ▯ 19		22 ▯ DATA IN
VDD ▯ 20		21 ▯ CLOCK IN

S-5796

BLOCK DIAGRAM
Fig. 1

SGS-THOMSON MICROELECTRONICS

STATIC ELECTRICAL CHARACTERISTICS (T_{amb} within operating range, V_{DD} = 4.75V to 13.2V, V_{SS} = 0V, unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage		4.75		13.2	V
I_{DD}	Supply Current	V_{DD} = 13.2V			7	mA
V_I	Input Voltage Logical "0" Level Logical "1" Level	± 10 μA input bias 4.75 ⩽ V_{DD} ⩽ 5.25 V_{DD} > 5.25	-0.3 2.2 V_{DD}-2		0.8 V_{DD} V_{DD}	V V V
I_B	Brightness Input Current (note 2)		0		0.75	mA
V_B	Brightness Input Voltage (pin 19)	Input current = 750 μA	3		4.3	V
$V_{O(off)}$	Off State Out. Voltage				13.2	V

I_O	Out. Sink Current (note 3)
	Segment OFF
	Segment ON
		V_O = 3V
		V_O = 1V (note 4)
		  Brightness In. = 0 μA
		  Brightness In. = 100 μA
		  Brightness In. = 750 μA
			
			0
			2
			12
				
				2.7
				15
					10
					
					10
					4
					25
						μA
						
						μA
						mA
						mA

f_{clock}	Input Clock Frequency		0		0.5	MHz
I_O	Output Matching (note 1)				± 20	%

Notes : 1. Output matching is calculated as the percent variation from I_{MAX} + I_{MIN}/2.

2. With a fixed resistor on the brightness input some variation in brightness will occur from one device to another.

3. Absolute maximum for each output should be limited to 40 mA.

4. The V_O voltage should be regulated by the user. See figures 5 and 6 for allowable V_O versus I_O operation.

FUNCTIONAL DESCRIPTION

Both the M5450 and the M5451 are specifically designed to operate 4 or 5-digit alphanumeric displays with minimal interface with the display and the data source. Serial data transfer from the data source to the display driver is accomplished with 2 signals, serial data and clock. Using a format of a leading "1" followed by the 35 data bits allows data transfer without an additional load signal. The 35 data bits are latched after the 36th bit is complete, thus providing non-multiplexed, direct drive to the display.
Outputs change only if the serial data bits differ from the previous time.
Display brightness is determined by control of the output current LED displays.
A 1nF capacitor should be connected to brightness control, pin 19, to prevent possible oscillations.
A block diagram is shown in figure 1. For the M5450 a DATA ENABLE is used instead of the 35th output. The DATA ENABLE input is a metal option for the M5450.

SGS-THOMSON
MICROELECTRONICS

FUNCTIONAL DESCRIPTION (continued)

The output current is typically 20 times greater than the current into pin 19, which is set by an external variable resistor. There is an internal limiting resistor of 400Ω nominal value.

Figure 2 shows the input data format. A start bit of logical "1" precedes the 35 bits of data. At the 36th clock a LOAD signal is generated synchronously with the high state of the clock, which loads the 35 bits of the shift registers into the latches.

At the low state of the clock a RESET signal is generated which clears all the shift registers for the next set of data. The shift registers are static master-slave configurations. There is no clear for the master portion of the first shift register, thus allowing continuous operation.

There must be a complete set of 36 clocks or the shift registers will not clear.

When power is first applied to the chip an internal power ON reset signal is generated which resets all registers and all latches. The START bit and the first clock return the chip to its normal operation.

Bit 1 is the first bit following the start bit and it will appear on pin 18. A logical "1" at the input will turn on the appropriate LED.
Figure 3 shows the timing relationship between Data, Clock and $\overline{\text{DATA ENABLE}}$.
A max clock frequency of 0.5 MHz is assumed.

For applications where a lesser number of outputs are used, it is possible to either increase the current per output or operate the part at higher than 1V V_{OUT}.
The following equation can be used for calculations.

$$T_j = [(V_{OUT}) (I_{LED}) (\text{No. of segments}) + (V_{DD} \cdot 7 \text{ mA})] (124\,°C/W) + T_{amb}$$

where:

T_j = junction temperature (150°C max)

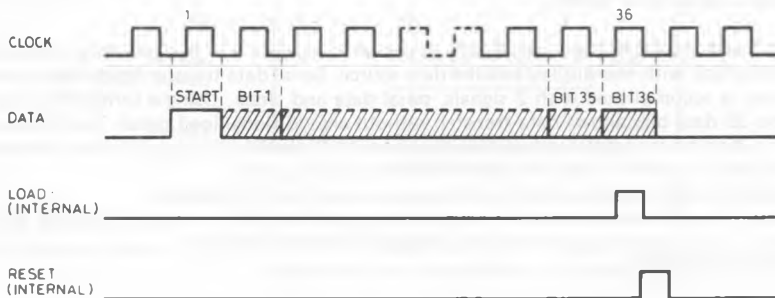V_{OUT} = the voltage at the LED driver outputs

I_{LED} = the LED current

124°C/W = thermal coefficient of the package

T_{amb} = ambient temperature

The above equation was used to plot figure 4, 5 and 6.
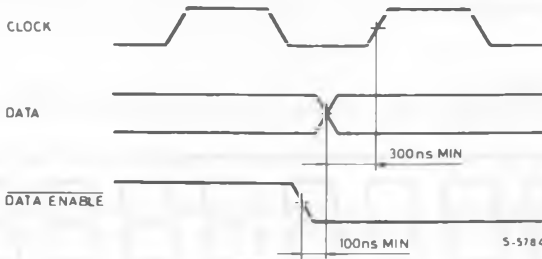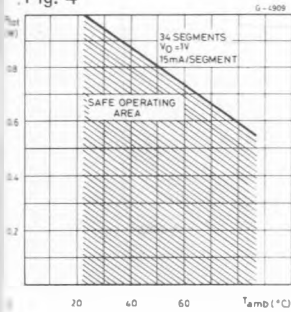
Fig. 2 - Input Data Format

S-5827/1

SGS-THOMSON
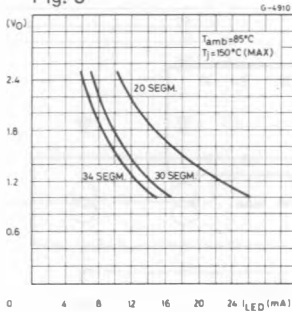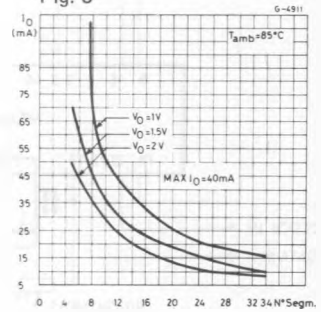MICROELECTRONICS

Fig. 3

Fig. 4
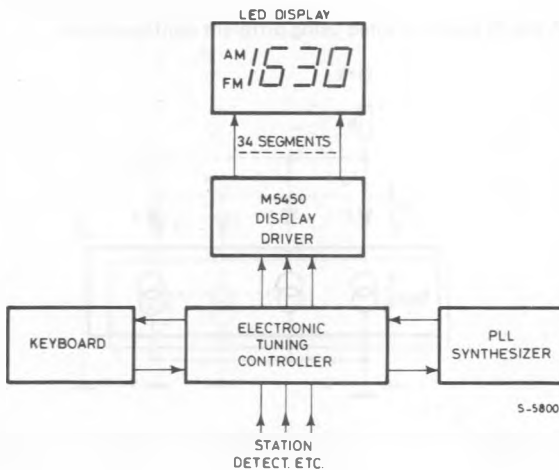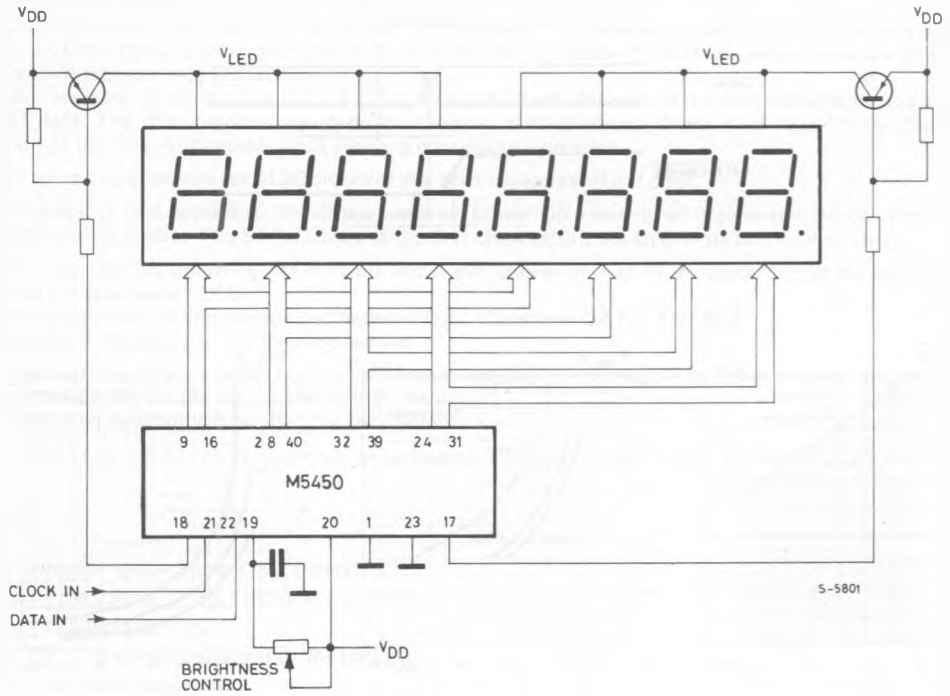

Fig. 5

Fig. 6

TYPICAL APPLICATIONS

Basic electronically tuned Radio or TV system
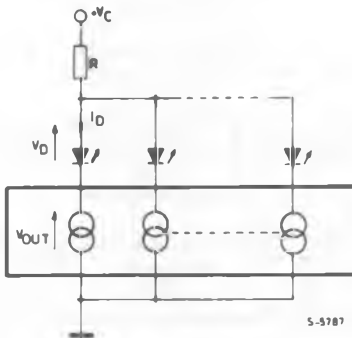
TYPICAL APPLICATIONS (continued)

Duplexing 8 Digits with One M5450

POWER DISSIPATION OF THE IC

The power dissipation of the IC can be limited using different configurations.

a)

SGS-THOMSON
MICROELECTRONICS

In this application R must be chosen taking into account the worst operating conditions.
R is determined by the maximum number of segments activated

$$R = \frac{V_C - V_{D\ MAX} - V_{O\ MIN}}{N_{MAX} \cdot I_D}$$

The worst case condition for the device is when roughly half of the maximum number of segments are activated.
It must be checked that the total power dissipation does not exceed the absolute maximum ratings of the device.
In critical cases more resistors can be used in conjunction with groups of segments.
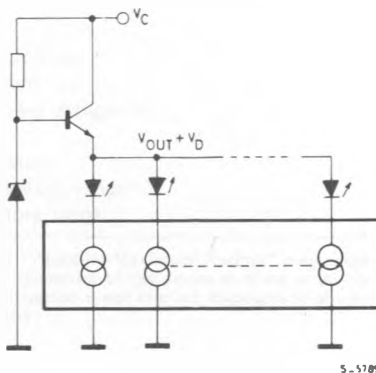In this case the current variation in the single resistor is reduced and P_{tot} limited.

b)

S-5788
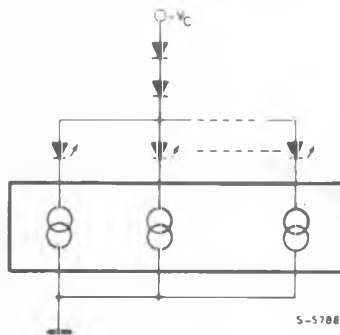
In this configuration the drop on the serial connected diodes is quite stable if the diodes are properly chosen.
The total power dissipation of the IC depends, in a first approximation, only on the number of segments activated.

c)

S-5789

In this configuration $V_{OUT} + V_D$ is constant. The total power dissipation of the IC depends only on the number of segments activated.