SGS-THOMSON MICROELECTRONICS

M54HC113
M74HC113

DUAL J-K FLIP FLOP WITH PRESET

- HIGH SPEED
  f_{MAX} = 64 MHz (Typ.) at V_{CC} = 5V
- LOW POWER DISSIPATION
  I_{CC} = 2 μA at T_A = 25°C
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28% V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2 to 6V
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS113

B1N
Plastic Package

F1
Ceramic Frit Seal Package

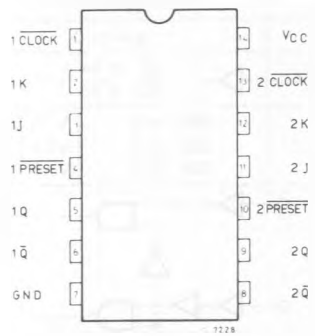
M1
Micro Package

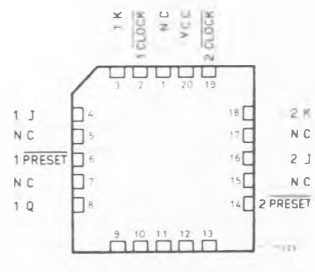
C1
Plastic Chip Carrier

ORDERING NUMBERS:

M54HC113 F1
M74HC113 B1N
M74HC113 F1
M74HC113 C1
M74HC113 M1

PIN CONNECTIONS (top view)





NC = No Internal Connection

DESCRIPTION

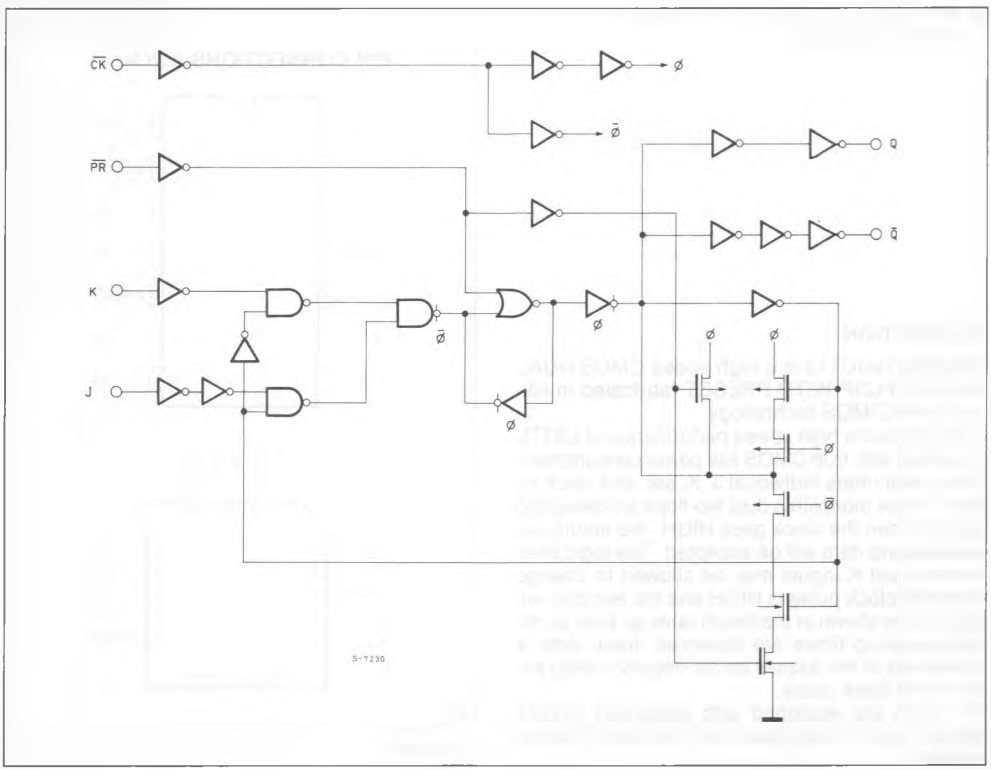
The M54/74HC113 is a high speed CMOS DUAL J-K FLIP FLOP WITH PRESET fabricated in silicon gate C²MOS technology.
It has the same high speed performance of LSTTL combined with true CMOS low power consumption. This circuit offers individual J, K, set, and clock inputs. These monolithic dual flip-flops are designed so that when the clock goes HIGH, the inputs are enabled and data will be accepted. The logic level of the J and K inputs may be allowed to change when the clock pulse is HIGH and the bistable will function as shown in the thruth table as long as minimum set-up times are observed. Input data is transferred to the outputs on the negative-going edge of the clock pulse.
All inputs are equipped with protection circuits against static discharge and transient excess voltage.

TRUTH TABLE

INPUTS				OUTPUT		FUNCTION
$\overline{PR}$	J	K	$\overline{CK}$	Q	$\overline{Q}$	
L	X	X	X	H	L	PRESET
H	L	L	↓	Qn	$\overline{Qn}$	NO CHANGE
H	L	H	↓	L	H	
H	H	L	↓	H	L	
H	H	H	↓	$\overline{Qn}$	Qn	TOGGLE
H	X	X	↑	Qn	$\overline{Qn}$	NO CHANGE

X: DON'T CARE

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to 7	V
V_I	DC Input Voltage	−0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	−0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	−65 to 150	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

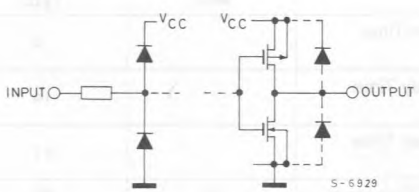
(*) 500 mW = 65° derate to 10 mW/°C from 65°C to 85°C for plastic package

(*) 500 mW = 65° derate to 12 mW/°C from 100 to 125°C for frit-seal package

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value		Unit
V_{CC}	Supply Voltage		2 to 6		V
V_I	Input Voltage		0 to V_{CC}		V
V_O	Output Voltage		0 to V_{CC}		V
T_A	Operating Temperature	74HC Series 54HC Series	−40 to 85 −55 to 125		°C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V V_{CC} = 4.5V V_{CC} = 6 V	0 to 1000 0 to 500 0 to 400		ns

INPUT AND OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	V_{CC}	Test Condition		$T_A = 25°C$ 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0 4.5 6.0			1.5 3.15 4.2	— — —	— — —	1.5 3.15 4.2	— — —	1.5 3.15 4.2	— — —	V
V_{IL}	Low Level Input Voltage	2.0 4.5 6.0			— — —	— — —	0.5 1.35 1.8	— — —	0.5 1.35 1.8	— — —	0.5 1.35 1.8	V
V_{OH}	High Level Output Voltage	2.0 4.5 6.0 4.5 6.0	V_I V_{IH} or V_{IL}	I_O − 20 μA − 4.0 mA − 5.2 mA	1.9 4.4 5.9 4.18 5.68	2.0 4.5 6.0 4.31 5.8	— — — — —	1.9 4.4 5.9 4.13 5.63	— — — — —	1.9 4.4 5.9 4.10 5.60	— — — — —	V
V_{OL}	Low Level Output Voltage	2.0 4.5 6.0 4.5 6.0	V_{IH} or V_{IL}	20 μA 4.0 mA 5.2 mA	— — — — —	0.0 0.0 0.0 0.17 0.18	0.1 0.1 0.1 0.26 0.26	— — — — —	0.1 0.1 0.1 0.33 0.33	— — — — —	0.1 0.1 0.1 0.40 0.40	V
I_I	Input Leakage Current	6.0	$V_I = V_{CC}$ or GND		—	—	±0.1	—	±1.0	—	±1.0	μA
I_{CC}	Quiescent Supply Current	6.0	$V_I = V_{CC}$ or GND		—	—	2	—	20	—	40	μA

AC ELECTRICAL CHARACTERISTICS ($V_{CC} = 5V$, $T_A = 25°C$, $C_L = 15pF$, Input $t_r = t_f = 6ns$)

Symbol	Parameter	54HC and 74HC			Unit
		Min.	Typ.	Max.	
t_{TLH} t_{THL}	Output Transition Time		4	8	ns
t_{PLH} t_{PHL}	Propagation Delay Time (CLOCK-Q, $\overline{Q}$)		14	23	ns
t_{PHL}	Propagation Delay Time (PRESET-Q, $\overline{Q}$)		17	27	ns
f_{MAX}	Maximum Clock Frequency	35	64		MHz

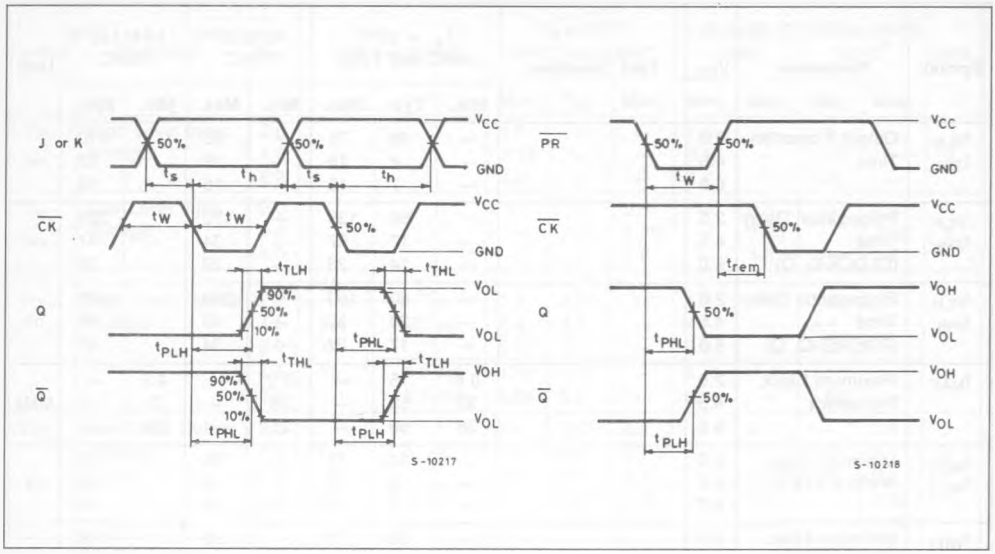
AC ELECTRICAL CHARACTERISTICS ($C_L = 50pF$, Input $t_r = t_f = 6ns$)

Symbol	Parameter	V_{CC}	Test Condition	T_A = 25°C 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0		—	30	75	—	95		110	ns
		4.5		—	8	15	—	19		22	
		6.0		—	7	13	—	16		19	
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{CLOCK}$-Q, $\overline{Q}$)	2.0		—	68	135	—	170		205	ns
		4.5		—	17	27	—	34		41	
		6.0		—	14	23	—	29		35	
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{PRESET}$-Q, $\overline{Q}$)	2.0		—	80	160	—	200		240	ns
		4.5		—	20	32	—	40		48	
		6.0		—	17	27	—	34		41	
f_{MAX}	Maximum Clock Frequency	2.0		6.4	15	—	5.2	—	4.2	—	MHz
		4.5		32	58	—	26	—	21	—	
		6.0		38	68	—	31	—	25	—	
$t_{W(H)}$ $t_{W(L)}$	Minimum Pulse Width ($\overline{CLOCK}$)	2.0		—	30	75	—	95		110	ns
		4.5		—	8	15	—	19		22	
		6.0		—	7	13	—	16		19	
$t_{W(L)}$	Minimum Pulse Width $\overline{PRESET}$	2.0		—	30	75	—	95		110	ns
		4.5		—	8	15	—	19		22	
		6.0		—	7	13	—	16		19	
t_s	Minimum Set-up Time J, K	2.0		—	25	75	—	95		110	ns
		4.5		—	5	15	—	19		22	
		6.0		—	4	13	—	16		19	
t_h	Minimum Hold Time J, K	2.0		—	—	0	—	0	—	0	ns
		4.5		—	—	0	—	0	—	0	
		6.0		—	—	0	—	0	—	0	
t_{REM}	Minimum Removal Time ($\overline{PRESET}$)	2.0		—	0	0	—	0	—	0	ns
		4.5		—	0	0	—	0	—	0	
		6.0		—	0	0	—	0	—	0	
C_{IN}	Input Capacitance			—	5	10	—	10		10	pF
C_{PD} (*)	Power Dissipation Capacitance			—	38	—	—	—			pF

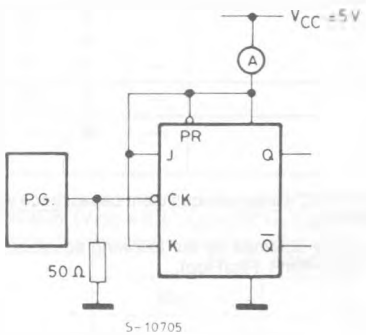
Note (*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the following equation:
$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/2$ (for 1 Flip/Flop).

SWITCHING CHARACTERISTICS TEST WAVEFORM



TEST CIRCUIT I_{CC} (Opr.)



INPUT TRANSITION TIME IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST