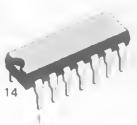
SGS-THOMSON MICROELECTRONICS

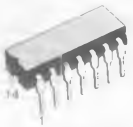
M54HC164
M74HC164

8 BIT SIPO SHIFT REGISTER

- HIGH SPEED
  t_{PD} = 18 ns (TYP) at V_{CC} = 5V
- LOW POWER DISSIPATION
  I_{CC} = 4 μA at T_A = 25°C
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- BALANCED PROPAGATION DELAYS
  t_{PLH} = t_{PHL}
- SYMMETRICAL OUTPUT IMPEDANCE
  I_{OL} = $|I_{OH}|$
- HIGH NOISE IMMUNITY
  V_{NIH} = V_{NIL} = 28% V_{CC} (MIN.)
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2V to 6V
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS164



B1N
Plastic Package



F1
Ceramic Frit Seal Package

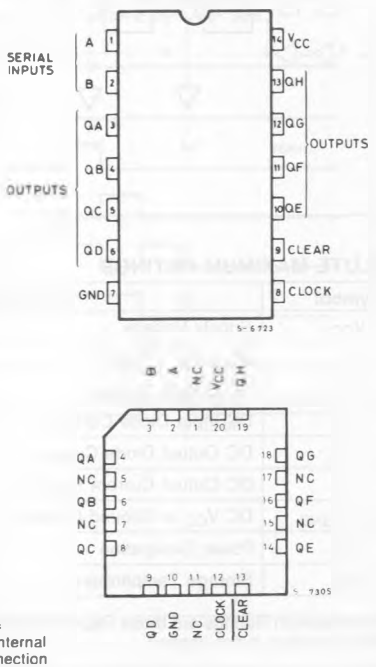
M1
Micro Package

C1
Plastic Chip Carrier

ORDERING NUMBERS:

M54HC164 F1
M74HC164 B1N
M74HC164 F1
M74HC164 C1
M74HC164 M1

PIN CONNECTIONS (top view)



NC = No Internal Connection

DESCRIPTION

The M54/74HC164 is a high speed CMOS 8 BIT SIPO SHIFT REGISTER fabricated in silicon gate C²MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low power consumption.

The HC164 is an 8 bit shift register with serial data entry and an output from each of the eight stages. Data is entered serially through one of two inputs (A or B), either of these inputs can be used as an active high enable for data entry through the other input. An unused input must be high, or both inputs connected together. Each low-to-high transition on the clock input shifts data one place to the right and enters into QA, the logic NAND of the two data inputs ($\overline{A \cdot B}$), the data that existed before the rising clock edge. A low level on the clear input overrides all other inputs and clears the register asynchronously, forcing all Q outputs low.

All inputs are equipped with protection circuits against static discharge and transient excess voltage.

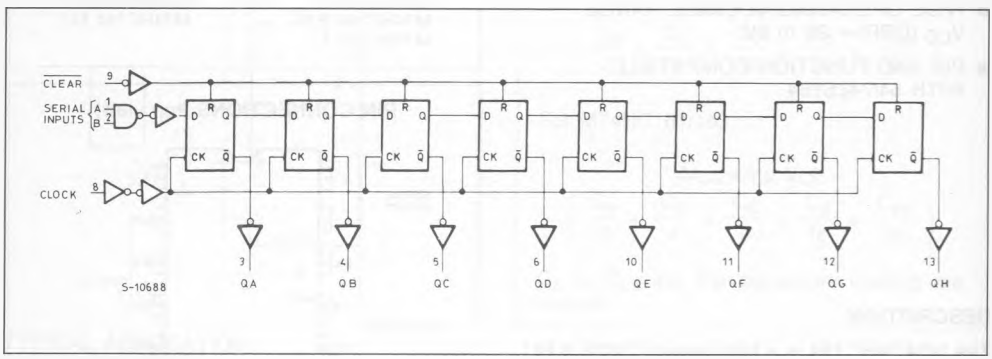
TRUTH TABLE

INPUTS				OUTPUTS			
$\overline{CLEAR}$	CLOCK	SERIAL IN		QA	QB	.....	QH
		A	B				
L	X	X	X	L	L	.....	L
H	↓	X	X	NO CHANGE			
H	↑	L	X	L	QAn	.....	QGn
H	↑	X	L	L	QAn	.....	QGn
H	↑	H	H	H	QAn	.....	QGn

X : DON'T CARE

QAn ~ QGn : THE LEVEL OF QA ~ QG, RESPECTIVELY, BEFORE THE MOST-RECENT POSITIVE TRANSITION OF THE CLOCK.

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to 7	V
V_I	DC Input Voltage	−0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	−0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Current Per Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	−65 to 150	°C

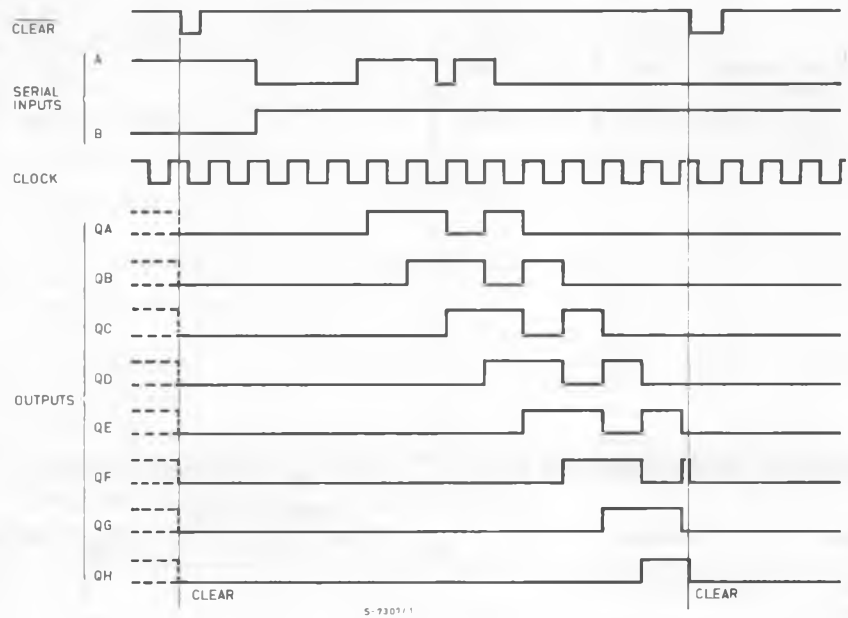
Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW≅ 65°C derate to 300 mW by 10 mW/°C: 65°C to 85°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	2 to 6	V
V_I	Input Voltage	0 to V_{CC}	V
V_O	Output Voltage	0 to V_{CC}	V
T_A	Operating Temperature 74HC Series 54HC Series	−55 to 125 −40 to 85	°C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V: 0 to 1000 V_{CC} = 4.5V: 0 to 500 V_{CC} = 6 V: 0 to 400	ns

TIMING CHART



DC SPECIFICATIONS

Symbol	Parameter	V_{CC}	Test Condition		$T_A = 25°C$ 54HC and 74HC			− 40 to 85°C 74HC		− 55 to 125°C 54HC		Unit
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5	—	—	1.5	—	1.5	—	V
		4.5			3.15	—	—	3.15	—	3.15	—	
		6.0			4.2	—	—	4.2	—	4.2	—	
V_{IL}	Low Level Input Voltage	2.0			—	—	0.5	—	0.5	—	0.5	V
		4.5			—	—	1.35	—	1.35	—	1.35	
		6.0			—	—	1.8	—	1.8	—	1.8	
V_{OH}	High Level Output Voltage	2.0	V_I	I_O	1.9	2.0	—	1.9	—	1.9	—	V
		4.5	V_{IH} or V_{IL}	− 20 μA	4.4	4.5	—	4.4	—	4.4	—	
		6.0			5.9	6.0	—	5.9	—	5.9	—	
		4.5		− 4.0 mA	4.18	4.31	—	4.13	—	4.10	—	
		6.0		− 5.2 mA	5.68	5.8	—	5.63	—	5.60	—	
V_{OL}	Low Level Output Voltage	2.0	V_{IH} or V_{IL}	20 μA	—	0.0	0.1	—	0.1	—	0.1	V
		4.5			—	0.0	0.1	—	0.1	—	0.1	
		6.0			—	0.0	0.1	—	0.1	—	0.1	
		4.5		4.0 mA	—	0.17	0.26	—	0.33	—	0.40	
		6.0		5.2 mA	—	0.18	0.26	—	0.33	—	0.40	
I_I	Input Leakage Current	6.0	$V_I = V_{CC}$ or GND		—	—	±0.1	—	±1.0	—	±1.0	μA
I_{CC}	Quiescent Supply Current	6.0	$V_I = V_{CC}$ or GND		—	—	4	—	40	—	80	μA

AC ELECTRICAL CHARACTERISTICS ($V_{CC} = 5V$, $T_A = 25°C$, $C_L = 15pF$, Input $t_r = t_f = 6ns$)

Symbol	Parameter	54HC and 74HC			Unit
		Min.	Typ.	Max.	
t_{TLH} t_{THL}	Output Transition Time		4	8	ns
t_{PLH} t_{PHL}	Propagation Delay Time (CK-Q)		18	29	ns
t_{PHL}	Propagation Delay Time ($\overline{CLEAR}$-Q)		19	30	ns
f_{MAX}	Maximum Clock Frequency	30	51		Mhz

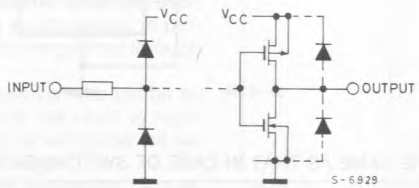
AC ELECTRICAL CHARACTERISTICS ($C_L = 50pF$, Input $t_r = t_f = 6ns$)

Symbol	Parameter	V_{CC}	Test Condition	T_A = 25°C 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0 4.5 6.0		— — —	30 8 7	75 15 13	— — —	95 19 16		110 22 19	ns
t_{PLH} t_{PHL}	Propagation Delay Time (CLOCK - Q)	2.0 4.5 6.0		— — —	88 22 19	175 35 30	— — —	220 44 37		260 52 44	ns
t_{PHL}	Propagation Delay Time ($\overline{CLEAR}$-Q)	2.0 4.5 6.0		— — —	92 23 20	180 36 31	— — —	225 45 38		270 54 46	ns
f_{MAX}	Maximum Clock Frequency	2.0 4.5 6.0		5 27 32	9 46 54	— — —	4 22 26	— — —	3 18 21	— — —	MHz
$t_{W(H)}$ $t_{W(L)}$	Minimum Pulse Width (CLOCK)	2.0 4.5 6.0		— — —	30 8 7	75 15 13	— — —	95 19 16		110 22 19	ns
$t_{W(L)}$	Minimum Pulse Width ($\overline{CLEAR}$)	2.0 4.5 6.0		— — —	30 8 7	75 15 13	— — —	95 19 16		110 22 19	ns
t_s	Minimum Set-up Time (A, B)	2.0 4.5 6.0		— — —	25 7 6	75 15 13	— — —	95 19 16		110 22 19	ns
t_h	Minimum Hold Time (A, B)	2.0 4.5 6.0		— — —	— — —	0 0 0	— — —	0 0 0	— — —	0 0 0	ns
t_{REM}	Minimum Removal Time ($\overline{CLEAR}$)	2.0 4.5 6.0		— — —	— — —	0 0 0	— — —	0 0 0	— — —	0 0 0	ns
C_{IN}	Input Capacitance			—	5	10	—	10		10	pF
C_{PD} (*)	Power Dissipation Capacitance			—	112	—	—	—			pF

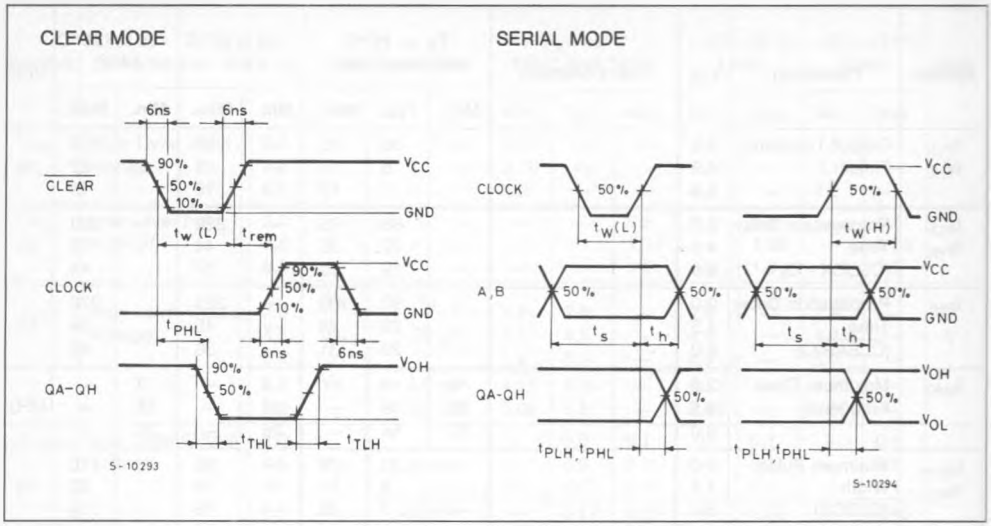
Note (*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current is: $I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$

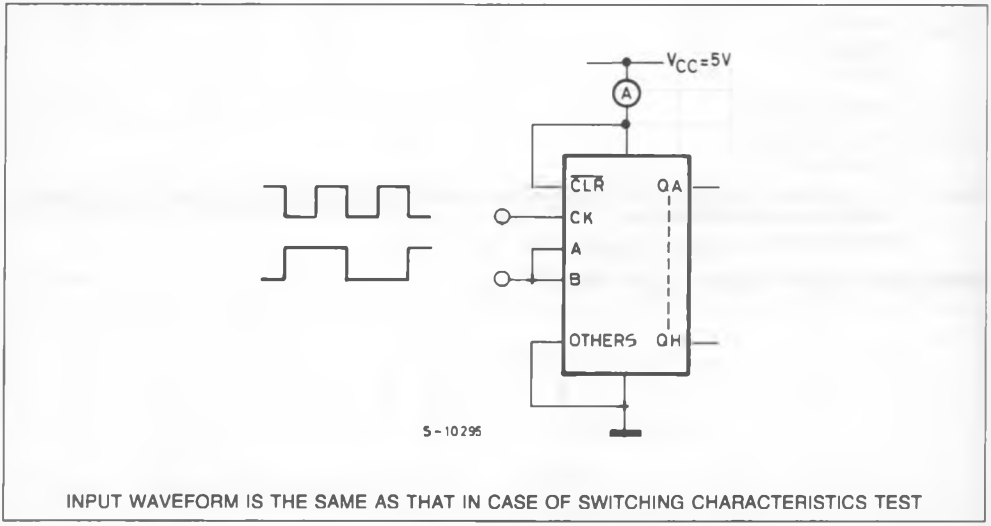
INPUT AND OUTPUT EQUIVALENT CIRCUIT



SWITCHING CHARACTERISTICS TEST WAVEFORM



TEST CIRCUIT I_{CC} (Opr.)



INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST