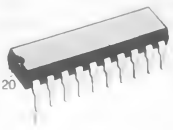
SGS-THOMSON MICROELECTRONICS

M54/74HC373/573
M54/74HC533/563

OCTAL D-TYPE LATCH WITH 3-STATE OUTPUT
HC373/573 NON INVERTING, HC533/563 INVERTING

- HIGH SPEED
  t_{PD} = 15 ns (TYP.) at V_{CC} = 5V
- LOW POWER DISSIPATION
  I_{CC} = 4 μA (MAX.) at T_A = 25°C
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28% V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  15 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 6 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2V to 6V
- PIN AND FUNCTION COMPATIBLE
  WITH 74LS373/533/563/573



B1N
Plastic Package

F1
Ceramic Frit Seal Package

M1
Micro Package

C1
Plastic Chip Carrier

ORDERING NUMBERS:

M54HCXXX F1
M74HCXXX B1N
M74HCXXX F1
M74HCXXX C1
M74HCXXX M1

DESCRIPTION

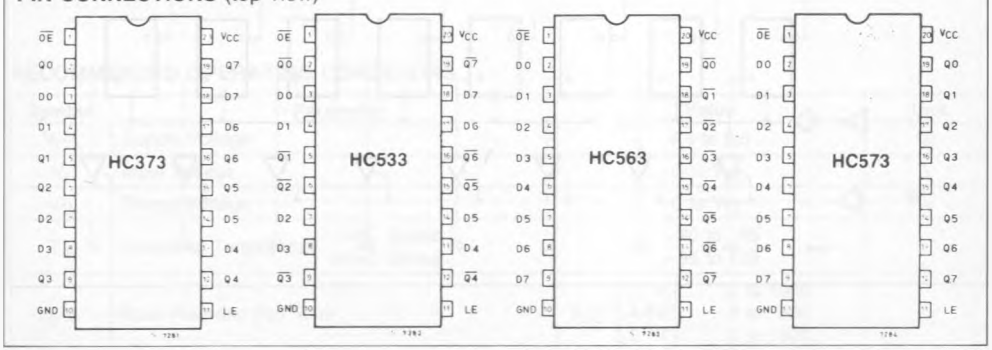
The M54/74HC373, M54/74HC533, M54/74HC563 and M54/74HC573 are high speed CMOS OCTAL LATCH with 3-STATE OUTPUT fabricated with silicon gate C²MOS technology.

These ICs achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

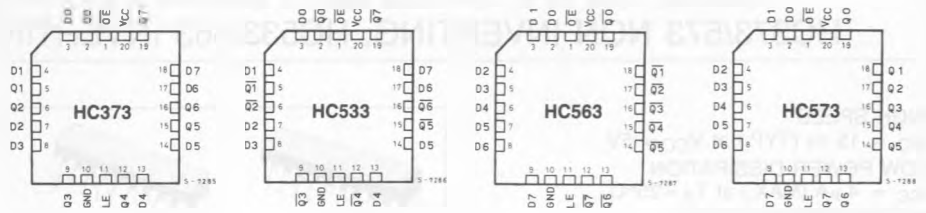
These 8-bit D-type latches are controlled by a latch enable input (LE) and a output enable input ($\overline{OE}$). While the LE input is held at a high level, the Q outputs will follow the data input precisely or inversely. When the LE is taken low, the Q outputs will be latched precisely or inversely at the logic level of D input data. While the $\overline{OE}$ input is at low level, the eight outputs will be in a normal logic state (high or low logic level) and while high level the outputs will be in a high impedance state.

The application designer has a choice of combination of inverting and non-inverting outputs, symmetrical and neighbouring input/output pin layout. The HC373 and the HC573, the HC533 and the HC563 have the same function and the same characteristics respectively, but have different pin layouts. The three-state output configuration and the wide choice of outline make bus-organized systems simple. All inputs are equipped with protection circuits against static discharge and transient excess voltage.

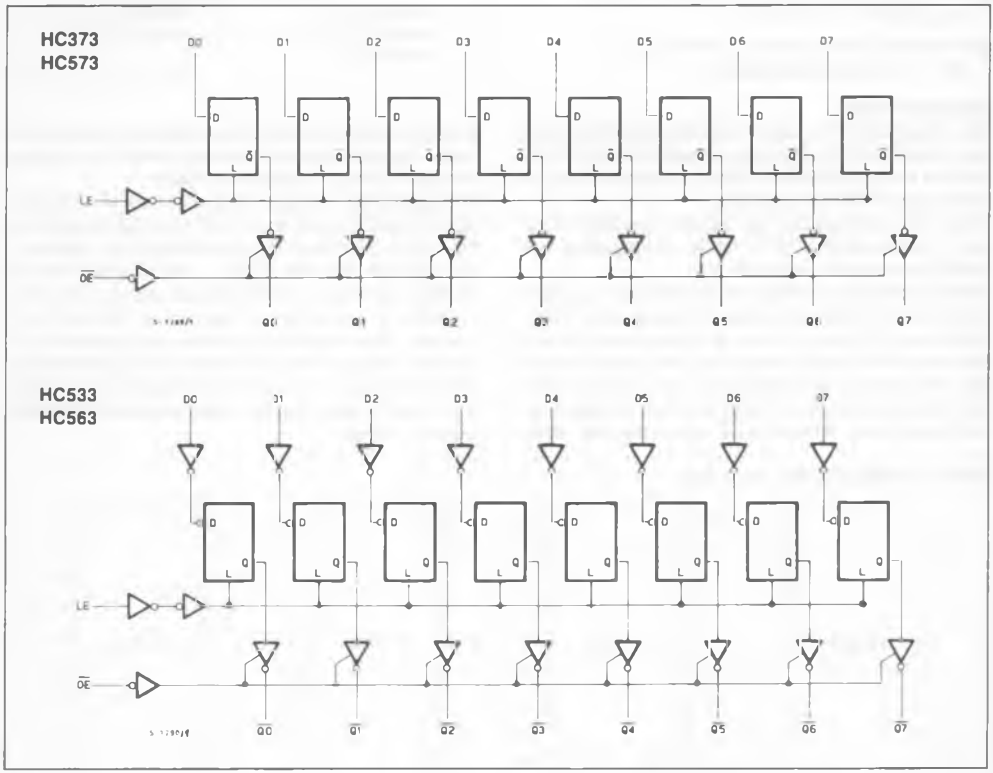
PIN CONNECTIONS (top view)



CHIP CARRIER



LOGIC DIAGRAM



TRUTH TABLE

INPUTS			OUTPUTS	
$\overline{OE}$	LE	D	Q (HC373) (HC573)	$\overline{Q}$ (HC533) (HC563)
H	X	X	Z	Z
L	L	X	NO CHANGE*	NO CHANGE*
L	H	L	L	H
L	H	H	H	L

X: DON'T CARE Z: HIGH IMPEDANCE

*: Q/$\overline{Q}$ OUTPUTS ARE LATCHED AT THE TIME WHEN THE LE INPUT IS TAKEN LOW LOGIC LEVEL.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to 7	V
V_I	DC Input Voltage	−0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	−0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 35	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 70	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	−65 to 150	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: ≅ 65°C derate to 300 mW by 10 mW/°C: 65°C to 85°C

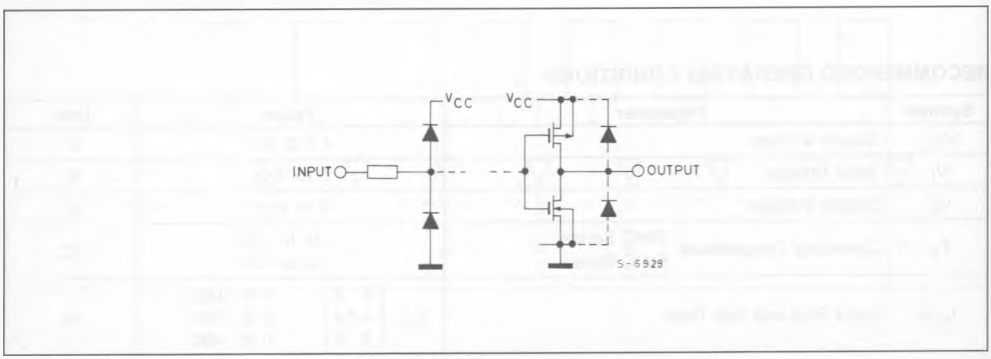
RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value		Unit
V_{CC}	Supply Voltage	4.5 to 5.5		V
V_I	Input Voltage	0 to V_{CC}		V
V_O	Output Voltage	0 to V_{CC}		V
T_A	Operating Temperature 74HC Series 54HC Series	−40 to 85 −55 to 125		°C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V	0 to 1000	ns
		V_{CC} = 4.5V	0 to 500	
		V_{CC} = 6 V	0 to 400	

DC SPECIFICATIONS

Symbol	Parameter	V_{CC}	Test Condition		$T_A = 25°C$ 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5	—	—	1.5	—	1.5	—	V
		4.5			3.15	—	—	3.15	—	3.15	—	
		6.0			4.2	—	—	4.2	—	4.2	—	
V_{IL}	Low Level Input Voltage	2.0			—	—	0.5	—	0.5	—	0.5	V
		4.5			—	—	1.35	—	1.35	—	1.35	
		6.0			—	—	1.8	—	1.8	—	1.8	
V_{OH}	High Level Output Voltage	2.0	V_I	I_O	1.9	2.0	—	1.9	—	1.9	—	V
		4.5	V_{IH} or V_{IL}	−20 μA	4.4	4.5	—	4.4	—	4.4	—	
		6.0			5.9	6.0	—	5.9	—	5.9	—	
		4.5		−6.0 mA	4.18	4.31	—	4.13	—	4.10	—	
		6.0		−7.8 mA	5.68	5.8	—	5.63	—	5.60	—	
V_{OL}	Low Level Output Voltage	2.0	V_{IH} or V_{IL}	20 μA	—	0.0	0.1	—	0.1	—	0.1	V
		4.5			—	0.0	0.1	—	0.1	—	0.1	
		6.0			—	0.0	0.1	—	0.1	—	0.1	
		4.5		6.0 mA	—	0.17	0.26	—	0.33	—	0.40	
		6.0		7.8 mA	—	0.18	0.26	—	0.33	—	0.40	
I_I	Input Leakage Current	6.0	$V_I = V_{CC}$ or GND		—	—	±0.1	—	±1.0	—	±1.0	μA
I_{OZ}	3-State Output Off-State Current	6.0	$V_I = V_{IH}$ or V_{IL} $V_O = V_{CC}$ or GND		—	—	±0.5	—	±5.0	—	±1.0	μA
I_{CC}	Quiescent Supply Current	6.0	$V_I = V_{CC}$ or GND $I_O = 0$		—	—	4	—	40	—	80	μA

INPUT AND OUTPUT EQUIVALENT CIRCUIT



AC ELECTRICAL CHARACTERISTICS (C_L = 50pF, Input $t_r = t_f$ = 6ns)

Symbol	Parameter	V_{CC}	Test Condition	T_A = 25°C 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0		—	24	60	—	75	—	90	ns
		4.5		—	8	12	—	15	—	18	
		6.0		—	6	10	—	13	—	15	
t_{PLH} t_{PHL}	Propagation Delay Time (LE - Q, $\overline{Q}$) *	2.0		—	82	175	—	220	—	265	ns
		4.5		—	22	35	—	44	—	53	
		6.0		—	19	30	—	37	—	45	
t_{PLH} t_{PHL}	Propagation Delay Time (LE-Q, $\overline{Q}$) **	2.0		—	75	150	—	190	—	225	ns
		4.5		—	19	30	—	38	—	45	
		6.0		—	16	26	—	33	—	38	
t_{PLH} t_{PHL}	Propagation Delay Time (D-Q, $\overline{Q}$) *	2.0		—	66	145	—	180	—	220	ns
		4.5		—	18	29	—	36	—	44	
		6.0		—	16	25	—	31	—	38	
t_{PLH} t_{PHL}	Propagation Delay Time (D-Q, $\overline{Q}$) **	2.0		—	63	130	—	165	—	195	ns
		4.5		—	16	26	—	33	—	39	
		6.0		—	14	22	—	28	—	33	
$t_{W(H)}$	Minimum Pulse Width (LE)	2.0		—	30	75	—	95	—	110	ns
		4.5		—	8	15	—	19	—	22	
		6.0		—	7	13	—	16	—	19	
t_s	Minimum Set-up Time	2.0		—	10	50	—	65	—	75	ns
		4.5		—	2	10	—	13	—	15	
		6.0		—	2	9	—	11	—	13	
t_h	Minimum Hold Time	2.0		—	—	50	—	65	—	75	ns
		4.5		—	—	10	—	13	—	15	
		6.0		—	—	9	—	11	—	13	
t_{PZL} t_{PZH}	Output Enable Time *	2.0	R_L = 1KΩ	—	72	150	—	190	—	225	ns
		4.5		—	18	30	—	38	—	45	
		6.0		—	15	26	—	33	—	38	
t_{PZL} t_{PZH}	Output Enable Time **	2.0	R_L = 1KΩ	—	62	140	—	175	—	210	ns
		4.5		—	18	28	—	35	—	42	
		6.0		—	16	24	—	30	—	36	
t_{PZH} t_{PHZ}	Output Disable Time *	2.0	R_L = 1kΩ	—	45	150	—	190	—	225	ns
		4.5		—	22	30	—	38	—	45	
		6.0		—	20	26	—	33	—	37	
t_{PLZ} t_{PHZ}	Output Disable Time **	2.0	R_L = 1KΩ	—	45	150	—	190	—	225	ns
		4.5		—	22	30	—	38	—	45	
		6.0		—	20	26	—	33	—	38	
C_{IN}	Input Capacitance			—	5	10	—	10	—	—	pF
C_{OUT}	Output Capacitance			—	10	—	—	—	—	—	pF
C_{PD} ◆	Power Dissipation Capacitance			—	41	—	—	—	—	—	pF

Note ◆ C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit)

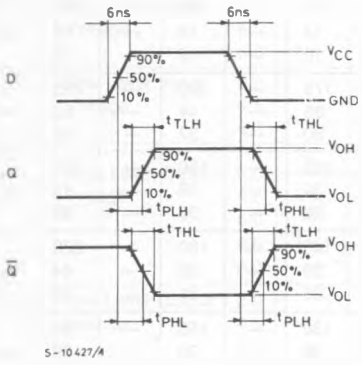
Average operating current can be obtained by the following equation.

$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8$ (per Latch)

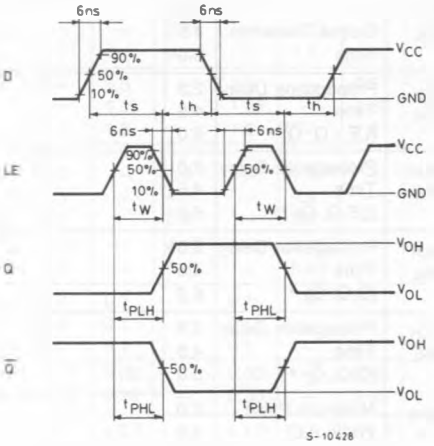
* M54/74HC373/533 ** M54/74HC563/573

SWITCHING CHARACTERISTICS TEST WAVEFORM

t_{PLH}, t_{PHL} (D - Q, $\overline{Q}$)



t_{PLH}, t_{PHL} (LE - Q, $\overline{Q}$), t_s, t_h, t_W

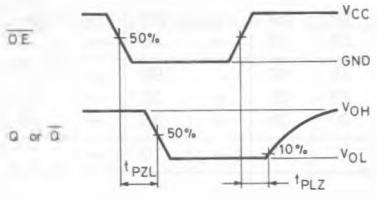


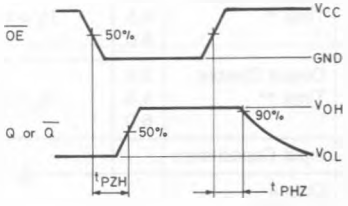
t_{PLZ}, t_{PZL}

The 1KΩ load resistors should be connected between outputs and V_{CC} line and the 50 pF load capacitors should be connected between outputs and GND line. All inputs except $\overline{OE}$ input should be connected to V_{CC} line or GND line such that outputs will be in low logic level while $\overline{OE}$ in put is held low.

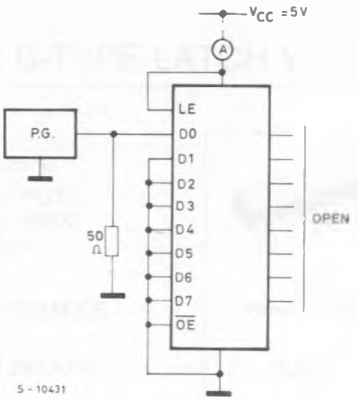
t_{PHZ}, t_{PZH}

The 1KΩ load resistors and the 50pF load capacitors should be connected between each output and GND line.
All inputs except $\overline{OE}$ input should be connected to V_{CC} or GND line such that output will be in high logic level while $\overline{OE}$ input is held low.





TEST CIRCUIT I_{CC} (Opr.)



INPUT WAVEFORM IN THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.