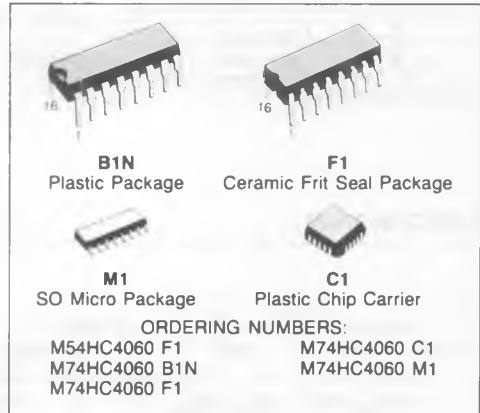


14-STAGE BINARY COUNTER/OSCILLATOR

- **HIGH SPEED**
 $f_{MAX} = 60 \text{ MHz (TYP)}$ at $V_{CC} = 5V$
- **LOW POWER DISSIPATION**
 $I_{CC} = 4 \mu A \text{ (MAX.)}$ at $T_A = 25^\circ C$
- **HIGH NOISE IMMUNITY**
 $V_{NIH} = V_{NIL} = 28\% V_{CC} \text{ (MIN.)}$
- **OUTPUT DRIVE CAPABILITY**
 10 LSTTL LOADS
- **SYMMETRICAL OUTPUT IMPEDANCE**
 $|I_{OH}| = I_{OL} = 4 \text{ mA (MIN.)}$
- **BALANCED PROPAGATION DELAYS**
 $t_{PLH} = t_{PHL}$
- **WIDE OPERATING VOLTAGE RANGE**
 $V_{CC} \text{ (OPR)} = 2V \text{ to } 6V$
- **PIN AND FUNCTION COMPATIBLE**
 WITH 4060B



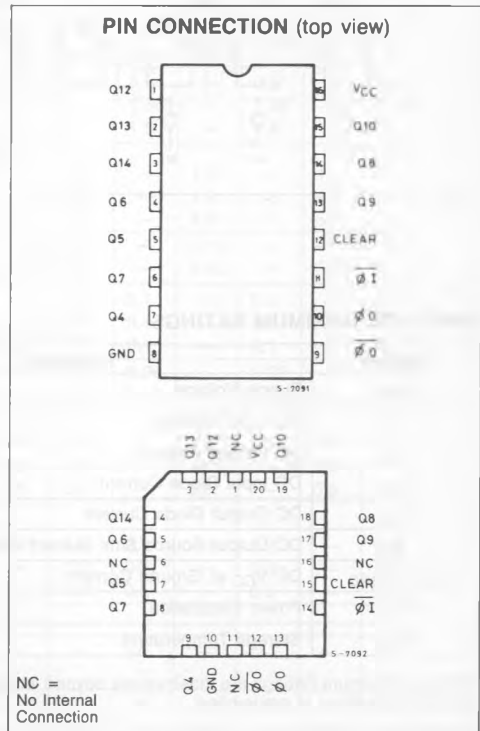
DESCRIPTION

The M54/74HC4060 is a high speed CMOS 14-STAGE BINARY COUNTER/OSCILLATOR fabricated in silicon gate C²MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low power consumption. It operates ten times faster than metal-gate C²MOS IC (4060B) with the same power dissipation.

The oscillator configuration allows design of either RC or crystal oscillator circuits. A high level on the CLEAR accomplishes the reset function, i.e. all counter outputs are made low and the oscillator is disabled.

A negative transition on the clock input increments the counter. Ten kinds of divided output are provided; 4 to 10 and 12 to 14 stage inclusive. The maximum division available at Q12 is 1/16384 f oscillator.

The $\bar{\theta}_1$ input and the CLEAR input are equipped with protection circuits against static discharge and transient excess voltage.

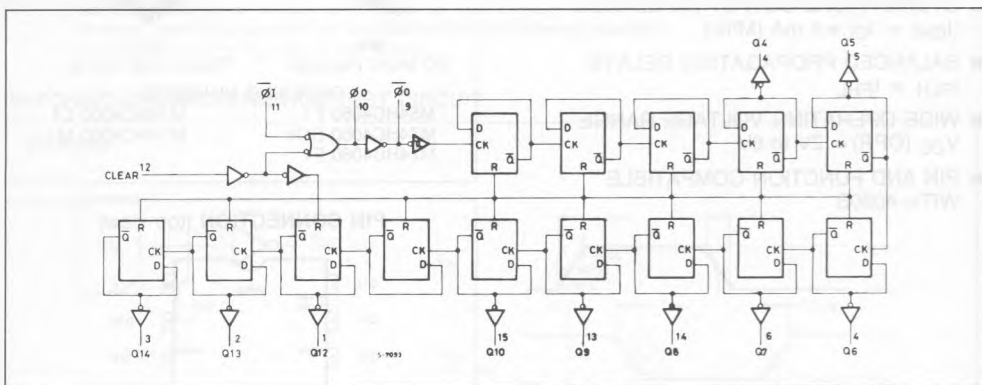


TRUTH TABLE

INPUTS		FUNCTION
θ_1	CLEAR	
X	H	COUNTER IS RESET TO ZERO STATE θ_0 OUTPUT GOES TO HIGH LEVEL $\bar{\theta}_0$ OUTPUT GOES TO LOW LEVEL
\downarrow	L	COUNT UP ONE STEP.
\uparrow	L	NO CHANGE.

X: DON'T CARE

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	- 0.5 to 7	V
V_I	DC Input Voltage	- 0.5 to $V_{CC} + 0.5$	V
V_O	DC Output Voltage	- 0.5 to $V_{CC} + 0.5$	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	- 65 to 150	$^{\circ}C$

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: \cong 65 $^{\circ}C$ derate to 300 mW by 10 mW by 10 mW/ $^{\circ}C$: 65 $^{\circ}C$ to 85 $^{\circ}C$.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	2 to 6	V
V_I	Input Voltage	0 to V_{CC}	V
V_O	Output Voltage	0 to V_{CC}	V
T_A	Operating Temperature 74HC Series 54HC Series	- 40 to 85 - 55 to 125	°C
t_r, t_f	Input Rise and Fall Time	$V_{CC} \begin{cases} 2 \text{ V} & 0 \text{ to } 1000 \\ 4.5 \text{ V} & 0 \text{ to } 500 \\ 6 \text{ V} & 0 \text{ to } 400 \end{cases}$	ns

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	V_{CC}	Test Condition		$T_A = 25^\circ\text{C}$ 54HC and 74HC			- 40 to 85°C 74HC		- 55 to 125°C 54HC		Unit		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.			
V_{IH}	High Level Input Voltage	2.0			1.5	—	—	1.5	—	1.5	—	V		
		4.5			3.15	—	—	3.15	—	3.15	—			
		6.0			4.2	—	—	4.2	—	4.2	—			
V_{IL}	Low Level Input Voltage	2.0			—	—	0.5	—	0.5	—	0.5	V		
		4.5			—	—	1.35	—	1.35	—	1.35			
		6.0			—	—	1.8	—	1.8	—	1.8			
V_{OH}	High Level Output Voltage (Q Outputs)	2.0	V_I	I_O	1.9	2.0	—	1.9	—	1.9	—	V		
		4.5			V_{IH} or V_{IL}	- 20 μA	4.4	4.5	—	4.4	—		4.4	—
		6.0					5.9	6.0	—	5.9	—		5.9	—
		4.5			- 4.0 mA - 5.2 mA	4.18	4.31	—	4.13	—	4.10		—	
6.0	5.68	5.8	—	5.63		—	5.60	—						
V_{OL}	Low Level Output Voltage (Q Outputs)	2.0	V_{IH} or V_{IL}	20 μA	—	0.0	0.1	—	0.1	—	0.1	V		
		4.5			—	0.0	0.1	—	0.1	—	0.1			
		6.0			—	0.0	0.1	—	0.1	—	0.1			
		4.5			4.0 mA 5.2 mA	—	0.17	0.26	—	0.33	—		0.40	
6.0	—	0.18	0.26	—		0.33	—	0.40						
V_{OH}	High Level Output Voltage $\bar{\theta}_0, \bar{\theta}_0$ Output	2.0	V_I	I_O	1.8	2.0	—	1.8	—	1.8	—	V		
		4.5			V_{IH} or V_{IL}	- 20 μA	4.0	4.5	—	4.0	—		4.0	—
		6.0					5.5	5.9	—	5.5	—		5.5	—
V_{OL}	Low Level Output Voltage $\bar{\theta}_0, \bar{\theta}_0$ Output	2.0	V_{IH} or V_{IL}	20 μA	—	0.0	0.2	—	0.2	—	0.2	V		
		4.5			—	0.0	0.5	—	0.5	—	0.5			
		6.0			—	0.1	0.5	—	0.5	—	0.5			
I_I	Input Leakage Current	6.0	$V_I = V_{CC}$ or GND		—	—	± 0.1	—	± 1	—	± 1	μA		
I_{CC}	Quiescent Supply Current	6.0	$V_I = V_{CC}$ or GND		—	—	4	—	40	—	80	μA		

AC ELECTRICAL CHARACTERISTICS ($V_{CC} = 5V$, $T_A = 25^\circ C$, $C_L = 15pF$, Input $t_r = t_f = 6ns$)

Symbol	Parameter	54HC and 74HC			Unit
		Min.	Typ.	Max.	
t_{TLH} t_{THL}	Output Transition Time		4	8	ns
t_{PHL} t_{PHL}	Propagation Delay Time ($\emptyset - Q_4$)		43	65	ns
t_{PLH} t_{PHL}	Propagation Delay Time ($Q_n - Q_{n+1}$)		7	12	ns
t_{PLH} t_{PHL}	Propagation Delay Time (CLEAR - Q_n)		21	34	ns
f_{MAX}	Maximum Clock Frequency	33	60		MHz

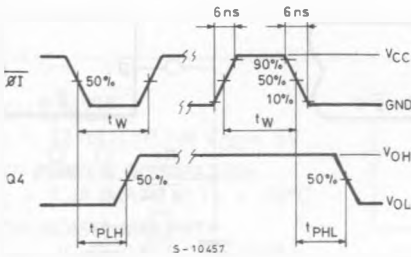
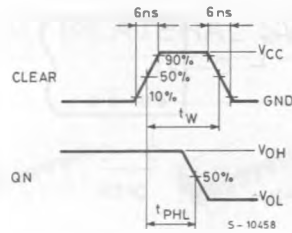
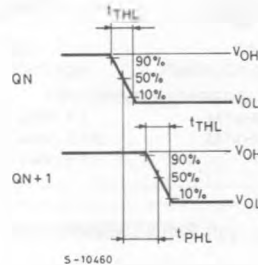
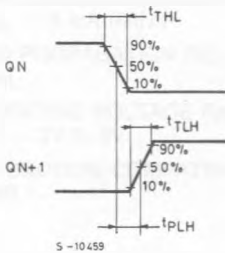
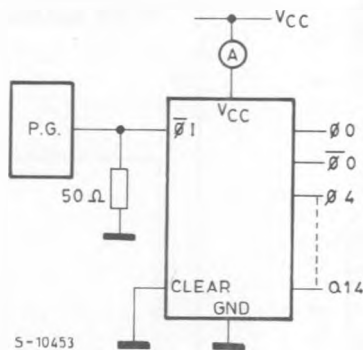
AC ELECTRICAL CHARACTERISTICS ($C_L = 50pF$, Input $t_r = t_f = 6ns$)

Symbol	Parameter	V_{CC}	Test Condition	$T_A = 25^\circ C$ 54HC and 74HC			-40 to $85^\circ C$ 74HC		-55 to $125^\circ C$ 54HC		Unit	
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.		
				t_{TLH} t_{THL}	Output Transition Time	2.0 4.5 6.0		— — —	30 8 7	75 15 13		— — —
t_{PLH} t_{PHL}	Propagation Delay Time ($\beta_1 - Q_4$)	2.0 4.5 6.0		— — —	196 49 42	370 74 63	— — —	465 93 80	— — —	555 111 95	ns	
t_{PLH} t_{PHL}	Propagation Delay Time ($Q_n - Q_{n+1}$)	2.0 4.5 6.0		— — —	35 9 8	75 15 13	— — —	95 19 16	— — —	110 22 19	ns	
t_{PHL}	Propagation Delay Time (CLEAR - Q_n)	2.0 4.5 6.0		— — —	100 25 21	195 39 33	— — —	245 49 42	— — —	295 59 50	ns	
f_{MAX}	Maximum Clock Frequency	2.0 4.5 6.0		— — —	6 30 35	13 55 64	— — —	5 24 28	— — —	4 20 24	— — —	MHz
$t_{W(L)}$ $t_{W(H)}$	Minimum Pulse Width CLOCK (β_1)	2.0 4.5 6.0		— — —	30 8 7	75 15 13	— — —	95 19 16	— — —	110 22 19	ns	
$t_{W(H)}$	Minimum Pulse Width (CLEAR)	2.0 4.5 6.0		— — —	60 15 13	125 25 21	— — —	155 31 26	— — —	190 38 32	ns	
t_{REM}	Minimum Removal Time (CLEAR)	2.0 4.5 6.0		— — —	40 10 9	100 20 17	— — —	125 25 21	— — —	150 30 26	ns	
C_{IN}	Input Capacitance			—	5	10	—	10	—	10	pF	
C_{PD}^*	Power Dissipation			—	33	—	—	—	—	—	pF	

Note (*) C_{PD} is defined as the value of the IC's of internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit)

Average operating current can be obtained by the following equation $I_{CC} (Opr.) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$

SWITCHING CHARACTERISTICS TEST WAVEFORM

 t_{PLH} , t_{PHL} (CLOCK-Q) t_W (CLOCK) t_{PHL} (CLEAR - Qn), t_W (CLEAR) t_{PLH} , t_{PHL} (Qn - Qn + 1)TEST CIRCUIT I_{CC} (Opr.)

* θ_J INPUT $t_r = t_f = 6$ ns
DUTY = 50%

S-10453

NOTE: WHEN CR OR CRYSTAL OSCILLATION CIRCUIT IS ADOPTED, THE DYNAMIC POWER DISSIPATION WILL BE GREATER THAN THE MEASURED VALUE FROM THE TEST CIRCUIT SHOWN LEFT, BECAUSE THESE OSCILLATION CIRCUITS SPEND MUCH SUPPLY CURRENT

TYPICAL CLOCK DRIVE CIRCUITS

