SGS-THOMSON MICROELECTRONICS

M54HC4094
M74HC4094

8-BIT SIPO SHIFT LATCH REGISTER (3-STATE)

- HIGH SPEED
  f_{MAX} = 42 MHz (TYP.) at V_{CC} = 5V
- LOW POWER DISSIPATION
  I_{CC} = 4 μA (MAX.) at T_A = 25°C
- HIGH NOISE IMMUNITY
  V_{NIH} = V_{NIL} = 28% V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}|$ = I_{OL} = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  t_{PLH} = t_{PHL}
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2V to 6V
- PIN AND FUNCTION COMPATIBLE
  WITH 4094B

B1N
Plastic Package

F1
Ceramic Frit Seal Package

M1
Micro Package

C1
Plastic Chip Carrier

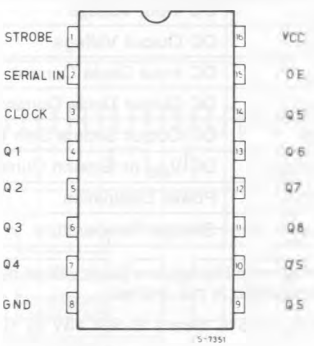
ORDERING NUMBERS:

M54HC4094 F1
M74HC4094 B1N
M74HC4094 F1
M74HC4094 C1
M74HC4094 M1

DESCRIPTION

The M54/74HC4094 is a high speed CMOS 8 BIT SIPO SHIFT LATCH REGISTER fabricated with silicon gate C²MOS technology.
It has the same high speed performance of LSTTL combined with true CMOS low power consumption. This device consists of an 8-bit shift register and an 8-bit latch with 3-state output buffer. Data is shifted serially through the shift register on the positive going transition of the clock input signal. The output of the last stage (Qs) can be used to cascade several devices.
Data on the Qs output is transferred to a second output (Qs') on the following negative transition of the clock input signal. The data of each stage of the shift register is provided with a latch, which latches data on the negative going transition of the STROBE input signal. When the STROBE input is held high, data propagates through the latch to a 3-state output buffer.
This buffer is enabled when OUTPUT ENABLE input is taken high. All inputs are equipped with protection circuits against static discharge and transient excess voltage.

PIN CONNECTIONS (top view)



NC =
No Internal
Connection

TRUTH TABLE

CK	OE	ST	SI	PARA. OUT.		SERI. OUT	
				Q1	Qn	Qs	Qs'
↑	H	H	L	L	Qn-1	Q7	NC
↑	H	H	H	H	Qn-1	Q7	NC
↑	H	L	X	NC	NC	Q7	NC
↑	L	X	X	Z	Z	Q7	NC
↓	H	X	X	NC	NC	NC	Qs
↓	L	X	X	Z	Z	NC	Qs

X: DON'T CARE

NC: NO CHANGE

Z: HIGH IMPEDANCE

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	− 0.5 to 7	V
V_I	DC Input Voltage	− 0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	− 0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	− 65 to 150	°C

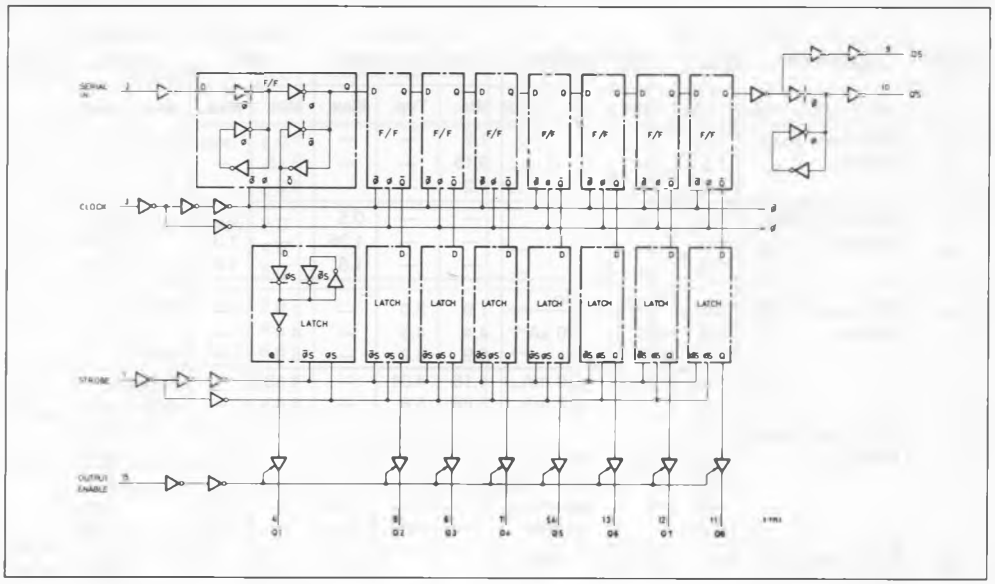
Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: ≅ 65°C derate to 300 mW by 10 mW/°C: 65°C to 85°C.

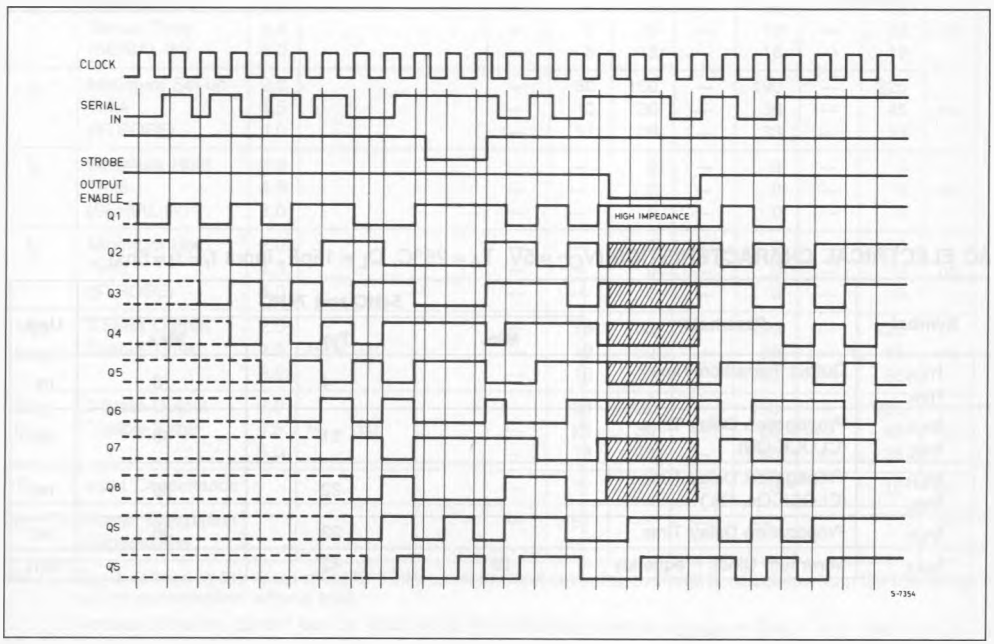
RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value		Unit
V_{CC}	Supply Voltage		2 to 6		V
V_I	Input Voltage		0 to V_{CC}		V
V_O	Output Voltage		0 to V_{CC}		V
T_A	Operating Temperature	74HC Series 54HC Series	− 40 to 85 − 55 to 125		°C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V V_{CC} = 4.5V V_{CC} = 6 V	0 to 1000 0 to 500 0 to 400		ns

LOGIC DIAGRAM



LOGIC DIAGRAM



DC SPECIFICATIONS

Symbol	Parameter	V_{CC}	Test Condition		$T_A = 25°C$ 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5	—	—	1.5	—	1.5	—	V
		4.5			3.15	—	—	3.15	—	3.15	—	
		6.0			4.2	—	—	4.2	—	4.2	—	
V_{IL}	Low Level Input Voltage	2.0			—	—	0.5	—	0.5	—	0.5	V
		4.5			—	—	1.35	—	1.35	—	1.35	
		6.0			—	—	1.8	—	1.8	—	1.8	
V_{OH}	High Level Output Voltage	2.0	V_I	I_O	1.9	2.0	—	1.9	—	1.9	—	V
		4.5	V_{IH} or V_{IL}	−20 μA	4.4	4.5	—	4.4	—	4.4	—	
		6.0			5.9	6.0	—	5.9	—	5.9	—	
		4.5		−4.0 mA	4.18	4.31	—	4.13	—	4.10	—	
		6.0		−5.2 mA	5.68	5.8	—	5.63	—	5.60	—	
V_{OL}	Low Level Output Voltage	2.0	V_{IH} or V_{IL}	20 μA	—	0.0	0.1	—	0.1	—	0.1	V
		4.5			—	0.0	0.1	—	0.1	—	0.1	
		6.0			—	0.0	0.1	—	0.1	—	0.1	
		4.5		4.0 mA	—	0.17	0.26	—	0.33	—	0.40	
		6.0		5.2 mA	—	0.18	0.26	—	0.33	—	0.40	
I_I	Input Leakage Current	6.0	$V_I = V_{CC}$ or GND		—	—	±0.1	—	±1.0	—	±1.0	μA
I_{OZ}	3-State Output Off-State Current	6.0	$V_I = V_{IH}$ or V_{IL} $V_O = V_{CC}$ or GND		—	—	±0.5	—	±5	—	±10	μA
I_{CC}	Quiescent Supply Current	6.0	$V_I = V_{CC}$ or GND		—	—	4	—	40	—	80	μA

AC ELECTRICAL CHARACTERISTICS ($V_{CC} = 5V$, $T_A = 25°C$, $C_L = 15pF$, Input $t_r = t_f = 6ns$)

Symbol	Parameter	54HC and 74HC			Unit
		Min.	Typ.	Max.	
t_{TLH} t_{THL}	Output Transition Time		4	8	ns
t_{PLH} t_{PHL}	Propagation Delay Time (CLOCK-QN)		31	48	ns
t_{PLH} t_{PHL}	Propagation Delay Time (CLOCK-Qs, Qs')		22	35	ns
t_{PLH}	Propagation Delay Time		23	36	ns
f_{MAX}	Maximum Clock Frequency	22	42		MHz

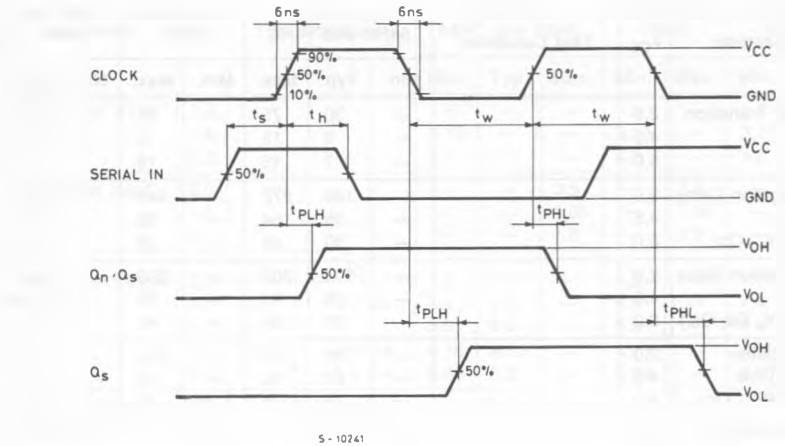
AC ELECTRICAL CHARACTERISTICS (C_L = 50pF, Input $t_r = t_f$ = 6ns)

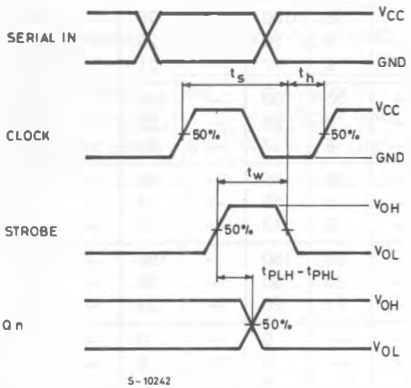
Symbol	Parameter	V_{CC}	Test Condition	T_A = 25°C 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0		—	30	75	—	95		110	ns
		4.5		—	8	15	—	19		22	
		6.0		—	7	13	—	16		19	
t_{PLH} t_{PHL}	Propagation Delay Time (CLOCK - Qn)	2.0		—	140	270	—	340		405	ns
		4.5		—	35	54	—	68		81	
		6.0		—	30	46	—	58		69	
t_{PLH} t_{PHL}	Propagation Delay Time (CLOCK, Qs, Qs')	2.0		—	104	200	—	250		300	ns
		4.5		—	26	40	—	50		60	
		6.0		—	22	34	—	43		51	
t_{PLH} t_{PHL}	Propagation Delay Time (STROBE - Qn)	2.0		—	135	210	—	265	—	315	ns
		4.5		—	27	42	—	53	—	63	
		6.0		—	23	36	—	45	—	54	
f_{MAX}	Maximum Clock Frequency	2.0		4	10	—	3.2	—	2.6	—	MHz
		4.5		20	38	—	16	—	13	—	
		6.0		24	45	—	19	—	15	—	
$t_{W(H)}$ $t_{W(L)}$	Minimum Pulse Width (CLOCK)	2.0		—	35	100	—	125		150	ns
		4.5		—	9	20	—	25		30	
		6.0		—	8	17	—	21		26	
$t_{W(H)}$	Minimum Pulse Width (STROBE)	2.0		—	35	100	—	125		150	ns
		4.5		—	9	20	—	25		30	
		6.0		—	8	17	—	21		26	
t_s	Minimum Set-up Time (SERIAL-IN)	2.0		—	26	75	—	95	—	110	ns
		4.5		—	6	15	—	19	—	22	
		6.0		—	5	13	—	16	—	19	
t_s	Minimum Set-up Time (STROBE)	2.0		—	50	150	—	190	—	225	ns
		4.5		—	13	30	—	38	—	45	
		6.0		—	11	26	—	33	—	38	
t_h	Minimum Hold Time (SERIAL-IN)	2.0		—	—	0	—	0	—	0	ns
		4.5		—	—	0	—	0	—	0	
		6.0		—	—	0	—	0	—	0	
t_h	Minimum Hold Time (STROBE)	2.0		—	—	0	—	0	—	0	ns
		4.5		—	—	0	—	0	—	0	
		6.0		—	—	0	—	0	—	0	
t_{PZL} t_{PZH}	3-State Output Enable Time	2.0	R_L = 1kΩ	—	76	150	—	190	—	225	ns
		4.5		—	19	30	—	38	—	45	
		6.0		—	16	26	—	33	—	38	
t_{PLZ} t_{PHZ}	3-State Output Disable Time	2.0	R_L = 1kΩ	—	84	150	—	190	—	225	ns
		4.5		—	21	30	—	38	—	45	
		6.0		—	18	26	—	33	—	38	
C_{IN}	Input Capacitance			—	5	10	—	10		10	pF
C_{PD} (*)	Power Dissipation Capacitance			—	167	—	—	—			pF

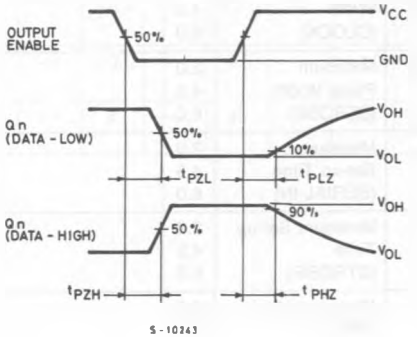
Note (*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the following equation. $I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$

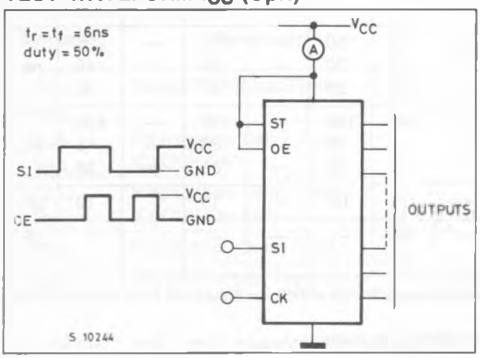
SWITCHING CHARACTERISTICS TEST WAVEFORM







TEST WAVEFORM I_{CC} (Opr.)



C_{PD} CALCULATION

C_{PD} is to be calculated with the following formula by using the measured value of I_{CC} (Opr.) in the test circuit opposite.

$$C_{PD} = \frac{I_{CC(Opr)}}{f_{IN} \cdot V_{CC}}$$

In determining the typical value of C_{PD}, a relatively high frequency of 1MHz was applied to f_{IN}, in order to eliminate any error caused by the quiescent supply current.