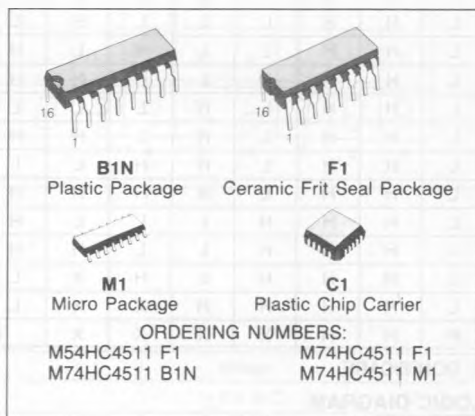


BCD TO-7 SEGMENT LATCH/DECODER/DRIVER

- **HIGH SPEED**
 $t_{PD} = 15 \text{ ns (Typ) at } V_{CC} = 5V$
- **LOW POWER DISSIPATION**
 $I_{CC} = 4 \mu A \text{ (MAX.) at } T_A = 25^\circ C$
- **HIGH NOISE IMMUNITY**
 $V_{NIH} = V_{NIL} = 28\% V_{CC} \text{ (MIN.)}$
- **OUTPUT DRIVE CAPABILITY**
 10 LSTTL LOADS
- **SYMMETRICAL OUTPUT IMPEDANCE**
 $|I_{OH}| = I_{OL} = 20 \text{ mA (MIN.)}$
- **BALANCED PROPAGATION DELAYS**
 $t_{PLH} = t_{PHL}$
- **WIDE OPERATING VOLTAGE RANGE**
 $V_{CC} \text{ (OPR)} = 2V \text{ to } 6V$
- **PIN AND FUNCTION COMPATIBLE**
 WITH 4511B



DESCRIPTION

The M54/74HC4511 is a high speed CMOS BCD-TO-7 SEGMENT LATCH/DECODER/DRIVER fabricated with silicon gate C²MOS technology. It enables high speed latch and decode operation with identical pin connection and function to standard CMOS 4511B.

The segment output driver, which is CMOS fabricated in silicon gate C²MOS technology, has large I_{OH} capability which enables common cathode Leds to be directly driven.

When lamp test (LT) is taken "L", all segment outputs will go to "H", and when blanking (BI) is taken "L" and $\overline{LT}$ is taken "H" all segment outputs will go to "L".

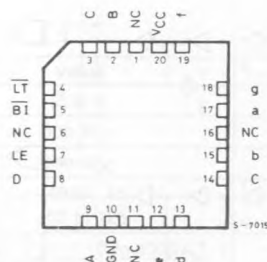
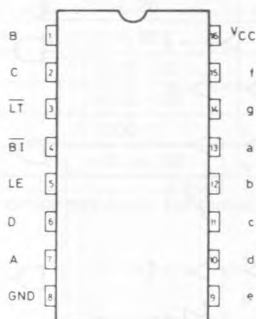
These functions operate regardless of other inputs and are used to test the display.

Input BI is used to pulse-modulate the brightness of the display.

When an error input code (over 10) is applied to the BCD input, all segment outputs will go "L" (turn off).

All inputs are equipped with protection circuits against static discharge and transient excess voltage.

PIN CONNECTION (top view)



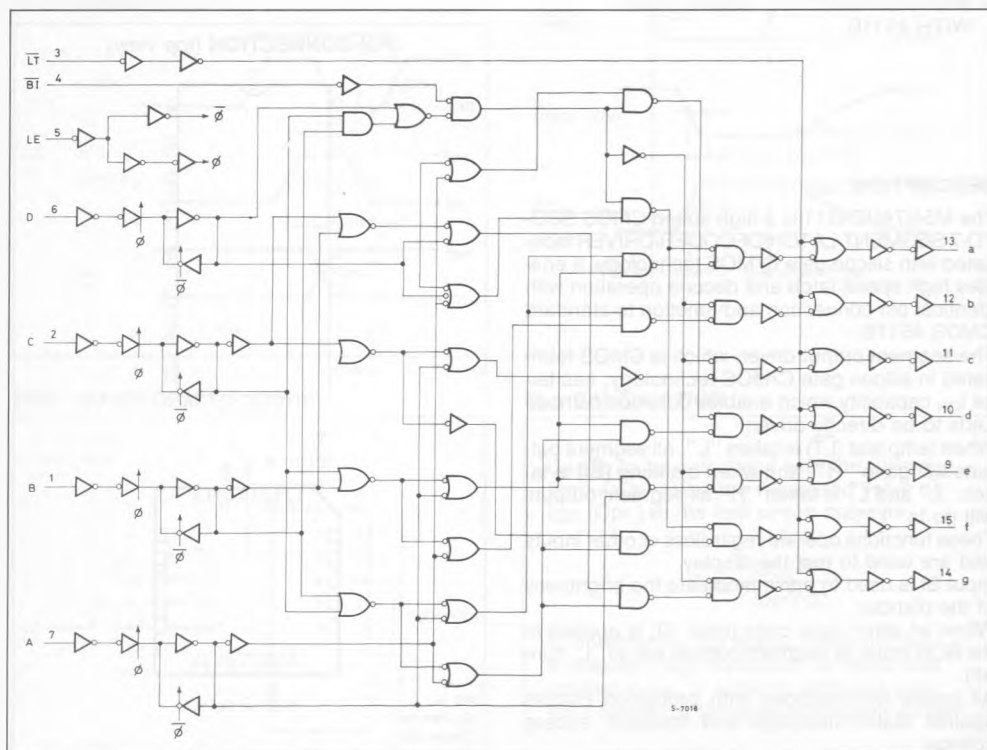
NC =
No Internal
Connection

TRUTH TABLE

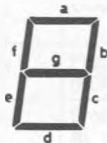
INPUTS							OUTPUTS							DISPLAY MODE
LE	$\overline{\text{BI}}$	$\overline{\text{LT}}$	D	C	B	A	a	b	c	d	e	f	g	
X	X	L	X	X	X	X	H	H	H	H	H	H	H	8
X	L	H	X	X	X	X	L	L	L	L	L	L	L	BLANK
L	H	H	L	L	L	L	H	H	H	H	H	H	L	0
L	H	H	L	L	L	H	L	H	H	L	L	L	L	1
L	H	H	L	L	H	L	H	H	L	H	H	L	H	2
L	H	H	L	L	H	H	H	H	H	L	L	L	H	3
L	H	H	L	H	L	L	L	H	H	L	L	H	H	4
L	H	H	L	H	L	H	H	L	H	H	L	H	H	5
L	H	H	L	H	H	L	L	L	H	H	H	H	H	6
L	H	H	L	H	H	H	H	H	H	L	L	L	L	7
L	H	H	H	L	L	L	H	H	H	H	H	H	H	8
L	H	H	H	L	L	H	H	H	H	L	L	H	H	9
L	H	H	H	L	H	X	L	L	L	L	L	L	L	BLANK
L	H	H	H	H	X	X	L	L	L	L	L	L	L	BLANK
H	H	H	X	X	X	X	Hold the stage at the leading edge of LE							

X: DON'T CARE

LOGIC DIAGRAM



DISPLAY MODE

	INPUT CODE	A	L	H	L	H	L	H	L	H	L	H
		B	L	L	H	H	L	L	H	H	L	L
		C	L	L	L	L	H	H	H	H	L	L
		D	L	L	L	L	L	L	L	L	H	H
		DISPLAY		0	1	2	3	4	5	6	7	8

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{CC}	Supply Voltage	− 0.5 to 7	V
V _I	DC Input Voltage	− 0.5 to V _{CC} + 0.5	V
V _O	DC Output Voltage	− 0.5 to V _{CC} + 0.5	V
I _{IK}	DC Input Diode Current	± 20	mA
I _{OK}	DC Output Diode Current	± 20	mA
I _O	DC Output Source Sink Current Per Output Pin	+ 25/ − 35	mA
I _{CC} or I _{GND}	DC V _{CC} or Ground Current	+ 150/ − 50	mA
P _D	Power Dissipation	500 (*)	mW
T _{stg}	Storage Temperature	− 65 to 150	°C

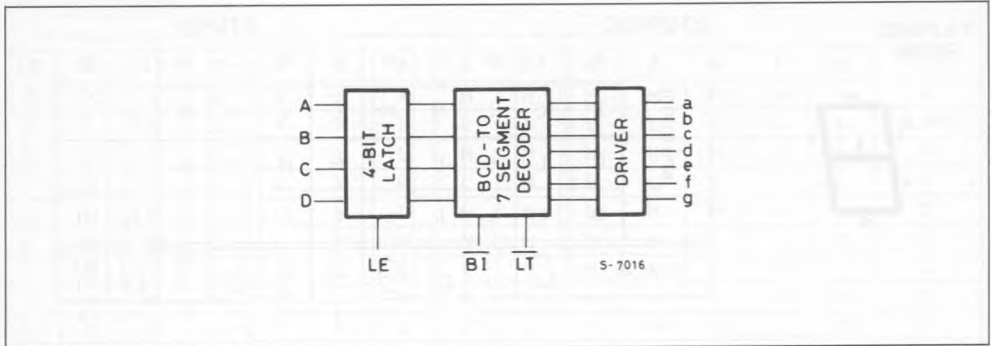
Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: ≡ 65°C derate to 300 mW by 10 mW/°C: 65°C to 85°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V _{CC}	Supply Voltage	2 to 6	V
V _I	Input Voltage	0 to V _{CC}	V
V _O	Output Voltage	0 to V _{CC}	V
T _A	Operating Temperature 74HC Series 54HC Series	− 40 to 85 − 55 to 125	°C
t _r , t _f	Input Rise and Fall Time	V _{CC} { 2 V 0 to 1000 4.5V 0 to 500 6 V 0 to 400	ns

BLOCK DIAGRAM



DC ELECTRICAL CHARACTERISTICS

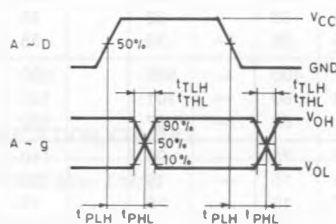
Symbol	Parameter	V _{CC}	Test Condition	T _A = 25°C 54HC and 74HC			- 40 to 85°C 74HC		- 55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V _{IH}	High Level Input Voltage	2.0 4.5 6.0		1.5 3.15 4.2	— — —	— — —	1.5 3.15 4.2	— — —	1.5 3.15 4.2	— — —	V
V _{IL}	Low Level Input Voltage	2.0 4.5 6.0		— — —	— — —	0.5 1.35 1.8	— 1.35 1.8	0.5 1.35 1.8	— — —	0.5 1.35 1.8	V
V _{OH}	High Level Output Voltage	2.0	V _I	I _O	1.9	2.0	—	1.9	—	1.9	V
		4.5	V _{IH} or V _{IL}	— 20 μA	4.4	4.5	—	4.4	—	4.4	
		6.0			5.9	6.0	—	5.9	—	5.9	
		4.5 6.0		— 6.0 mA — 20 mA — 5.2 mA	4.18 3.20 5.68	4.31 3.80 5.8	— — —	4.13 2.90 5.63	— — —	4.10 — 5.60	
V _{OL}	Low Level Output Voltage	2.0	V _{IH} or V _{IL}	20 μA	—	0.0	0.1	—	0.1	—	V
		4.5			—	0.0	0.1	—	0.1	—	
		6.0			—	0.0	0.1	—	0.1	—	
		4.5 6.0		4.0 mA 5.2 mA	— —	0.17 0.18	0.26 0.26	— —	0.33 0.33	— —	0.40 0.40
I _I	Input Leakage Current	6.0	V _I = V _{CC} or GND		—	—	± 0.1	—	± 1.0	—	μA
I _{CC}	Quiescent Supply Current	6.0	V _I = V _{CC} or GND		—	—	4	—	40	—	80 μA

AC ELECTRICAL CHARACTERISTICS ($V_{CC} = 5V$, $T_A = 25^\circ C$, $C_L = 15pF$, Input $t_r = t_f = 6ns$)

Symbol	Parameter	54HC and 74HC			Unit
		Min.	Typ.	Max.	
t_{TLH} t_{THL}	Output Transition Time		4	8	ns
t_{PLH} t_{PHL}	Propagation Delay Time (BCD - Segment)		46	71	ns
t_{PHL} t_{PHL}	Propagation Delay Time BI - Segment		28	44	ns
t_{PLH} t_{PHL}	Propagation Delay Time $\overline{LT}$ - Segment		16	26	ns
t_{PHL} t_{PHL}	Propagation Delay Time LE - Segment		46	71	ns

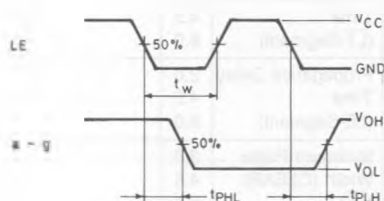
SWITCHING CHARACTERISTICS TEST WAVEFORM

Data Segment Delay Time

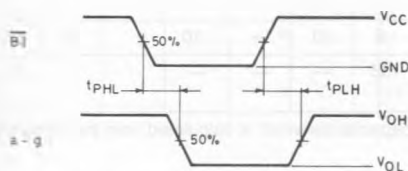


S-10229

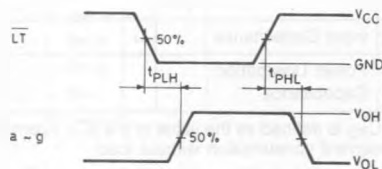
LE-Segment Delay Time



S-10230

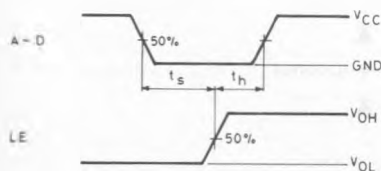
 $\overline{BI}$ -Segment Delay Time

S-10231

 $\overline{LT}$ -Segment Delay Time

S-10232

Data Set-up/Hold Time



S-10233

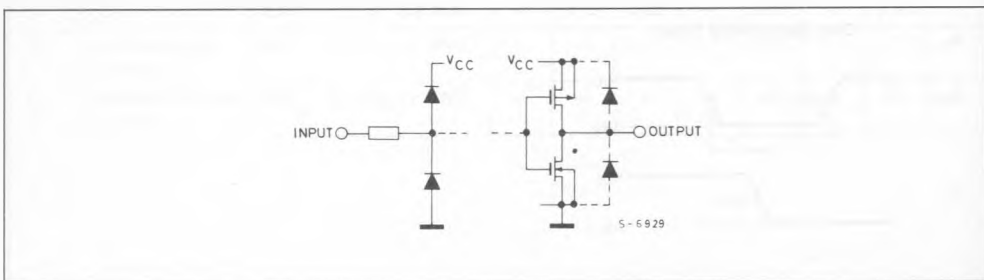
AC ELECTRICAL CHARACTERISTICS ($C_L = 50\text{pF}$, Input $t_r = t_f = 6\text{ns}$)

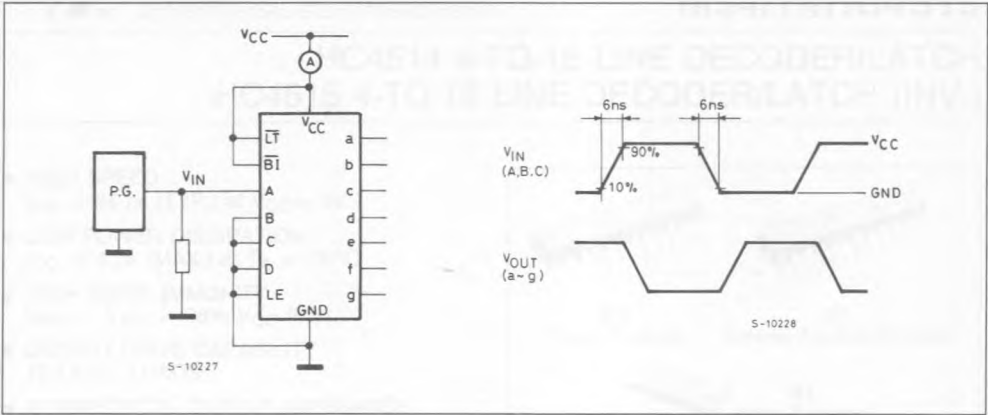
Symbol	Parameter	V_{CC}	Test Condition	$T_A = 25^\circ\text{C}$ 54HC and 74HC			-40 to 85°C 74HC		-55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time Low to High	2.0 4.5 6.0		— — —	25 6 5	60 12 10	— — —	75 15 13		90 18 15	ns
t_{THL}	Output Transition Time High to Low	2.0 4.5 6.0		— — —	30 8 7	75 15 13	— — —	95 19 16	— — —	110 22 19	ns
t_{PLH} t_{PHL}	Propagation Delay Time (BCD-Segment)	2.0 4.5 6.0		— — —	192 48 41	400 80 68	— — —	505 101 87		600 120 102	ns
t_{PLH} t_{PHL}	Propagation Delay Time (BI-Segment)	2.0 4.5 6.0		— — —	116 29 25	250 50 43	— — —	315 63 54		375 75 64	ns
t_{PLH} t_{PHL}	Propagation Delay Time (LT-Segment)	2.0 4.5 6.0		— — —	72 18 15	150 30 26	— — —	190 38 33		225 45 38	ns
t_{PLH} t_{PHL}	Propagation Delay Time (LE-Segment)	2.0 4.5 6.0		— — —	192 48 41	400 80 68	— — —	505 101 87		600 120 102	ns
$t_{W(L)}$	Minimum Pulse Width (CLEAR) (LE)	2.0 4.5 6.0		— — —	30 8 7	75 15 13	— — —	95 19 16		110 22 19	ns
t_s	Minimum Set-up Time	2.0 4.5 6.0		— — —	35 9 8	75 15 13	— — —	95 19 16		110 22 19	ns
t_h	Minimum Data Hold Time	2.0 4.5 6.0		— — —	— — —	0 0 0	— — —	0 0 0	— — —	0 0 0	ns
C_{IN}	Input Capacitance			—	5	10	—	10		10	pF
$C_{PD} (*)$	Power Dissipation Capacitance			—	136	—	—	—			pF

Note (*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load.

$$\text{Average operating current is: } I_{CC(\text{opr})} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

INPUT AND OUTPUT EQUIVALENT CIRCUIT



TEST CIRCUIT I_{CC} (Opr.)

APPLICATION CIRCUIT

Static Display Circuit

