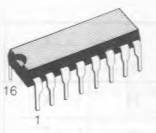
SGS-THOMSON MICROELECTRONICS

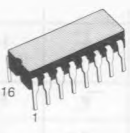
M54HC597
M74HC597

8-BIT LATCH/SHIFT REGISTER

- LOW POWER DISSIPATION
  I_{CC} = 4 μA (MAX.) at T_A = 25°C
- HIGH NOISE IMMUNITY
  V_{NIH} = V_{NIL} = 28% V_{CC} (Min.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}|$ = I_{OL} = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  t_{PLH} = t_{PHL}
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2V to 6V
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS597



B1N
Plastic Package



F1
Ceramic Frit Seal Package

M1
Micro Package

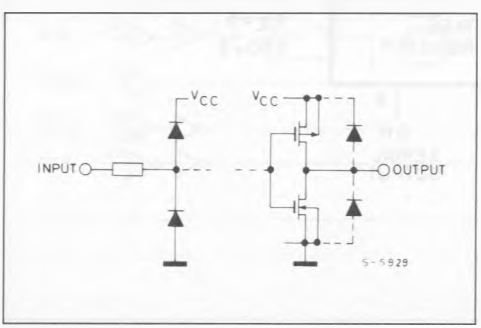
C1
Plastic Chip Carrier

ORDERING NUMBERS:
M54HC597 F1
M74HC597 B1N
M74HC597 F1
M74HC597 C1
M74HC597 M1

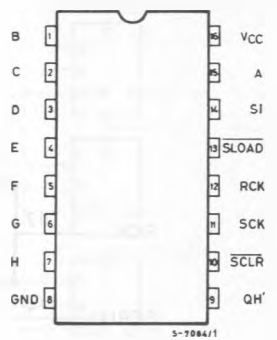
DESCRIPTION

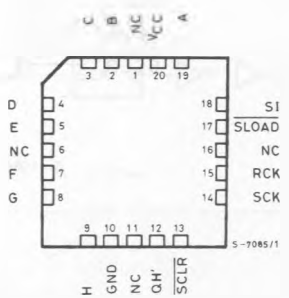
The M54/74HC597 is a high speed CMOS 8-BIT LATCH/SHIFT REGISTER fabricated in silicon gate C²MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low power consumption.
This devices comes in a 16-pin package and consist of an 8-bit storage latch feeding a parallel-in, serial-out 8-bit shift register. Both the storage register and shift register have positive-edge triggered clocks. The shift register also has direct load (from storage) and clear inputs.
All inputs are equipped with protection circuits against static discharge and transient voltage excess.

INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN CONNECTIONS (top view)





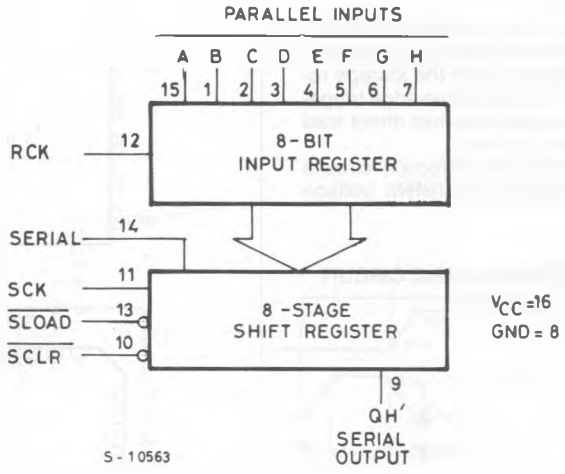
NC =
No Internal
Connection

TRUTH TABLE

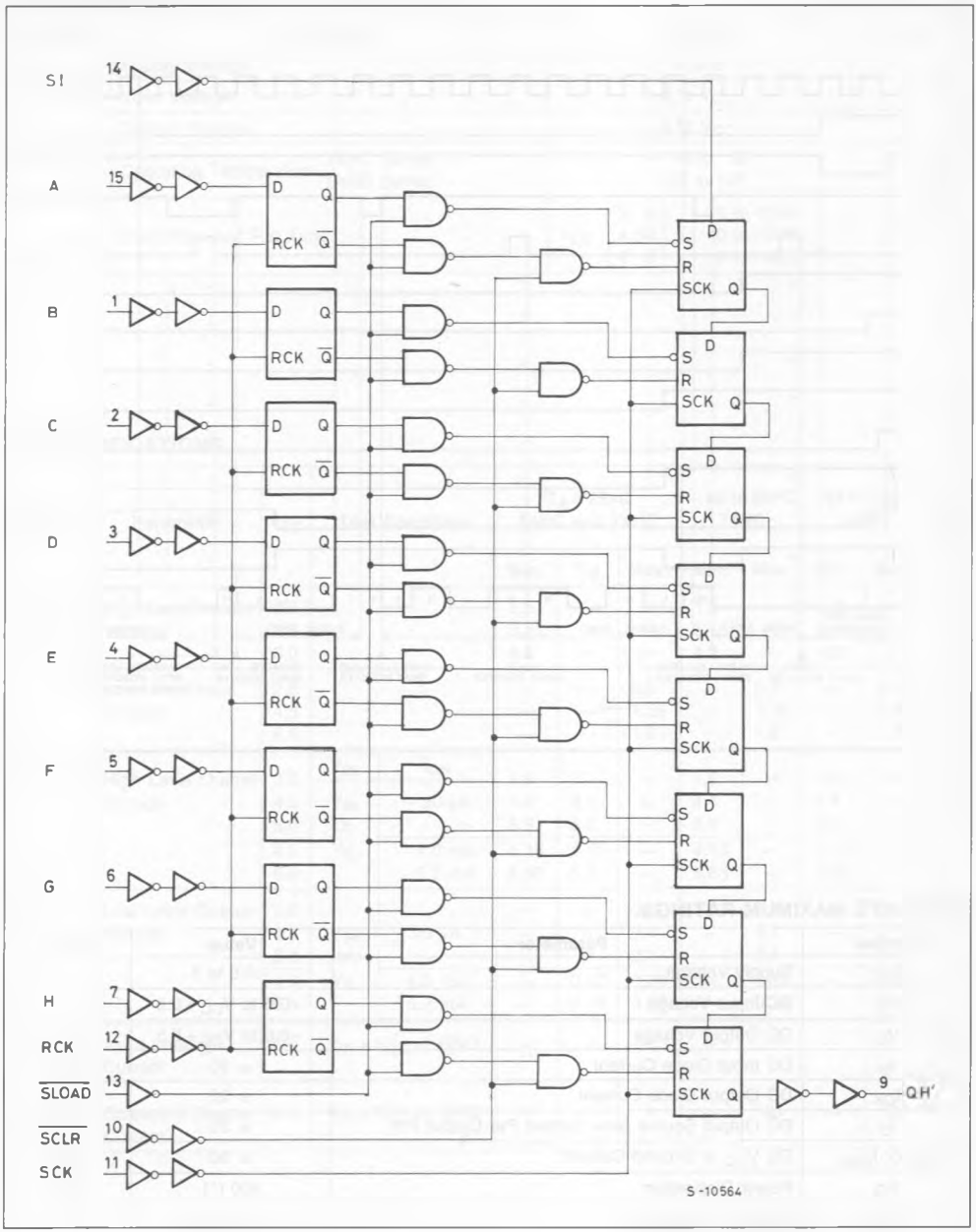
INPUTS					FUNCTION
SI	SCK	$\overline{SCLR}$	$\overline{SLOAD}$	RCK	
X	X	L	H	X	S.R. IS CLEARED TO "L"
X	X	H	L	X	INPUT REGISTER DATA IS STORE INTO S.R.
L	↑	H	H	X	FIRST STAGE OF S.R. BECOMES "L". OTHER STAGES STORE THE DATA OF PREVIOUS STAGE, RESPECTIVELY.
H	↑	H	H	X	FIRST STAGE OF S.R. BECOMES "H". OTHER STAGES STORE THE DATA OF PREVIOUS STAGE, RESPECTIVELY.
X	↓	H	H	X	STATE OF S.R. IS NOT CHANGED.
X	X	X	X	↑	INPUT DATA ON A ~ H LINE IS STORED INTO INPUT REGISTER
X	X	X	X	↓	STORAGE REGISTER STATE IS NOT CHANGED.

X = DON'T CARE

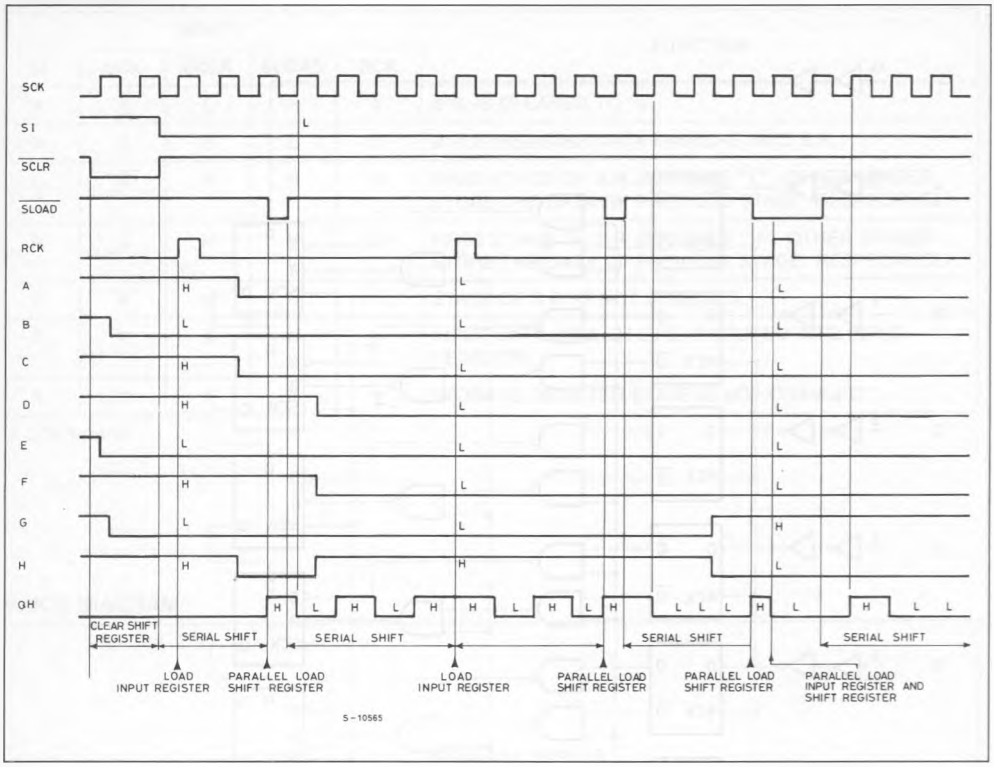
BLOCK DIAGRAM



LOGIC DIAGRAM



TIMING CHART



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to 7	V
V_I	DC Input Voltage	−0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	−0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	−65 to 150	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: ≡65°C derate to 300 mW by 10 mW/°C: 65°C to 85°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value		Unit
V_{CC}	Supply Voltage		2 to 6		V
V_I	Input Voltage		0 to V_{CC}		V
V_O	Output Voltage		0 to V_{CC}		V
T_A	Operating Temperature	74HC Series 54HC Series	– 40 to 85 – 55 to 125		°C
t_r, t_f	Input Rise and Fall Time		V_{CC} = 2 V	0 to 1000	ns
			V_{CC} = 4.5V	0 to 500	
			V_{CC} = 6 V	0 to 400	

DC SPECIFICATIONS

Symbol	Parameter	V_{CC}	Test Condition		T_A = 25°C 54HC and 74HC			– 40 to 85°C 74HC		– 55 to 125°C 54HC		Unit
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5	—	—	1.5	—	1.5	—	V
		4.5			3.15	—	—	3.15	—	3.15	—	
		6.0			4.2	—	—	4.2	—	4.2	—	
V_{IL}	Low Level Input Voltage	2.0			—	—	0.5	—	0.5	—	0.5	V
		4.5			—	—	1.35	—	1.35	—	1.35	
		6.0			—	—	1.8	—	1.8	—	1.8	
V_{OH}	High Level Output Voltage	2.0	V_{IN}	I_{OH}	1.9	2.0	—	1.9	—	1.9	—	V
		4.5	V_{IH} or V_{IL}	– 20 μA	4.4	4.5	—	4.4	—	4.4	—	
		6.0			5.9	6.0	—	5.9	—	5.9	—	
		4.5		– 4.0 mA	4.18	4.31	—	4.13	—	4.10	—	
		6.0		– 5.2 mA	5.68	5.8	—	5.63	—	5.60	—	
V_{OL}	Low Level Output Voltage	2.0	V_{IH} or V_{IL}	20 μA	—	0	0.1	—	0.1	—	0.1	V
		4.5			—	0	0.1	—	0.1	—	0.1	
		6.0			—	0	0.1	—	0.1	—	0.1	
		4.5		4.0 mA	—	0.17	0.26	—	0.33	—	0.40	
		6.0		5.2 mA	—	0.18	0.26	—	0.33	—	0.40	
I_{IN}	Input Leakage Current	6.0	V_{IN} = V_{CC} or GND		—	—	±0.1	—	±1	—	±1	μA
I_{CC}	Quiescent Supply Current	6.0	V_{IN} = V_{CC} or GND		—	—	4	—	40	—	80	

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V, T_A = 25°C, C_L = 15pF, Input $t_r = t_f$ = 6ns)

Symbol	Parameter	54HC and 74HC			Unit
		Min.	Typ.	Max.	
t_{TLH} t_{THL}	Output Transition Time		4	8	ns
t_{PLH} t_{PHL}	Propagation Delay Time (SCK - QH')		15	24	ns
t_{PLH} t_{PHL}	Propagation Delay Time (RCK - QH')		23	36	ns
t_{PHL}	Propagation Delay Time ($\overline{SLOAD}$ - QH')		19	30	ns
t_{PHL}	Propagation Delay Time ($\overline{SCLR}$ - QH')		19	30	ns
f_{MAX}	Maximum Clock Frequency	33	60		MHz

AC ELECTRICAL CHARACTERISTICS (C_L = 50pF, Input $t_r = t_f$ = 6ns)

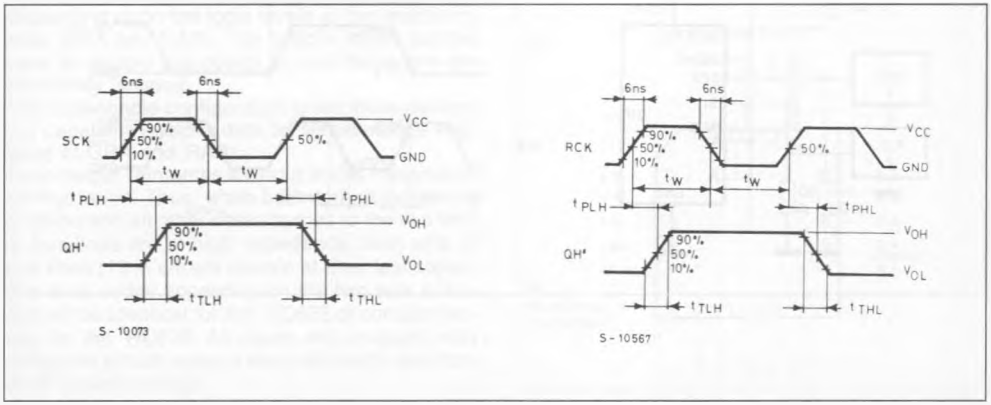
Symbol	Parameter	V_{CC}	Test Condition	T_A = 25°C 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0 4.5 6.0		— — —	30 8 7	75 15 13	— — —	95 19 16	— — —	110 22 19	ns
t_{PLH} t_{PHL}	Propagation Delay Time (SCK-QH')	2.0 4.5 6.0		— — —	72 18 15	145 29 25	— — —	180 36 31	— — —	220 44 37	ns
t_{PLH} t_{PHL}	Propagation Delay Time (RCK-QH')	2.0 4.5 6.0	$\overline{SLOAD}$ = L	— — —	108 27 23	210 42 36	— — —	265 53 45	— — —	315 63 54	ns
t_{PHL}	Propagation Delay Time ($\overline{SLOAD}$-QH')	2.0 4.5 6.0		— — —	88 22 19	175 35 30	— — —	220 44 37	— — —	265 53 45	ns
t_{PHL}	Propagation Delay Time ($\overline{SCLR}$-QH')	2.0 4.5 6.0		— — —	92 23 20	175 35 30*	— — —	220 44 37	— — —	265 53 45	ns
f_{MAX}	Maximum Clock Frequency	2.0 4.5 6.0		6 30 35	14 55 64	— — —	5 24 28	— — —	4 20 24	— — —	MHz

AC ELECTRICAL CHARACTERISTICS (Continued)

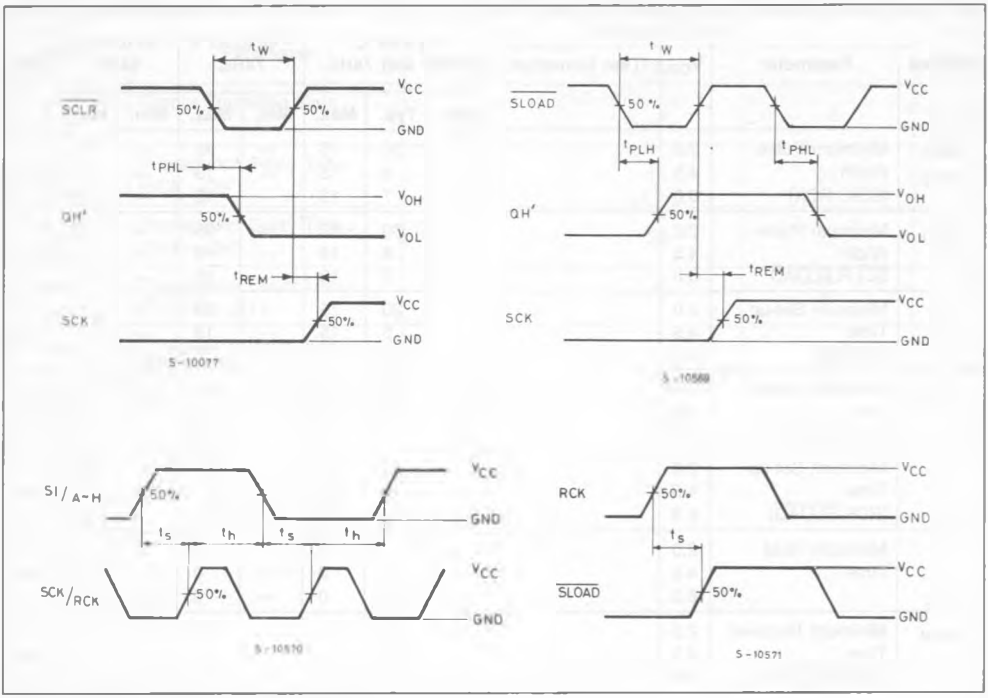
Symbol	Parameter	V_{CC}	Test Condition	T_A = 25°C 54HC and 74HC			− 40 to 85°C 74HC		− 55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
$t_{W(H)}$ $t_{W(L)}$	Minimum Pulse Width (SCK, RCK)	2.0 4.5 6.0		— — —	30 8 7	75 15 13	— — —	95 19 16	— — —	110 22 19	ns
$t_{W(L)}$	Minimum Pulse Width $\overline{SCLR}$,$\overline{SLOAD}$	2.0 4.5 6.0		— — —	30 8 7	75 15 13	— — —	95 19 16	— — —	110 22 19	ns
t_s	Minimum Set-up Time (SI-SCK)	2.0 4.5 6.0		— — —	20 5 4	75 15 13	— — —	95 19 16	— — —	110 22 19	ns
t_s	Minimum Set-up Time (A...H-RCK)	2.0 4.5 6.0		— — —	20 5 4	75 15 13	— — —	95 19 16	— — —	110 22 19	ns
t_s	Minimum Set-up Time (RCK-$\overline{SLOAD}$)	2.0 4.5 6.0		— — —	50 13 11	125 25 21	— — —	155 31 26	— — —	190 38 32	ns
t_h	Minimum Hold Time	2.0 4.5 6.0		— — —	— — —	0 0 0	— — —	0 0 0	— — —	0 0 0	ns
t_{REM}	Minimum Removal Time ($\overline{SCLR}$,$\overline{SLOAD}$)	2.0 4.5 6.0		— — —	10 3 3	50 10 9	— — —	65 13 11	— — —	75 15 13	ns
C_{IN}	Input Capacitance			—	5	10	—	10	—	10	pF
C_{PD} (*)	Power Dissipation Capacitance			—	76	—	—	—	—	—	pF

Note (*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit)
Average opeating current is: $I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$

SWITCHING CHARACTERISTICS TEST WAVEFORM



TEST WAVEFORM (Continued)



TEST CIRCUIT I_{CC} (Opr.)