SGS-THOMSON MICROELECTRONICS

M54/74HC646
M54/74HC648

HC646 OCTAL BUS TRANSCEIVER/REGISTER (3-STATE)
HC648 OCTAL BUS TRANSCEIVER/REGISTER (INVERTING-3 STATE)

- LOW POWER DISSIPATION
  I_{CC} = 4 μA (MAX.) at T_A = 25°C
- HIGH NOISE IMMUNITY
  V_{NIH} = V_{NIL} = 28% V_{CC} (Min.)
- OUTPUT DRIVE CAPABILITY
  15 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}|$ = I_{OL} = 6 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  t_{PLH} = t_{PHL}
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2V to 6V
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS646/648

B1N
Plastic Package

F1
Ceramic Frit Seal Package

M1
Micro Package

ORDERING NUMBERS:

M54HCXXXF1	M74HCXXXM1
M74HCXXXB1N	M74HCXXXF1

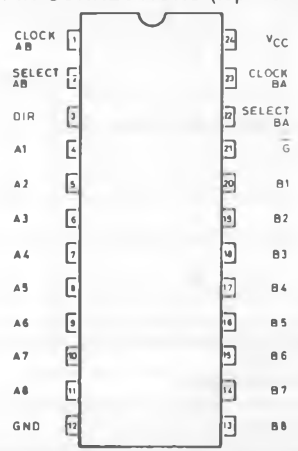
DESCRIPTION

The M54/74HC646/648 are high speed CMOS OCTAL BUS TRANSCEIVERS AND REGISTERS, (3 STATE) fabricated in silicon gate C²MOS technology. They have the same high speed performance of LSTTL combined with true CMOS low power consumption.

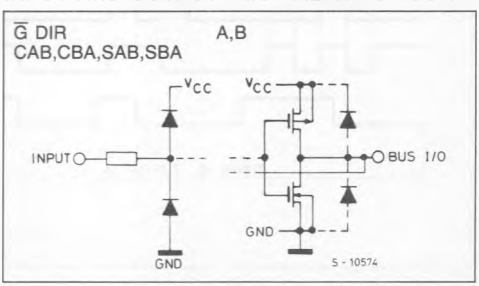
These devices consist of bus transceiver circuits with 3-state output, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal registers. Data on the A or B bus will be clocked into the registers on the low-to-high transition of the appropriate clock pin (Clock AB - or Clock BA). Enable ($\overline{G}$) and direction (DIR) pins are provided to control the transceiver functions. In the transceiver mode, data present at the high-impedance port may be stored in either register or in both.

The select controls (Select AB select BA) can multiplex stored and real-time (transparent mode) data. The direction control determines which bus will receive data when enable $\overline{G}$ is active (low).
In the isolation mode (enable $\overline{G}$ high), "A" data may be stored in one register and/or "B" data may be stored in the other register. When an output function is disabled, the input function is still enabled and may be used to store and transmit data. Only one of the two buses, A or B, may be driven at a time. All inputs are equipped with protection circuits against static discharge and transient excess voltage.

PIN CONNECTIONS (top view)



INPUT AND OUTPUT EQUIVALENT CIRCUIT



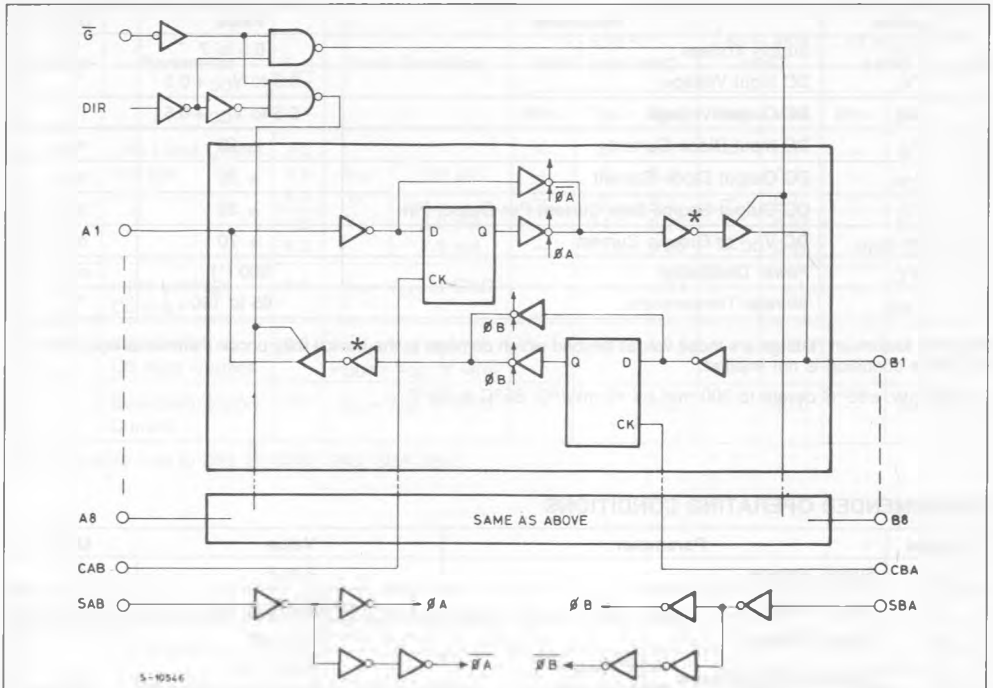
TRUTH TABLE

M54/74HC646 (The truth table for M54/74HC648 is the same as this, but with the outputs inverted)

$\overline{G}$	DIR	CAB	CBA	SAB	SBA	A	B	FUNCTION
H	X					INPUTS	INPUTS	Both the A bus and the B bus are inputs.
		X	X	X	X	Z	Z	The output functions of the A and B bus are disabled.
		↑	↑	X	X	INPUTS	INPUTS	Both the A and B bus are used for inputs to the internal flip-flops. Data at the bus will be stored on low to high transition of the clock inputs.
L	H					INPUTS	OUTPUTS	The A bus are inputs and the B bus are outputs.
		X	X*	L	X	L H	L H	The data at the A bus are displayed at the B bus.
		↑	X*	L	X	L H	L H	The data at the A bus are displayed at the B bus. The data of A bus are stored to the internal flip-flops on low to high transition of the clock pulse.
		X	X*	H	X	X	Qn	The data stored to the internal flip-flops are displayed at the B bus.
		↑	X*	H	X	L H	L H	The data at the A bus are stored to the internal flip-flops on low to high transition of the clock pulse. The states of the internal flip-flops output directly to the B bus
L	L					OUTPUTS	OUTPUTS	The B bus are inputs and the A bus are outputs.
		X*	X	X	L	L H	L H	The data at the B bus are displayed at the A bus.
		X*	↑	X	L	L H	L H	The data at the B bus are displayed at the A bus. The data of 8 bus are stored to the internal flip-flops on low to high transition of the clock pulse.
		X*	X	X	H	Qn	X	The data stored to the internal flip-flops are diplayed at the B bus.
		X*	↑	X	H	L H	L H	The data at the B bus are stored to the internal flip-flops on low to high transition of the clock pulse. The states of the internal flip-flops output directly to the A bus.

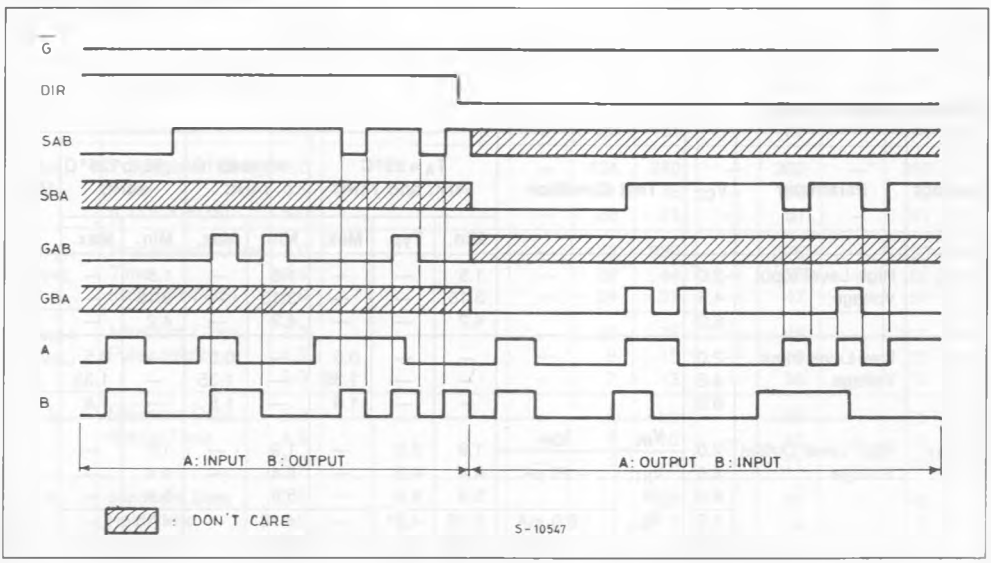
X: DON'T CARE.
Z: HIGH IMPEDANCE.
Qn: THE DATA STORED TO THE INTERNAL FLIP-FLOPS BY MOST RECENT LOW TO HIGH TRANSITION OF THE CLOCK INPUTS.
*: THE DATA AT THE A AND B BUS WILL BE STORED TO THE INTERNAL FLIP-FLOPS ON EVERY LOW TO TRANSITION OF THE CLOCK INPUTS.

LOGIC DIAGRAM (HC648)



NOTE: IN CASE OF M54/74HC646 OUTPUT INVERTER MARKED* AT A BUS AND B BUS ARE ELIMINATED.

TIMING CHART



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to 7	V
V_I	DC Input Voltage	−0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	−0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 35	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 70	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	−65 to 150	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: ≡65°C derate to 300 mW by 10 mW/°C: 65°C to 85°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value		Unit
V_{CC}	Supply Voltage		2 to 6		V
V_I	Input Voltage		0 to V_{CC}		V
V_O	Output Voltage		0 to V_{CC}		V
T_A	Operating Temperature	74HC Series 54HC Series	−40 to 85 −55 to 125		°C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V V_{CC} = 4.5 V V_{CC} = 6 V	0 to 1000 0 to 500 0 to 400		ns

DC SPECIFICATIONS

Symbol	Parameter	V_{CC}	Test Condition		T_A = 25°C 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5	—	—	1.5	—	1.5	—	V
		4.5			3.15	—	—	3.15	—	3.15	—	
		6.0			4.2	—	—	4.2	—	4.2	—	
V_{IL}	Low Level Input Voltage	2.0			—	—	0.5	—	0.5	—	0.5	V
		4.5			—	—	1.35	—	1.35	—	1.35	
		6.0			—	—	1.8	—	1.8	—	1.8	
V_{OH}	High Level Output Voltage	2.0	V_{IN}	I_{OH}	1.9	2.0	—	1.9	—	1.9	—	V
		4.5	V_{IH}	−20 μA	4.4	4.5	—	4.4	—	4.4	—	
		6.0	or		5.9	6.0	—	5.9	—	5.9	—	
		4.5	V_{IL}	−6.0 mA	4.18	4.31	—	4.13	—	4.10	—	
		6.0		−7.8 mA	5.68	5.8	—	5.63	—	5.60	—	

DC SPECIFICATIONS (Continued)

Symbol	Parameter	V_{CC}	Test Condition		$T_A = 25°C$ 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{OL}	Low Level Output Voltage	2.0	V_{IH} or V_{IL}	20 μA	—	0	0.1	—	0.1	—	0.1	V
		4.5			—	0	0.1	—	0.1	—	0.1	
		6.0			—	0	0.1	—	0.1	—	0.1	
		4.5		6.0 mA	—	0.17	0.26	—	0.33	—	0.40	
		6.0		7.8 mA	—	0.18	0.26	—	0.33	—	0.40	
I_{IN}	Input Leakage Current *	6.0	$V_{IN} = V_{CC}$ or GND		—	—	±0.1	—	±1	—	±1	μA
I_{OZ}	3-State Output Off state Current	6.0	$V_I = V_{IH}$ or V_{IL} $V_{OUT} = V_{CC}$ or GND		—	—	±0.5	—	±5.0	—	±10	
I_{CC}	Quiescent Supply Current	6.0	$V_{IN} = V_{CC}$ or GND		—	—	4.0	—	40.0	—	80.0	

*: Applicable only to DIR, $\overline{G}$, CAB, SAB, SBA input.

AC ELECTRICAL CHARACTERISTICS ($C_L = 50pF$, Input $t_r = t_f = 6ns$)

Symbol	Parameter	V_{CC}	Test Condition	$T_A = 25°C$ 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0		—	25	60	—	75	—	90	ns
		4.5		—	7	12	—	15	—	18	
		6.0		—	6	10	—	13	—	15	
t_{PLH} t_{PHL}	Propagation Delay Time (BUS-BUS)	2.0		—	92	180	—	225	—	270	ns
		4.5		—	23	36	—	45	—	54	
		6.0		—	20	31	—	38	—	46	
t_{PLH} t_{PHL}	Propagation Delay Time (CLOCK-BUS)	2.0		—	124	240	—	300	—	360	ns
		4.5		—	31	48	—	60	—	72	
		6.0		—	26	41	—	51	—	61	
t_{PLH} t_{PHL}	Propagation Delay Time (SELECT-BUS)	2.0		—	112	220	—	275	—	330	ns
		4.5		—	28	44	—	55	—	66	
		6.0		—	24	37	—	47	—	56	
$t_{W(H)}$ $t_{W(L)}$	Minimum Clock Pulse Width	2.0		—	30	75	—	95	—	110	ns
		4.5		—	8	15	—	19	—	22	
		6.0		—	7	13	—	16	—	19	
t_s	Minimum Data Set-up Time	2.0		—	5	50	—	65	—	75	ns
		4.5		—	1	10	—	13	—	15	
		6.0		—	1	9	—	11	—	13	
t_h	Minimum Data Hold Time	2.0		—	—	25	—	30	—	40	ns
		4.5		—	—	5	—	6	—	8	
		6.0		—	—	5	—	5	—	7	

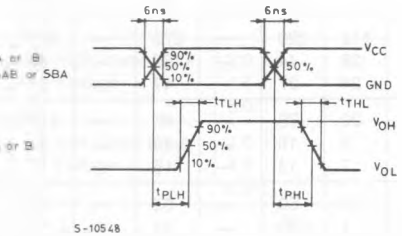
AC ELECTRICAL CHARACTERISTICS (Continued)

Symbol	Parameter	V_{CC}	Test Condition	$T_A = 25°C$ 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{PZL} t_{PZH}	3-State Output Enable Time ($\overline{G}$, DIR)	2.0 4.5 6.0	$R_L = 1k\Omega$	— — —	104 26 22	205 41 35	— — —	250 50 43	— — —	310 62 53	ns
t_{PLZ} t_{PHZ}	3-State Output Disable Time ($\overline{G}$, DIR)	2.0 4.5 6.0	$R_L = 1k\Omega$	— — —	104 29 25	210 42 36	— — —	250 50 43	— — —	310 60 50	ns
C_{IN}	Input Capacitance			—	5	10	—	10	—	10	pF
C_{OUT}	Output Capacitance		BUS I/O	—	13	—	—	—	—	—	pF
C_{PD} (*)	Power Dissipation Capacitance			—	46	—	—	—	—	—	pF

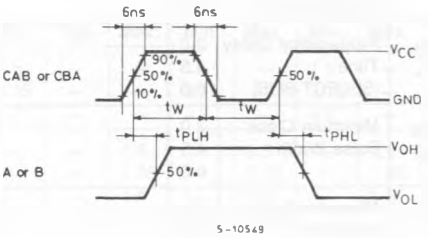
Note (*) C_{PD} is defined as the value of IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit)
Average opeating current is: $I_{CC(opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8$ (per bit)

SWITCHING CHARACTERISTICS TEST WAVEFORM

WAVEFORM 1

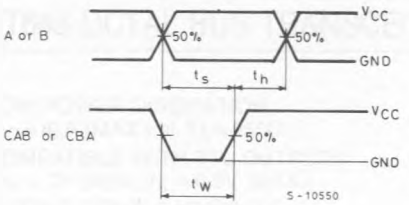


WAVEFORM 2

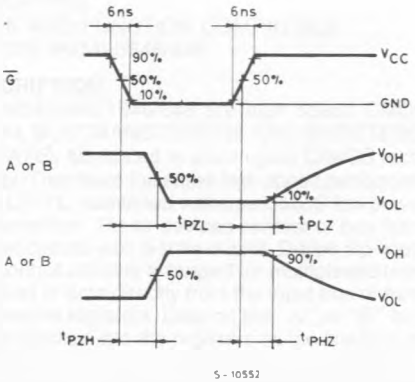


SWITCHING CHARACTERISTICS TEST WAVEFORM (Continued)

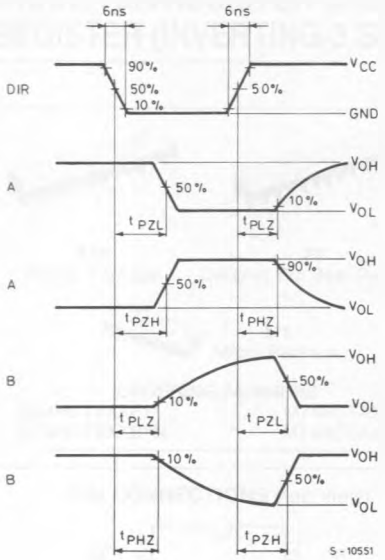
WAVEFORM 3



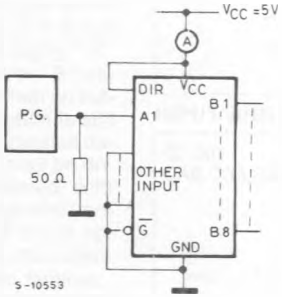
WAVEFORM 4



WAVEFORM 5



TEST CIRCUIT I_{CC} (Opr.)



INPUT TRANSITION TIME IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST