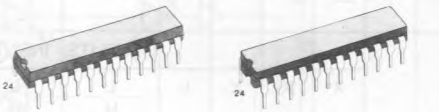
SGS-THOMSON MICROELECTRONICS

M54/74HC651
M54/74HC652

HC651 OCTAL BUS TRANSCEIVER/REGISTER (3-STATE, INV.)
HC652 OCTAL BUS TRANSCEIVER/REGISTER (3-STATE)

- LOW POWER DISSIPATION
  I_{CC} = 4 μA (MAX.) at T_A = 25°C
- HIGH NOISE IMMUNITY
  V_{NIH} = V_{NIL} = 28% V_{CC} (Min)
- OUTPUT DRIVE CAPABILITY
  15 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}|$ = I_{OL} = 6 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  t_{PLH} = t_{PHL}
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2V to 6V
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS651/652



B1N
Plastic Package

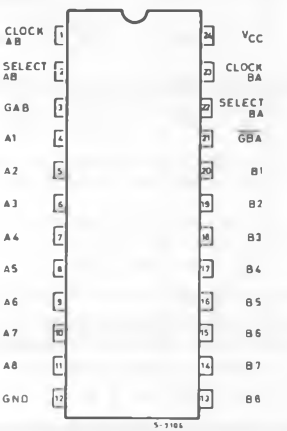
F1
Ceramic Frit Seal Package

M1
Micro Package

ORDERING NUMBERS:

M54HCXXXF1
M74HCXXXB1N
M74HCXXXM1
M74HCXXXF1

PIN CONNECTIONS (top view)



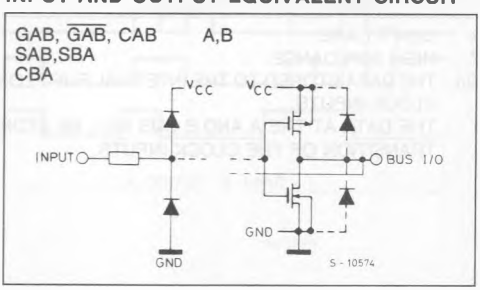
DESCRIPTION

M54/74HC651/652 are high speed CMOS OCTAL BUS TRANSCEIVERS AND REGISTERS (3-STATE), fabricated in silicon gate C²MOS technology. They have the same high speed performance of LSTTL combined with true CMOS low power consumption. These devices consist of bus transceiver circuits, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal storage registers. Enable GAB and GBA are provided to control the transceiver functions.

Select AB and Select BA control pins are provided to select whether real-time or stored data is transfered. A low input level selects real-time data, and a high selects stored data.

Data on the A or B bus, or both, can be stored in the internal D flip-flops by low-to-high transitions at the appropriate clock pins (CLOCK AB or CLOCK BA) regardless of the select or enable control pins. When select AB and select BA are in the real-time transfer mode, it is also possible to store data without using the internal D-type flip-flops by simultaneously enabling GAB and GBA. In this configuration each output reinforces its input. Thus, when all other data sources to the two sets of bus lines are at high impedance, each set of bus lines will remain at its last state. All inputs are equipped with protection circuits against static discharge and transient excess voltage.

INPUT AND OUTPUT EQUIVALENT CIRCUIT



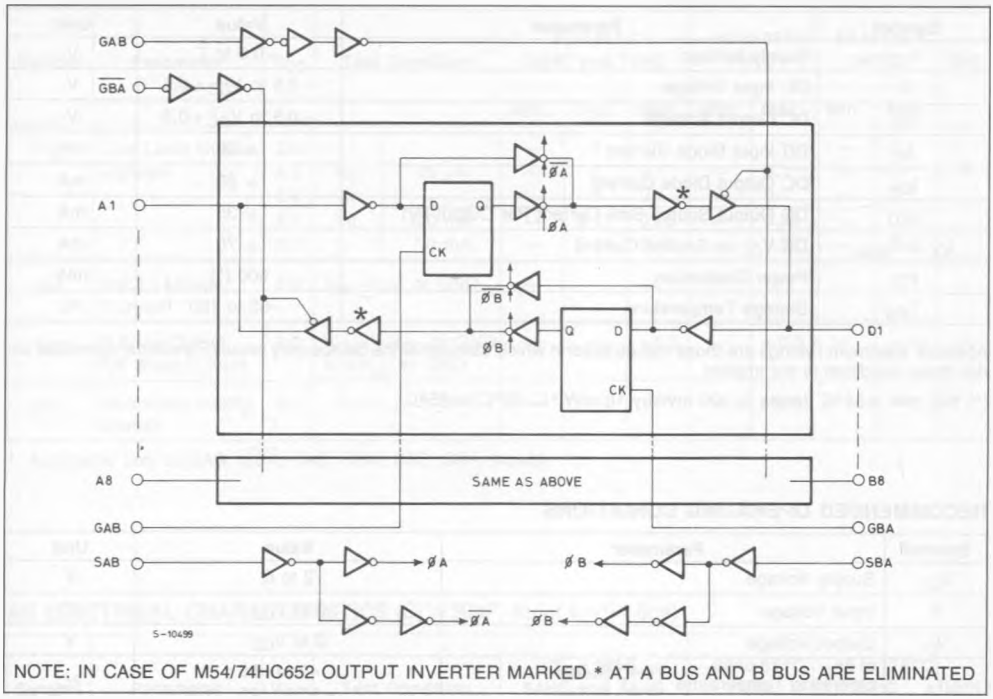
TRUTH TABLE

M54/74HC652 (The truth table for M54/74HC651 is the same as this, but with the outputs inverted)

GAB	$\overline{GBA}$	CAB	CBA	SAB	SBA	A	B	FUNCTION
L	H					INPUTS	INPUTS	Both the A bus and the B bus are inputs.
		X	X	X	X	Z	Z	The output functions of the A and B bus are disabled.
		↓	↓	X	X	INPUTS	INPUTS	Both the A and B bus are used for inputs to the internal flip-flops. Data at the bus will be stored on low to high transition of the clock inputs.
L	L					OUTPUTS	INPUTS	The A bus are outputs and the B bus are inputs.
		X*	X	X	L	L H	L H	The data at the B bus are dipayed at the A bus.
		X*	↓	X	L	L H	L H	The data at the B bus are dispayed at the A bus. The data of the B bus are stored to the internal flip-flops on low to high transition of the clock pulse.
		X*	X	X	H	Qn	X	The data stored to the internal flip-flops are dispayed at the A bus.
		X*	↓	X	H	L H	L H	The data at the B bus are stored to the internal flip-flops on low to high transition of the clock pulse. The states of the internal flip-flops output directly to the A bus.
H	H					INPUTS	OUTPUTS	The A bus are inputs and the B bus are outputs.
		X	X*	L	X	L H	L H	The data at the A bus are diplayed at the B bus.
		↓	X*	L	X	L H	L H	The data at the B bus are displayed at the A bus. The data of the B bus are stored to the internal flip-flops on low to high transition of the clock pulse.
		X	X*	H	X	X	Qn	The data stored to the internal flip-flops are displayed at the B bus.
		↓	X*	H	X	L H	L H	The data at the A bus are stored to the internal flip-flops on low to high transition of the clock pulse. The states of the internal flip-flops output directly to the B bus.
H	L					OUTPUTS	OUTPUTS	Both the A bus and the B bus are outputs.
		X	X	H	H	Qn	Qn	The data stored to the internal flip-flops are displayed at the A and B bus respectively.
		↓	↓	H	H	Qn	Qn	The output at the A bus are displayed at the B bus, the output at the B bus are displayed at the A bus respec.

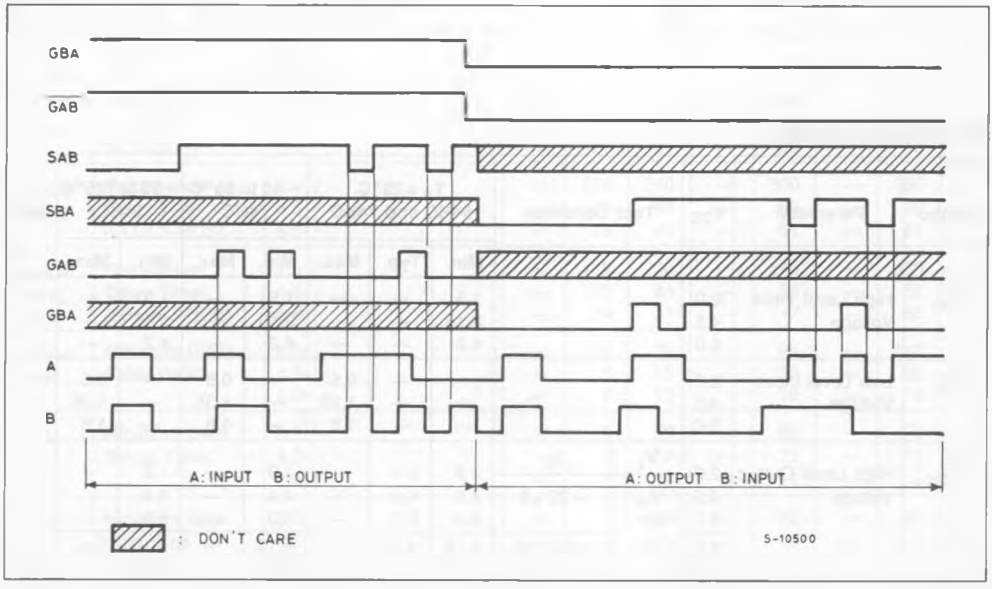
X : DON'T CARE.
Z : HIGH IMPEDANCE.
Qn : THE DATA STORED TO THE INTERNAL FLIP-FLOPS BY MOST RECENT LOW TO HIGH TRANSITION OF THE CLOCK INPUTS.
* : THE DATA AT THE A AND B BUS WILL BE STORED TO THE INTERNAL FLIP-FLOPS ON EVERY LOW TO TRANSITION OF THE CLOCK INPUTS.

LOGIC DIAGRAM (HC652)



NOTE: IN CASE OF M54/74HC652 OUTPUT INVERTER MARKED * AT A BUS AND B BUS ARE ELIMINATED

TIMING CHART



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to 7	V
V_I	DC Input Voltage	−0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	−0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 35	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 70	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	−65 to 150	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: ≅ 65°C derate to 300 mW by 10 mW/°C: 65°C to 85°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value		Unit
V_{CC}	Supply Voltage		2 to 6		V
V_I	Input Voltage		0 to V_{CC}		V
V_O	Output Voltage		0 to V_{CC}		V
T_A	Operating Temperature	74HC Series 54HC Series	−40 to 85 −55 to 125		°C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V V_{CC} = 4.5V V_{CC} = 6 V	0 to 1000 0 to 500 0 to 400		ns

DC SPECIFICATIONS

Symbol	Parameter	V_{CC}	Test Condition		T_A = 25°C 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5	—	—	1.5	—	1.5	—	V
		4.5			3.15	—	—	3.15	—	3.15	—	
		6.0			4.2	—	—	4.2	—	4.2	—	
V_{IL}	Low Level Input Voltage	2.0			—	—	0.5	—	0.5	—	0.5	V
		4.5			—	—	1.35	—	1.35	—	1.35	
		6.0			—	—	1.8	—	1.8	—	1.8	
V_{OH}	High Level Output Voltage	2.0	V_I	I_O	1.9	2.0	—	1.9	—	1.9	—	V
		4.5	V_{IH} or V_{IL}	−20 μA	4.4	4.5	—	4.4	—	4.4	—	
		6.0			5.9	6.0	—	5.9	—	5.9	—	
		4.5		−6.0 mA	4.18	4.31	—	4.13	—	4.10	—	
		6.0		−7.8 mA	5.68	5.8	—	5.63	—	5.60	—	

DC SPECIFICATIONS (Continued)

Symbol	Parameter	V_{CC}	Test Condition		$T_A = 25°C$ 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{OL}	Low Level Output Voltage	2.0	V_{IH} or V_{IL}	20 μA	—	0	0.1	—	0.1	—	0.1	V
		4.5			—	0	0.1	—	0.1	—	0.1	
		6.0			—	0	0.1	—	0.1	—	0.1	
		4.5		6.0 mA	—	0.17	0.26	—	0.33	—	0.40	
		6.0		7.8 mA	—	0.18	0.26	—	0.33	—	0.40	
I_{IN}	Input Leakage Current*	6.0	$V_{IN} = V_{CC}$ or GND		—	—	±0.1	—	±1	—	±1	μA
I_{OZ}	3-State Output Off State Current	6.0	$V_{OUT} = V_{CC}$ or GND $V_I = V_{CC}$ or GND		—	—	±0.5	—	±0.5	—	±10	
I_{CC}	Quiescent Supply Current	6.0	$V_I = V_{CC}$ or GND		—	—	4	—	40	—	80	

*: Applicable only to GAB, $\overline{GBA}$, CAB, CBA, SAB, SBA, inputs.

AC ELECTRICAL CHARACTERISTICS ($C_L = 50pF$, Input $t_r = t_f = 6ns$)

Symbol	Parameter	V_{CC}	Test Condition	$T_A = 25°C$ 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0		—	25	60	—	75	—	90	ns
		4.5		—	7	12	—	15	—	18	
		6.0		—	6	10	—	13	—	15	
t_{PLH} t_{PHL}	Propagation Delay Time (BUS-BUS)	2.0		—	92	180	—	225	—	270	ns
		4.5		—	23	36	—	45	—	54	
		6.0		—	20	31	—	38	—	46	
t_{PLH} t_{PHL}	Propagation Delay Time (CLOCK-BUS)	2.0		—	124	240	—	300	—	360	ns
		4.5		—	31	48	—	60	—	72	
		6.0		—	26	41	—	51	—	61	
t_{PLH} t_{PHL}	Propagation Delay Time (SELECT-BUS)	2.0		—	112	220	—	275	—	330	ns
		4.5		—	28	44	—	55	—	66	
		6.0		—	24	37	—	47	—	56	
$t_{W(H)}$ $t_{W(L)}$	Minimum Clock Pulse Width	2.0		—	30	75	—	95	—	110	ns
		4.5		—	8	15	—	19	—	22	
		6.0		—	7	13	—	16	—	19	
t_s	Minimum Data Set-up Time	2.0		—	5	50	—	65	—	75	ns
		4.5		—	1	10	—	13	—	15	
		6.0		—	1	9	—	11	—	13	
t_h	Minimum Data Hold Time	2.0		—	—	25	—	30	—	40	ns
		4.5		—	—	5	—	6	—	8	
		6.0		—	—	5	—	5	—	7	

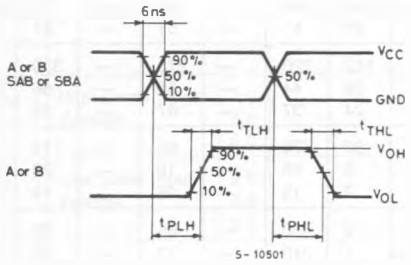
AC ELECTRICAL CHARACTERISTICS (Continued)

Symbol	Parameter	V_{CC}	Test Condition	T_A = 25°C 54HC and 74HC			− 40 to 85°C 74HC		− 55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{PZL} t_{PZH}	3-State Output Enable Time	2.0 4.5 6.0	R_L = 1kΩ	— — —	100 25 21	180 36 31	— — —	225 45 38	— — —	270 54 46	ns
t_{PZL} t_{PZH}	3-State Output Disable Time	2.0 4.5 6.0	R_L = 1kΩ	— — —	88 22 19	170 34 29	— — —	215 43 37	— — —	255 51 43	ns
C_{IN}	Input Capacitance			—	5	10	—	10	—	10	pF
C_{OUT}	Output Capacitance		BUS I/O	—	13	—	—	—	—	—	pF
C_{PD} (*)	Power Dissipation Capacitance			—	46	—	—	—	—	—	

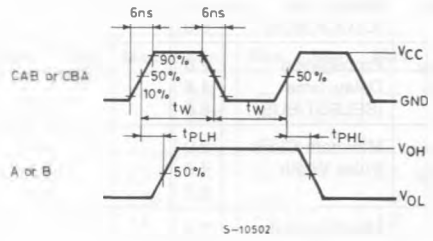
Note (*) C_{PD} is defined as the value of IC's internal equivalent capacitance which is calculated from the operating current consumption without load (refer to Test circuit).
Average operating current can be obtained by equation hereunder.
$I_{CC(opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8$ (per bit)

SWITCHING CHARACTERISTICS TEST CIRCUIT AND WAVEFORM

WAVEFORM 1

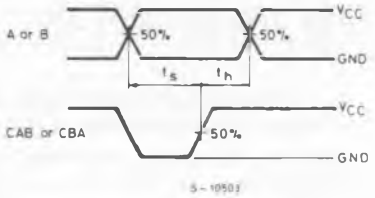


WAVEFORM 2

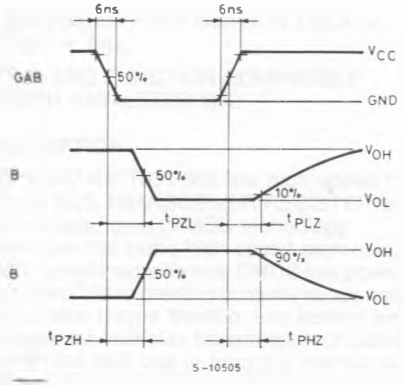


SWITCHING CHARACTERISTICS TEST CIRCUIT AND WAVEFORM (Continued)

WAVEFORM 3

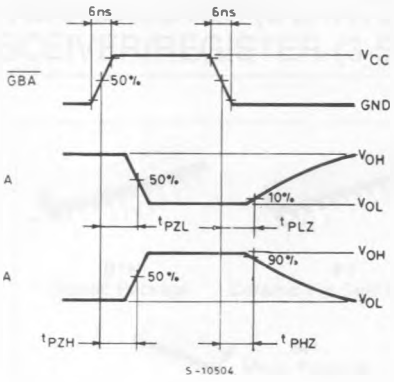


WAVEFORM 4



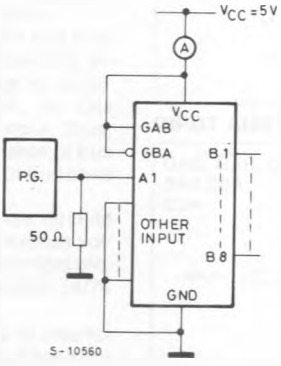
$\overline{GBA}$ = "H"

WAVEFORM 5



GAB = "L"

TEST WAVEFORM I_{CC} (Opr.)



INPUT TRANSITION TIME IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST