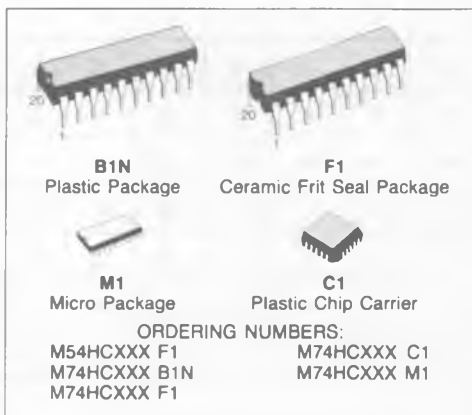


## HC696 U/D DECADE COUNTER/REGISTER (3-STATE) HC697 U/D 4-BIT BINARY COUNTER/REGISTER (3-STATE)

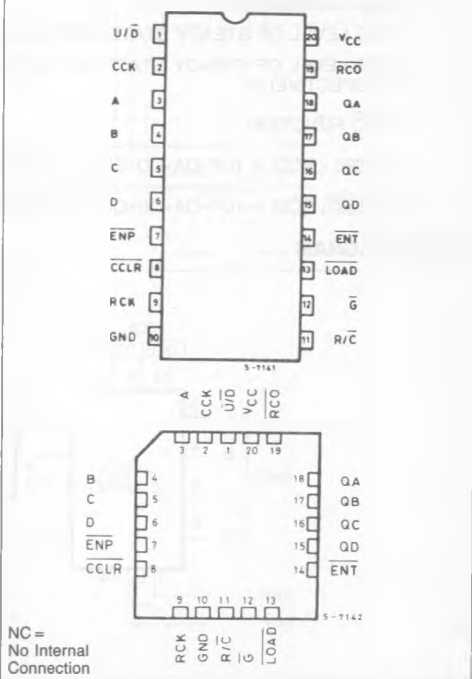
- **HIGH SPEED**  
 $f_{MAX} = 33\text{MHz}$  (TYP.) at  $V_{CC} = 5\text{V}$
- **LOW POWER DISSIPATION**  
 $I_{CC} = 4\ \mu\text{A}$  (MAX.) at  $T_A = 25^\circ\text{C}$
- **HIGH NOISE IMMUNITY**  
 $V_{NIH} = V_{NIL} = 28\% V_{CC}$  (MIN.)
- **OUTPUT DRIVE CAPABILITY**  
 15 LSTTL LOADS (FOR  $Q_A$  to  $Q_D$ )  
 10 LSTTL LOADS (FOR RCO)
- **SYMMETRICAL OUTPUT IMPEDANCE**  
 $|I_{OH}| = I_{OL} = 6\ \text{mA}$  (MIN.) FOR  $Q_A$  to  $Q_D$   
 $|I_{OH}| = I_{OL} = 4\ \text{mA}$  (MIN.) FOR RCO OUTPUT
- **BALANCED PROPAGATION DELAYS**  
 $t_{PLH} = t_{PHL}$
- **WIDE OPERATING VOLTAGE RANGE**  
 $V_{CC}(\text{OPR}) = 2\text{V}$  to  $6\text{V}$
- **PIN AND FUNCTION COMPATIBLE**  
 WITH LSTTL 54/74LS696/697

### DESCRIPTION

The HC696/697 are high speed CMOS up/down counters fabricated with silicon gate C<sup>2</sup>MOS technology. They achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation. The HC696 is a BCD DECADE COUNTER, and the HC697 is 4-BIT BINARY COUNTER. Both devices have register. They count on the positive edge of the counter clock input (CCK) when selected by the "Counter Mode". If the input U/D is held "H", the internal counter counts up, and held "L", counts down. The internal counter's outputs are stored in the output register at the positive edge of register clock (RCK). The outputs (QA - QD) are internal counter outputs or register outputs respectively and are selected by R/C. The clear function are cleared asynchronously to the clock. All inputs are equipped with protection circuits against static discharge and transient excess voltage.



### PIN CONNECTIONS (top view)



TRUTH TABLE

INPUTS									OUTPUTS				FUNCTION
$\overline{\text{CCLR}}$	$\overline{\text{LOAD}}$	$\overline{\text{ENP}}$	$\overline{\text{ENT}}$	$\text{CCK}$	$\text{U/D}$	$\text{RCK}$	$\text{R/C}$	$\overline{\text{G}}$	$\text{QA}$	$\text{QB}$	$\text{QC}$	$\text{QD}$	
X	X	X	X	X	X	X	X	H	Z	Z	Z	Z	HIGH IMPEDANCE
L	X	X	X	X	X	X	L	L	L	L	L	L	CLEAR COUNTER
H	L	X	X	$\uparrow$	X	X	L	L	a	b	c	d	LOAD COUNTER
H	H	H	X	$\uparrow$	X	X	L	L	NO CHANGE				NO COUNT
H	H	X	H	$\uparrow$	X	X	L	L	NO CHANGE				NO COUNT
H	H	L	L	$\uparrow$	H	X	L	L	COUNT UP				COUNT UP
H	H	L	L	$\uparrow$	L	X	L	L	COUNT DOWN				COUNT DOWN
H	X	X	X	$\downarrow$	X	X	L	L	NO CHANGE				NO COUNT
X	X	X	X	X	X	$\uparrow$	H	L	a'	b'	c'	d'	LOAD REGISTER
X	X	X	X	X	X	$\downarrow$	H	L	NO CHANGE				NO LOAD

X : DON'T CARE

Z : HIGH IMPEDANCE

a-d : THE LEVEL OF STEADY STATE INPUT AT INPUTS A THROUGH D RESPECTIVELY.

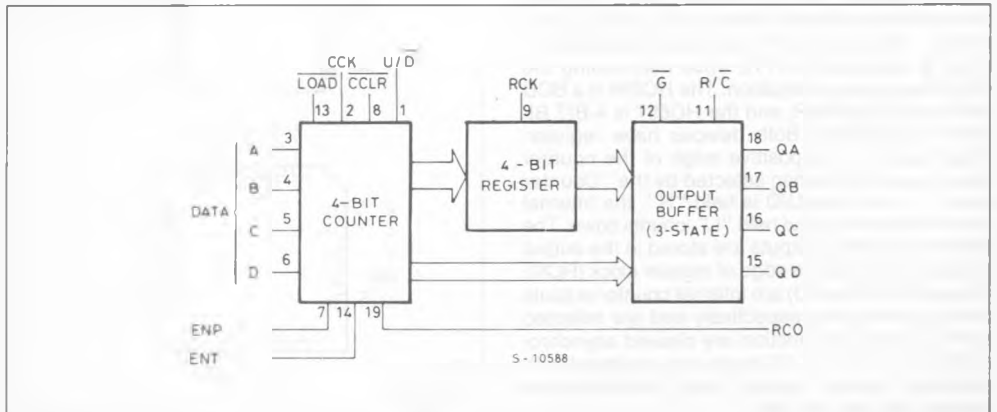
a'-d' : THE LEVEL OF STEADY STATE OUTPUTS AT INTERNAL COUNTER OUTPUTS QA' THROUGH QD' RESPECTIVELY.

RCO FUNCTION

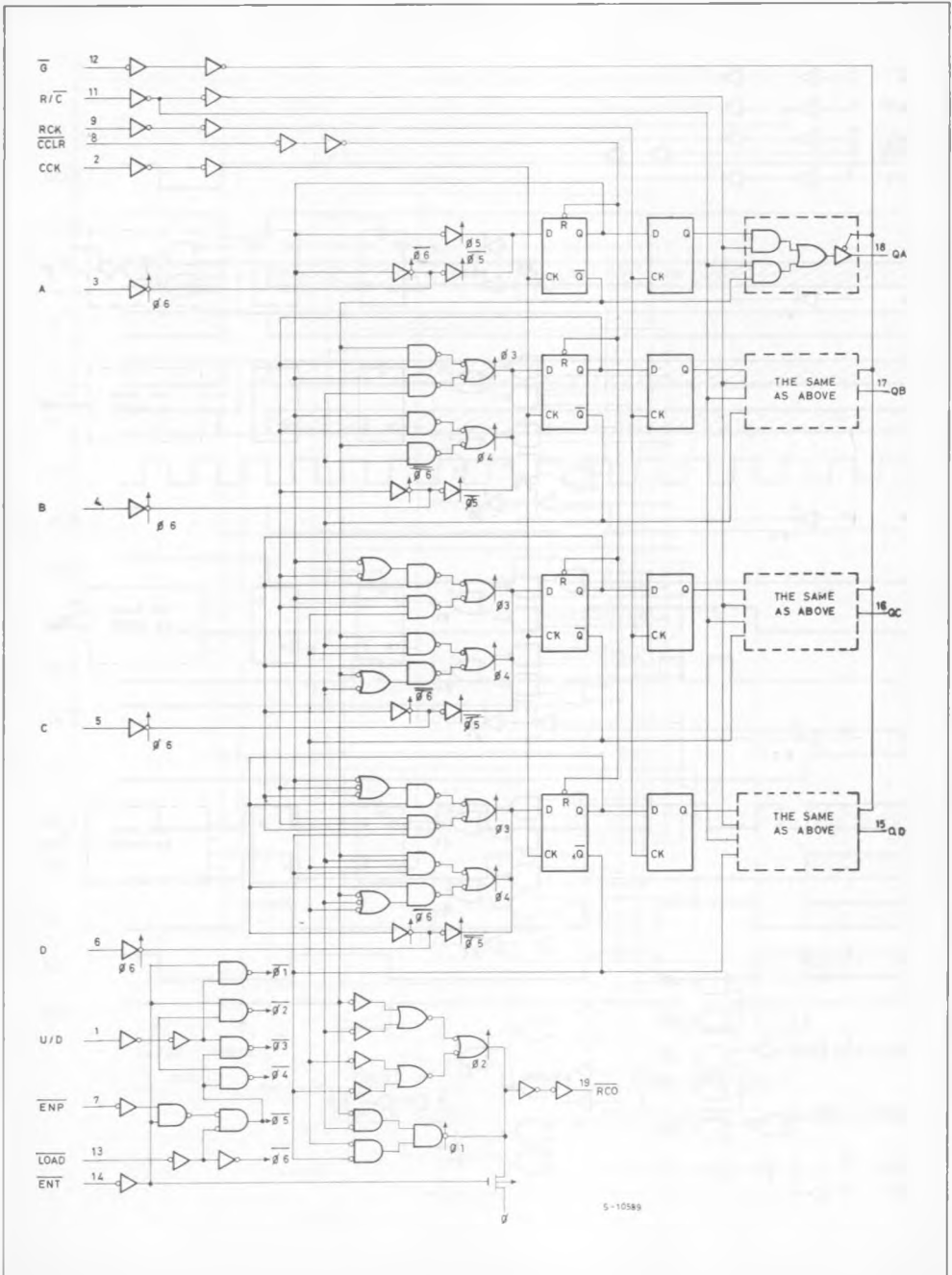
$$\text{HC696 - RCO} = (\text{UP} \cdot \text{QA} \cdot \text{QD} \cdot \text{ENT} + \overline{\text{UP}} \cdot \overline{\text{QA}} \cdot \overline{\text{QB}} \cdot \overline{\text{QC}} \cdot \overline{\text{QD}} \cdot \text{ENT})$$

$$\text{HC697 - RCO} = (\text{UP} \cdot \text{QA} \cdot \text{QB} \cdot \text{QC} \cdot \text{QD} \cdot \text{ENT} + \overline{\text{UP}} \cdot \overline{\text{QA}} \cdot \overline{\text{QB}} \cdot \overline{\text{QC}} \cdot \overline{\text{QD}} \cdot \text{ENT})$$

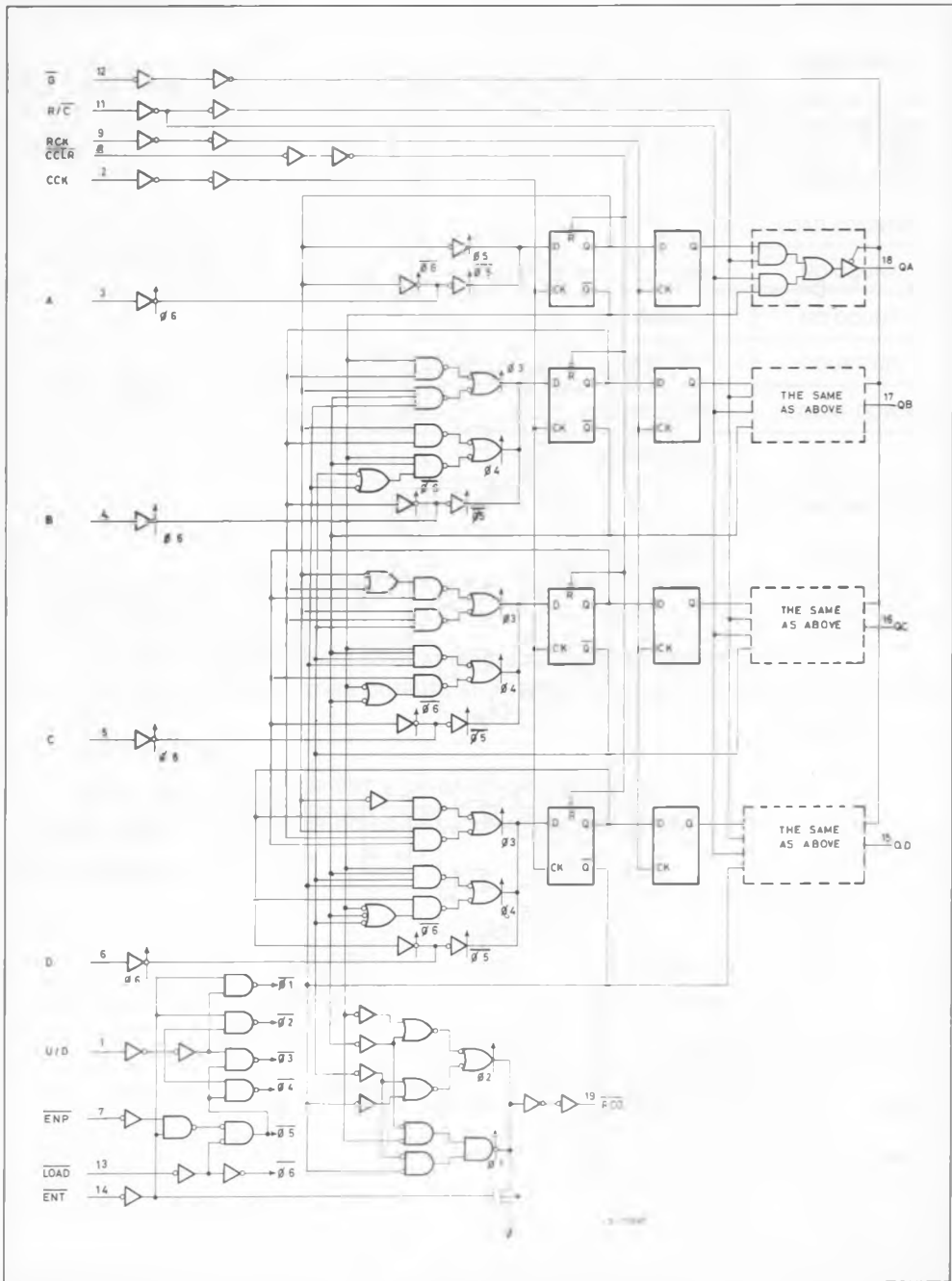
BLOCK DIAGRAM



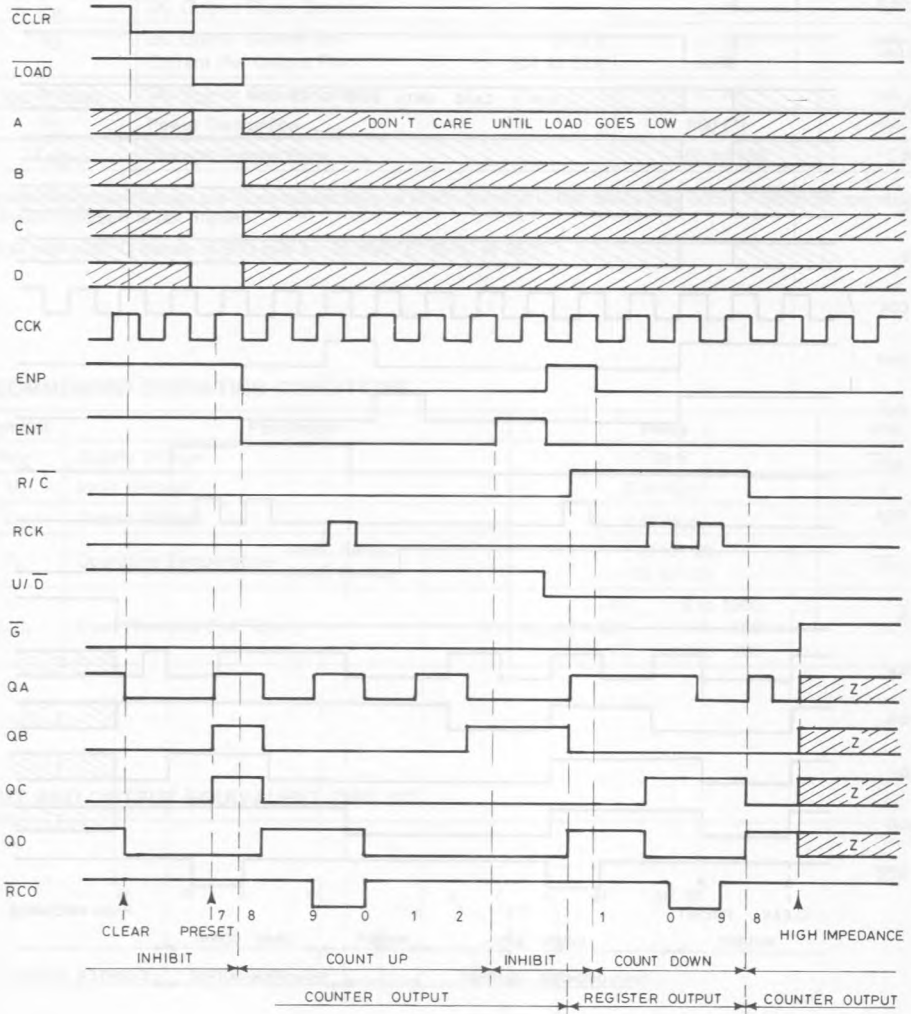
## LOGIC DIAGRAM (HC696)



LOGIC DIAGRAM (HC697)

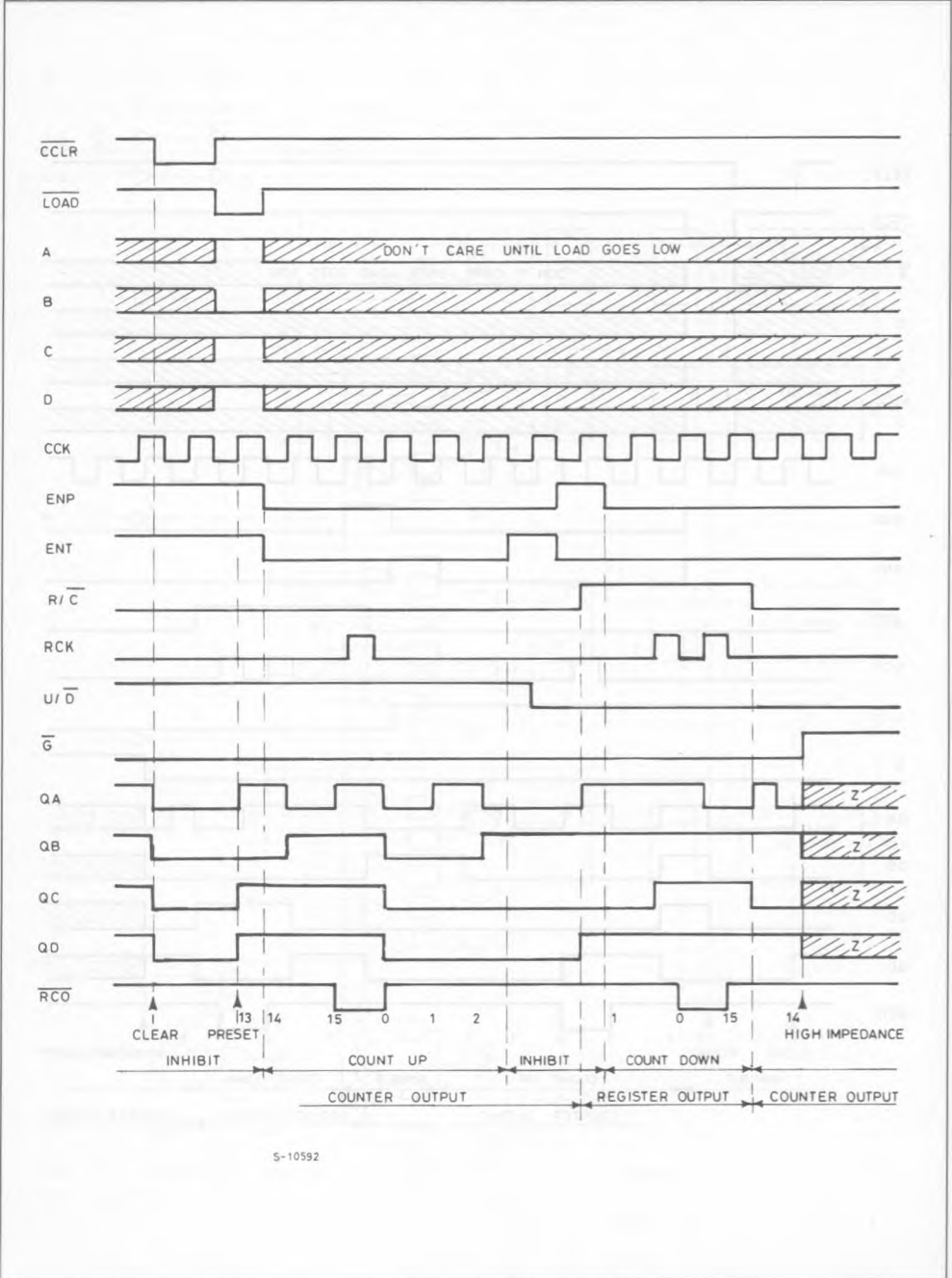


## TIMING CHART (HC696)



5-10591

TIMING CHART (HC697)



## ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
$V_{CC}$	Supply Voltage	- 0.5 to 7	V
$V_I$	DC Input Voltage	- 0.5 to $V_{CC} + 0.5$	V
$V_O$	DC Output Voltage	- 0.5 to $V_{CC} + 0.5$	V
$I_{IK}$	DC Input Diode Current	$\pm 20$	mA
$I_{OK}$	DC Output Diode Current	$\pm 20$	mA
$I_O$	DC Output Source Sink Current Per Output Pin (RCO) (QA to QD)	$\pm 20$ $\pm 35$	mA
$I_{CC}$ or $I_{GND}$	DC $V_{CC}$ or Ground Current	$\pm 70$	mA
$P_D$	Power Dissipation	500 (*)	mW
$T_{stg}$	Storage Temperature	- 65 to 150	$^{\circ}C$

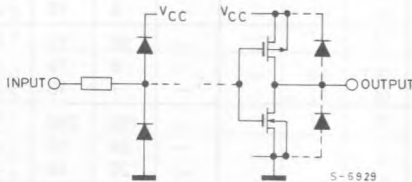
Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(\*) 500 mW:  $\cong 65^{\circ}C$  derate to 300 mW by 10 mW/ $^{\circ}C$ :  $65^{\circ}C$  to  $85^{\circ}C$

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
$V_{CC}$	Supply Voltage	2 to 6	V
$V_I$	Input Voltage	0 to $V_{CC}$	V
$V_O$	Output Voltage	0 to $V_{CC}$	V
$T_A$	Operating Temperature 74HC Series 54HC Series	- 40 to 85 - 55 to 125	$^{\circ}C$
$t_r, t_f$	Input Rise and Fall Time	$V_{CC} \begin{cases} 2 \text{ V} & 0 \text{ to } 1000 \\ 4.5 \text{ V} & 0 \text{ to } 500 \\ 6 \text{ V} & 0 \text{ to } 400 \end{cases}$	ns

## INPUT AND OUTPUT EQUIVALENT CIRCUIT



## DC SPECIFICATIONS

Symbol	Parameter	V <sub>CC</sub>	Test Condition	T <sub>A</sub> = 25°C 54HC and 74HC			- 40 to 85°C 74HC		- 55 to 125°C 54HC		Unit	
				Min	Typ	Max	Min	Max	Min	Max		
V <sub>IH</sub>	High Level Input Voltage	2.0		1.5	—	—	1.5	—	1.5	—	V	
		4.5		3.15	—	—	3.15	—	3.15	—		
		6.0		4.2	—	—	4.2	—	4.2	—		
V <sub>IL</sub>	Low Level Input Voltage	2.0		—	—	0.5	—	0.5	—	0.5	V	
		4.5		—	—	1.35	—	1.35	—	1.35		
		6.0		—	—	1.8	—	1.8	—	1.8		
V <sub>OH</sub>	High Level Output Voltage	2.0	V <sub>IN</sub>	I <sub>OH</sub>	1.9	2.0	—	1.9	—	1.9	—	V
		4.5	V <sub>IH</sub> or V <sub>IL</sub>	-20 μA	4.4	4.5	—	4.4	—	4.4	—	
		6.0			5.9	6.0	—	5.9	—	5.9	—	
		4.5	Q <sub>A</sub> -Q <sub>H</sub>	-6.0 mA -7.8 mA	4.18	4.31	—	4.13	—	4.10	—	
		6.0			5.68	5.8	—	5.63	—	5.60	—	
		4.5	RCO	-4.0 mA -5.2 mA	4.18	4.31	—	4.13	—	4.10	—	
6.0	5.68	5.8			—	5.63	—	5.60	—			
V <sub>OL</sub>	Low Level Output Voltage	2.0	V <sub>IN</sub>	I <sub>OL</sub>	—	0	0.1	—	0.1	—	0.1	V
		4.5	V <sub>IH</sub> or V <sub>IL</sub>	20 μA	—	0	0.1	—	0.1	—	0.1	
		6.0			—	0	0.1	—	0.1	—	0.1	
		4.5	Q <sub>A</sub> -Q <sub>H</sub>	6.0 mA 7.8 mA	—	0.17	0.26	—	0.33	—	0.40	
		6.0			—	0.18	0.26	—	0.33	—	0.40	
		4.5	RCO	4.0 mA 5.2 mA	—	0.17	0.26	—	0.33	—	0.40	
6.0	—	0.18			0.26	—	0.33	—	0.40			
I <sub>OZ</sub>	3-State Off Leak Current	6.0	V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> V <sub>OUT</sub> = V <sub>CC</sub> or GND		—	—	±0.5	—	±5.0	—	±10	
I <sub>IN</sub>	Input Leakage Current	6.0	V <sub>IN</sub> = V <sub>CC</sub> or GND		—	—	±0.1	—	±1.0	—	±1.0	
I <sub>CC</sub>	Quiescent Supply Current	6.0	V <sub>IN</sub> = V <sub>CC</sub> or GND		—	—	4.0	—	40.0	—	80.0	

AC ELECTRICAL CHARACTERISTICS (C<sub>L</sub> = 50pF, Input t<sub>r</sub> = t<sub>f</sub> = 6ns)

Symbol	Parameter	V <sub>CC</sub>	Test Condition	T <sub>A</sub> = 25°C 54HC and 74HC			- 40 to 85°C 74HC		- 55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t <sub>TLH</sub> t <sub>THL</sub>	Output Transition Time (Q)	2.0		—	25	60	—	75	—	90	ns
		4.5		—	7	12	—	15	—	18	
		6.0		—	6	10	—	13	—	15	
t <sub>TLH</sub> t <sub>THL</sub>	Output Transition Time (RCO)	2.0		—	30	75	—	95	—	110	ns
		4.5		—	8	15	—	19	—	22	
		6.0		—	7	13	—	16	—	19	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay Time (CCK-Q)	2.0		—	136	260	—	325	—	390	ns
		4.5		—	34	52	—	65	—	78	
		6.0		—	29	44	—	55	—	66	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay Time (RCK-Q)	2.0		—	116	225	—	280	—	340	ns
		4.5		—	29	45	—	56	—	68	
		6.0		—	25	38	—	48	—	58	



## AC ELECTRICAL CHARACTERISTICS (Continued)

Symbol	Parameter	V <sub>CC</sub>	Test Condition	T <sub>A</sub> = 25°C 54HC and 74HC			- 40 to 85°C 74HC		- 55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay Time (CCK-RCO)	2.0 4.5 6.0		— — —	160 40 34	305 61 52	— — —	385 77 66	— — —	460 92 78	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay Time (R/C-Q)	2.0 4.5 6.0		— — —	100 25 21	195 39 33	— — —	245 49 42	— — —	295 59 50	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay Time (ENT-RCO)	2.0 4.5 6.0		— — —	116 29 25	225 45 38	— — —	280 56 48	— — —	340 68 58	ns
t <sub>PHL</sub>	Propagation Delay Time (CCLR-Q)	2.0 4.5 6.0		— — —	148 37 31	285 57 48	— — —	355 71 60	— — —	430 86 73	ns
t <sub>PHL</sub>	Propagation Delay Time (CCLR-RCO)	2.0 4.5 6.0		— — —	172 43 37	325 65 55	— — —	405 81 69	— — —	490 98 83	ns
f <sub>MAX</sub>	Maximum Clock Frequency	2.0 4.5 6.0		4 20 24	8 30 35	— — —	3 16 19	— — —	3 13 15	— — —	MHz
t <sub>W(H)</sub> t <sub>W(L)</sub>	Minimum Pulse Width (CCK, RCK)	2.0 4.5 6.0		— — —	30 8 7	75 15 13	— — —	95 19 16	— — —	110 22 19	ns
t <sub>W(L)</sub>	Minimum Pulse Width (CCLR)	2.0 4.5 6.0		— — —	30 8 7	75 15 13	— — —	95 19 16	— — —	110 22 19	ns
t <sub>REM</sub>	Minimum Removal Time (CCLR)	2.0 4.5 6.0		— — —	— — —	5 5 5	— — —	5 5 5	— — —	5 5 5	ns
t <sub>S</sub>	Minimum Set-up Time (LOAD, ENT, ENP)	2.0 4.5 6.0		— — —	96 24 20	225 45 38	— — —	280 56 48	— — —	340 68 58	ns
t <sub>S</sub>	Minimum Set-up Time (A, B, C, D)	2.0 4.5 6.0		— — —	20 5 4	75 15 13	— — —	95 19 16	— — —	110 22 19	ns
t <sub>S</sub>	Minimum Set-up Time (CCK-RCK)	2.0 4.5 6.0		— — —	52 13 11	125 25 21	— — —	155 31 26	— — —	190 38 32	ns
t <sub>S</sub>	Minimum Set-up Time (U/D)	2.0 4.5 6.0		— — —	64 16 14	150 30 26	— — —	190 38 33	— — —	225 45 38	ns
t <sub>H</sub>	Minimum Hold Time	2.0 4.5 6.0		— — —	— — —	0 0 0	— — —	0 0 0	— — —	0 0 0	ns

AC ELECTRICAL CHARACTERISTICS (Continued)

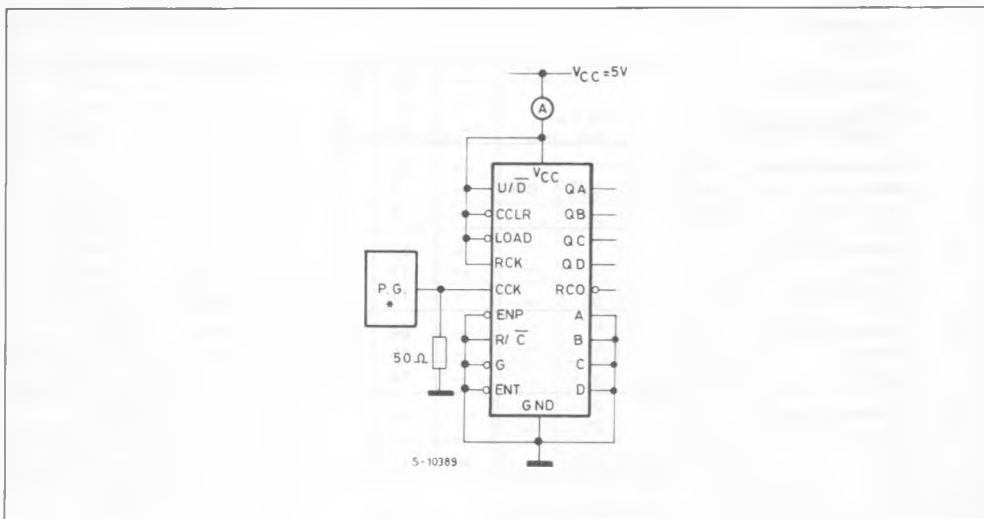
Symbol	Parameter	V <sub>CC</sub>	Test Condition	T <sub>A</sub> = 25°C 54HC and 74HC			- 40 to 85°C 74HC		- 55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t <sub>PZL</sub> t <sub>PZH</sub>	3-State Output Enable Time	2.0	R <sub>L</sub> = 1kΩ	—	64	130	—	165	—	195	ns
		4.5		—	16	26	—	33	—	39	
		6.0		—	14	22	—	28	—	33	
t <sub>PLZ</sub> t <sub>PHZ</sub>	3-State Output Disable Time	2.0	R <sub>L</sub> = 1kΩ	—	92	185	—	230	—	280	ns
		4.5		—	23	37	—	46	—	56	
		6.0		—	20	31	—	39	—	48	
C <sub>IN</sub>	Input Capacitance			—	5	10	—	10	—	10	pF
C <sub>PD</sub> (*)	Power Dissipation Capacitance		HC696	—	90	—	—	—	—	—	pF
			HC697	—	92	—	—	—	—	—	

Note (\*) C<sub>PD</sub> is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit).

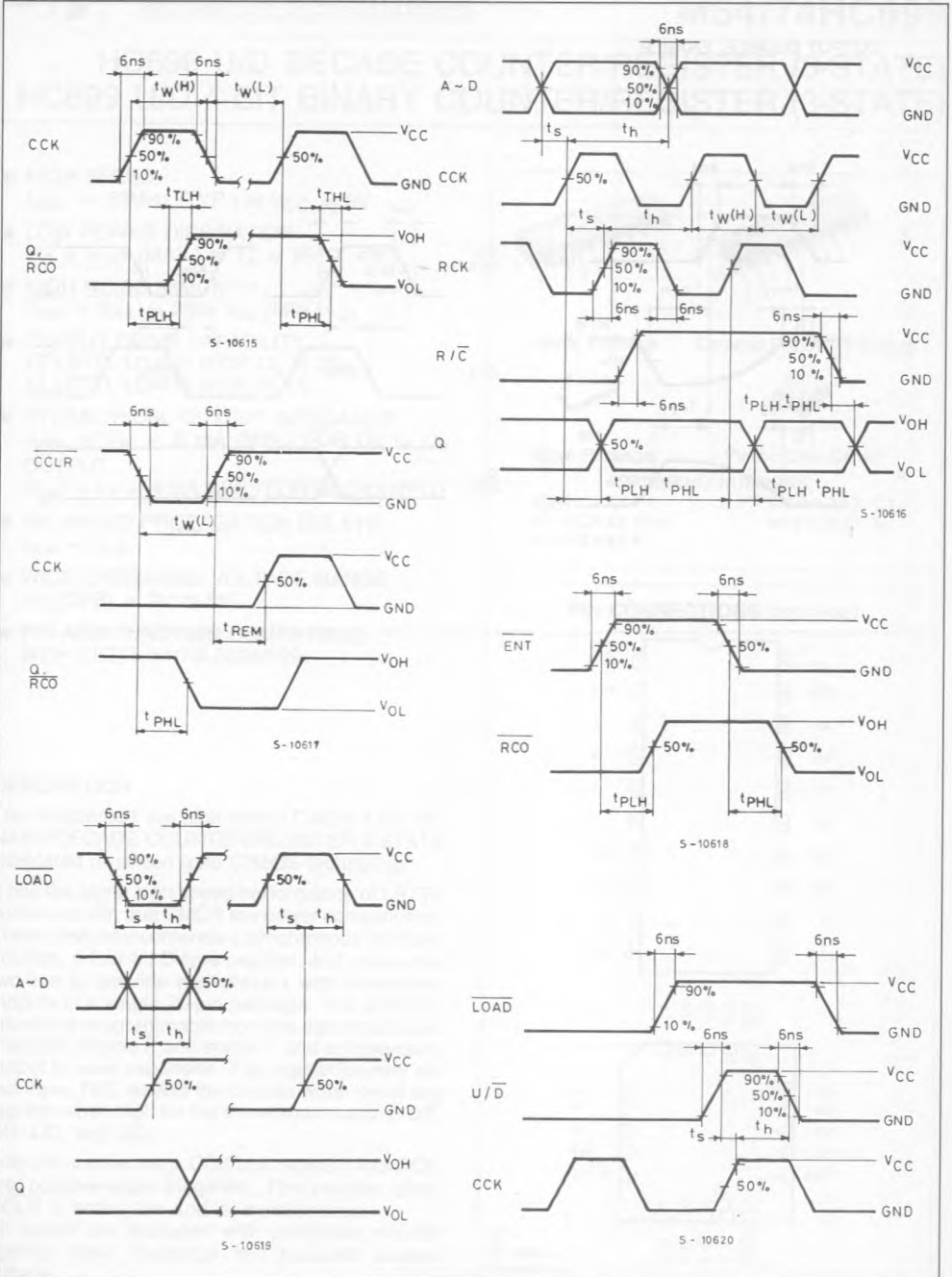
Average operating current can be obtained from the equation:

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

TEST CIRCUIT I<sub>CC</sub> (Opr.)



SWITCHING CHARACTERISTICS TEST WAVEFORM



SWITCHING CHARACTERISTICS TEST WAVEFORM (Continued)

OUTPUT DISABLE, ENABLE

