SGS-THOMSON MICROELECTRONICS

M54/74HC696
M54/74HC697

HC696 U/D DECADE COUNTER/REGISTER (3-STATE)
HC697 U/D 4-BIT BINARY COUNTER/REGISTER (3-STATE)

- HIGH SPEED
  f_{MAX} = 33MHz (TYP.) at V_{CC} = 5V
- LOW POWER DISSIPATION
  I_{CC} = 4 μA (MAX.) at T_A = 25°C
- HIGH NOISE IMMUNITY
  V_{NIH} = V_{NIL} = 28% V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  15 LSTTL LOADS (FOR Q_A to Q_D)
  10 LSTTL LOADS (FOR RCO)
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}|$ = I_{OL} = 6 mA (MIN.) FOR Q_A to Q_D
  $|I_{OH}|$ = I_{OL} = 4 mA (MIN.) FOR RCO OUTPUT
- BALANCED PROPAGATION DELAYS
  t_{PLH} = t_{PHL}
- WIDE OPERATING VOLTAGE RANGE
  V_{CC}(OPR) = 2V to 6V
- PIN AND FUNCTION COMPATIBLE
  WITH LSTTL 54/74LS696/697

B1N
Plastic Package

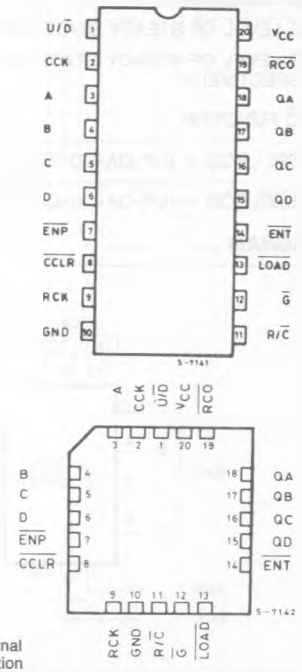
F1
Ceramic Frit Seal Package

M1
Micro Package

C1
Plastic Chip Carrier

ORDERING NUMBERS:
M54HCXXX F1
M74HCXXX B1N
M74HCXXX F1
M74HCXXX C1
M74HCXXX M1

PIN CONNECTIONS (top view)



NC =
No Internal
Connection

DESCRIPTION

The HC696/697 are high speed CMOS up/down counters fabricated with silicon gate C²MOS technology. They achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation. The HC696 is a BCD DECADE COUNTER, and the HC697 is 4-BIT BINARY COUNTER. Both devices have register. They count on the positive edge of the counter clock input (CCK) when selected by the "Counter Mode". If the input U/D is held "H", the internal counter counts up, and held "L", counts down. The internal counter's outputs are stored in the output register at the positive edge of register clock (RCK). The outputs (QA - QD) are internal counter outputs or register outputs respectively and are selected by R/C. The clear function are cleared asynchronously to the clock. All inputs are equipped with protection circuits against static discharge and transient excess voltage.

TRUTH TABLE

INPUTS									OUTPUTS				FUNCTION
$\overline{CCLR}$	$\overline{LOAD}$	$\overline{ENP}$	$\overline{ENT}$	CCK	U/$\overline{D}$	RCK	R/$\overline{C}$	$\overline{G}$	QA	QB	QC	QD	
X	X	X	X	X	X	X	X	H	Z	Z	Z	Z	HIGH IMPEDANCE
L	X	X	X	X	X	X	L	L	L	L	L	L	CLEAR COUNTER
H	L	X	X	↑	X	X	L	L	a	b	c	d	LOAD COUNTER
H	H	H	X	↑	X	X	L	L	NO CHANGE				NO COUNT
H	H	X	H	↑	X	X	L	L	NO CHANGE				NO COUNT
H	H	L	L	↑	H	X	L	L	COUNT UP				COUNT UP
H	H	L	L	↑	L	X	L	L	COUNT DOWN				COUNT DOWN
H	X	X	X	↓	X	X	L	L	NO CHANGE				NO COUNT
X	X	X	X	X	X	↑	H	L	a'	b'	c'	d'	LOAD REGISTER
X	X	X	X	X	X	↓	H	L	NO CHANGE				NO LOAD

X : DON'T CARE

Z : HIGH IMPEDANCE

a-d : THE LEVEL OF STEADY STATE INPUT AT INPUTS A THROUGH D RESPECTIVELY.

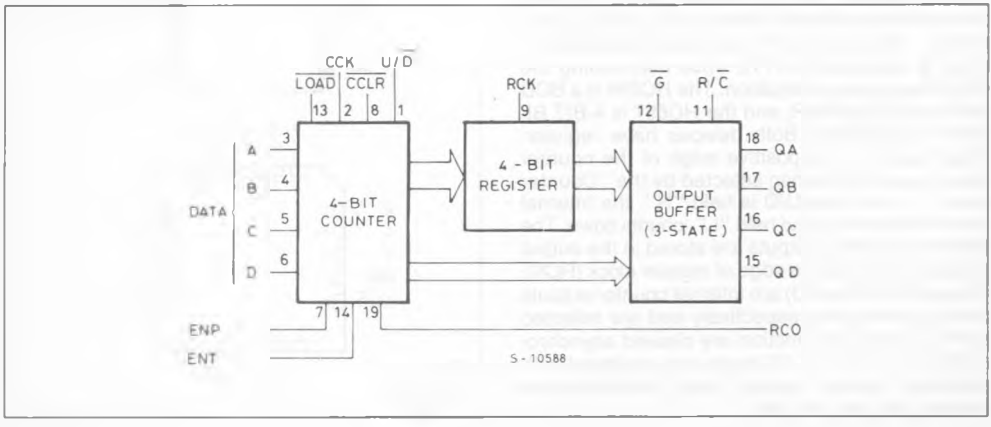
a'-d' : THE LEVEL OF STEADY STATE OUTPUTS AT INTERNAL COUNTER OUTPUTS QA' THROUGH QD' RESPECTIVELY.

$\overline{RCO}$ FUNCTION

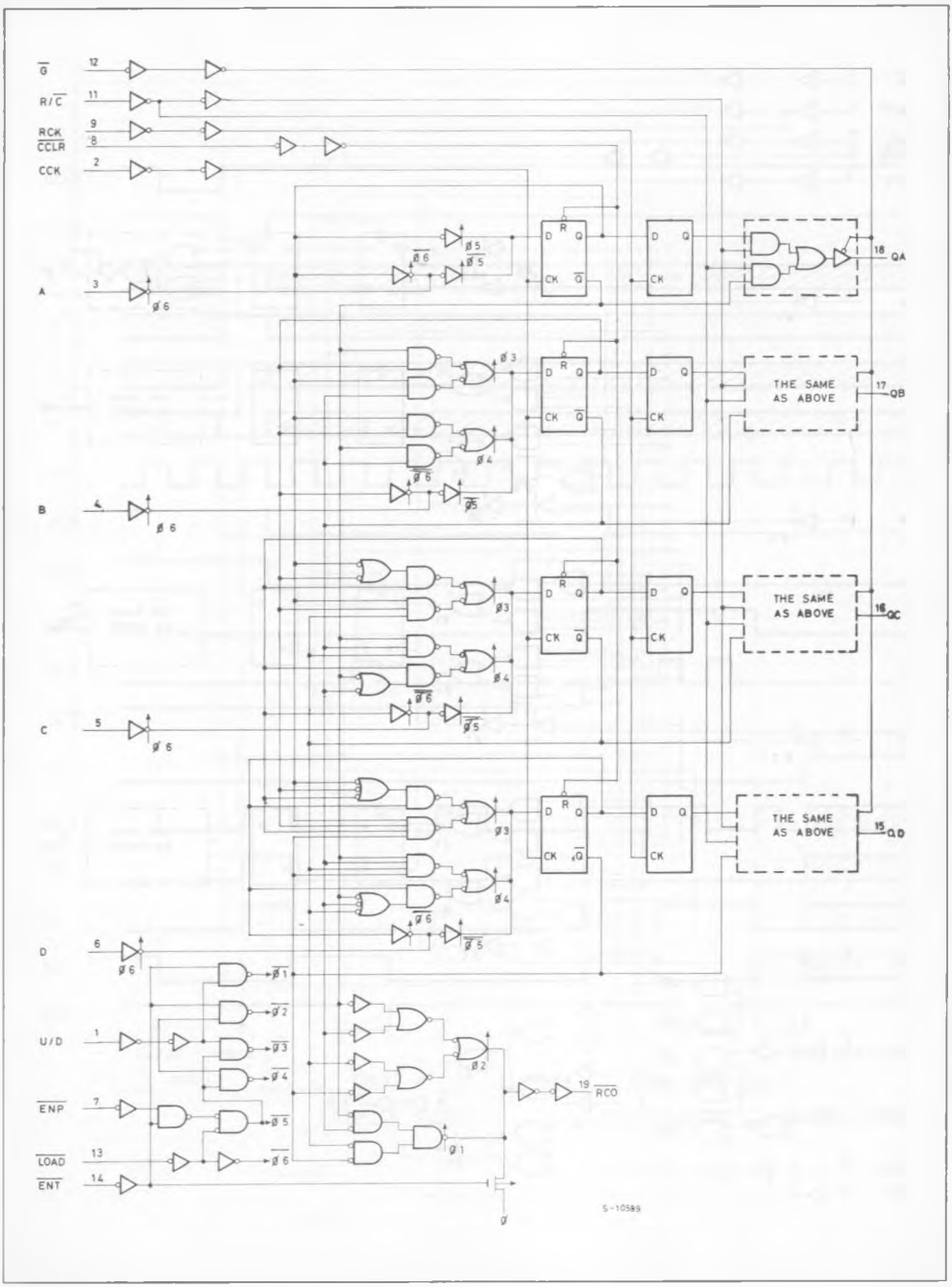
HC696 - $\overline{RCO} = \overline{(UP \cdot QA \cdot QD \cdot ENT + \overline{UP} \cdot \overline{QA} \cdot \overline{QB} \cdot \overline{QC} \cdot \overline{QD} \cdot ENT)}$

HC697 - $\overline{RCO} = \overline{(UP \cdot QA \cdot QB \cdot QC \cdot QD \cdot ENT + \overline{UP} \cdot \overline{QA} \cdot \overline{QB} \cdot \overline{QC} \cdot \overline{QD} \cdot ENT)}$

BLOCK DIAGRAM



LOGIC DIAGRAM (HC696)



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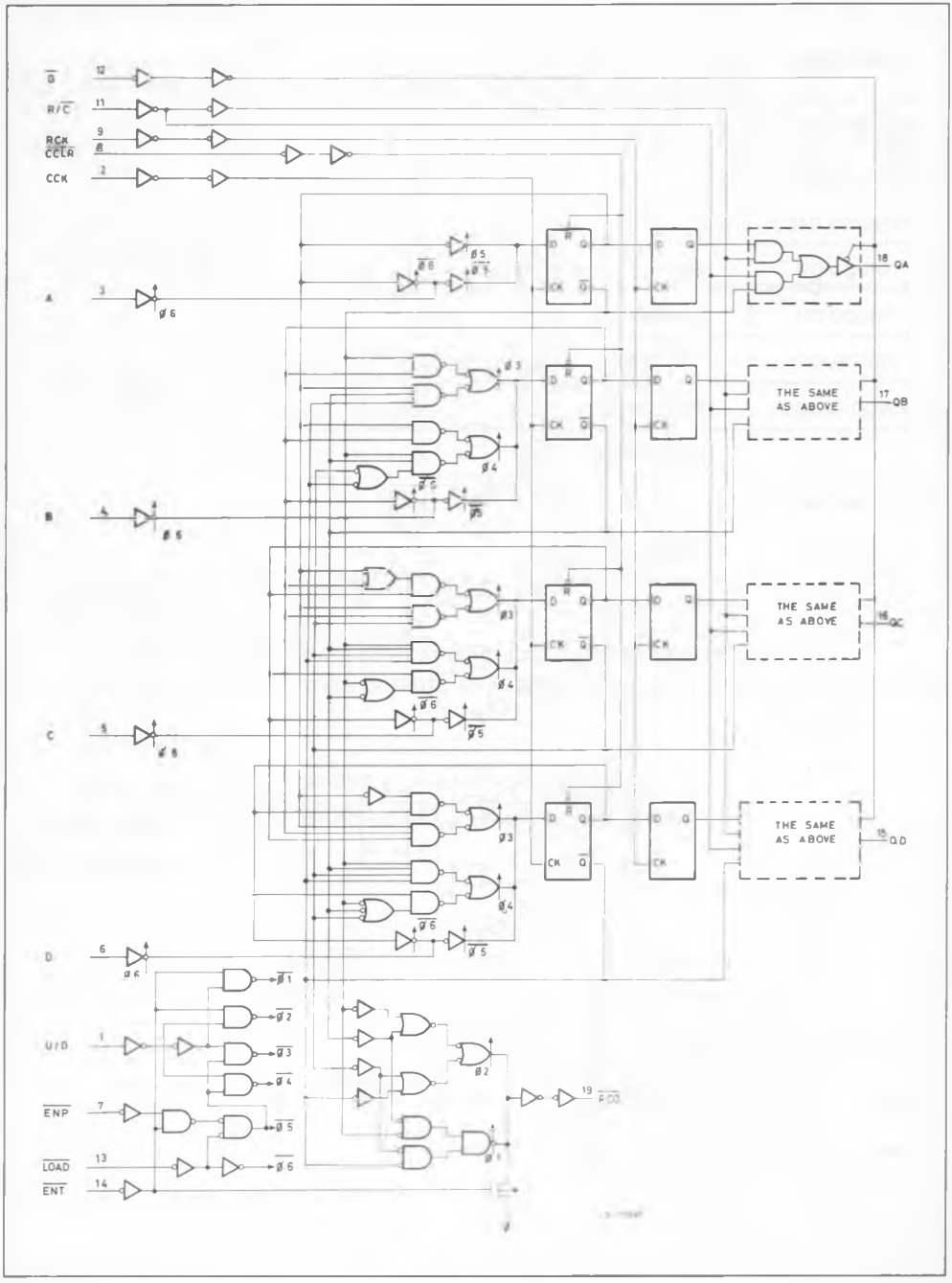
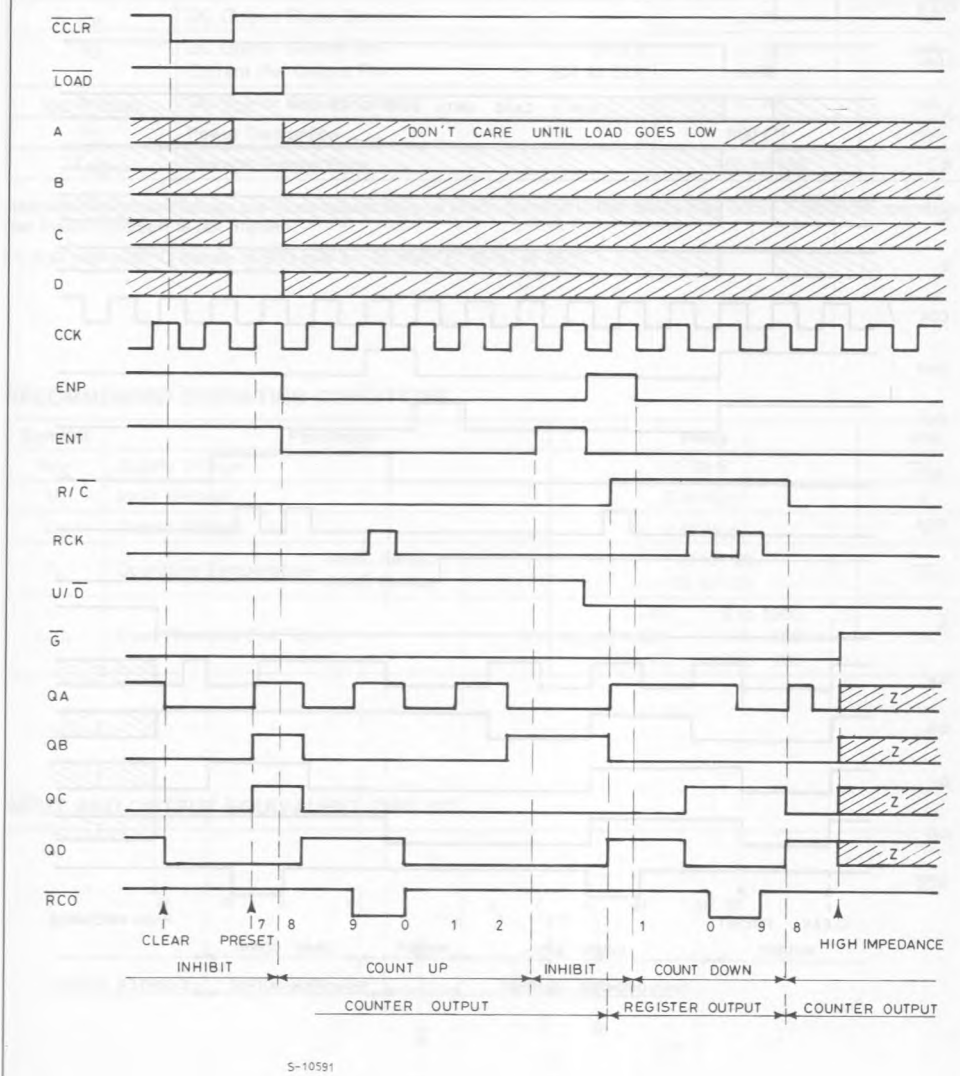
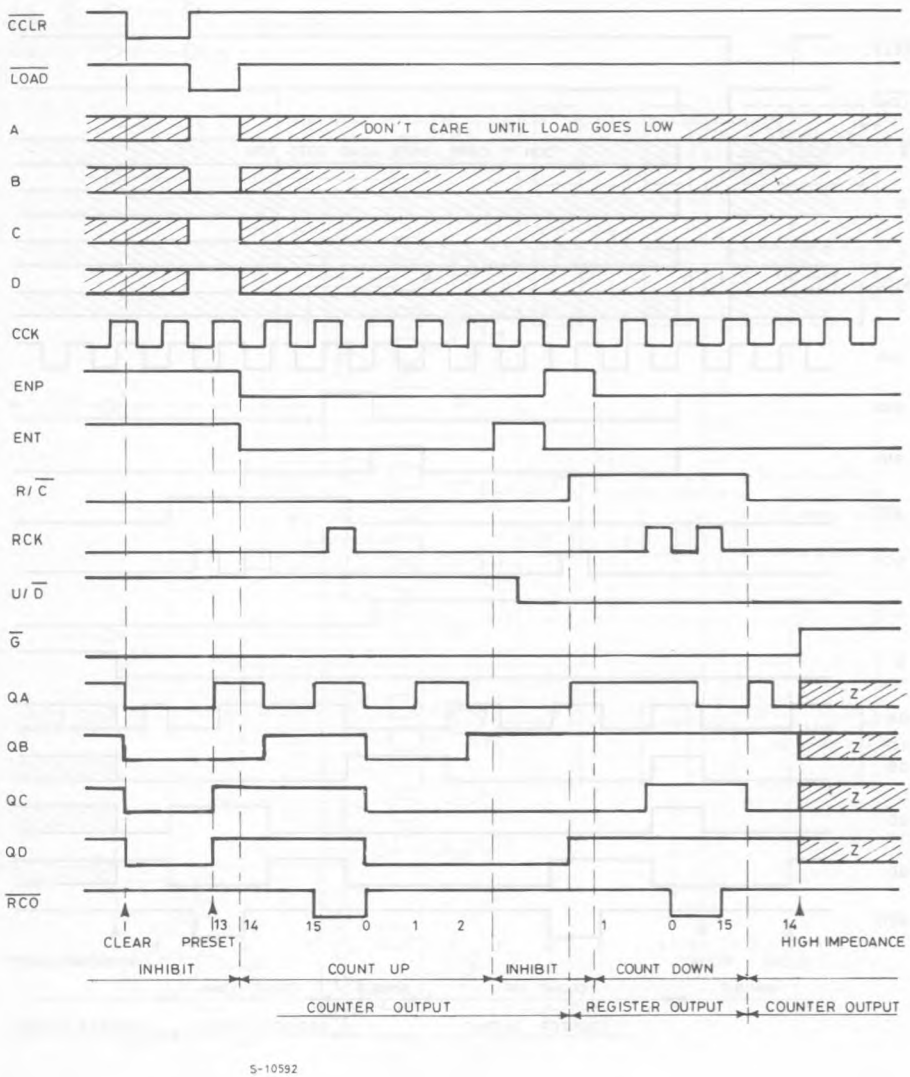


TIMING CHART (HC696)



TIMING CHART (HC697)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		−0.5 to 7	V
V_I	DC Input Voltage		−0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage		−0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current		± 20	mA
I_{OK}	DC Output Diode Current		± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	(RCO) (QA to QD)	± 20 ±35	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current		± 70	mA
P_D	Power Dissipation		500 (*)	mW
T_{stg}	Storage Temperature		−65 to 150	°C

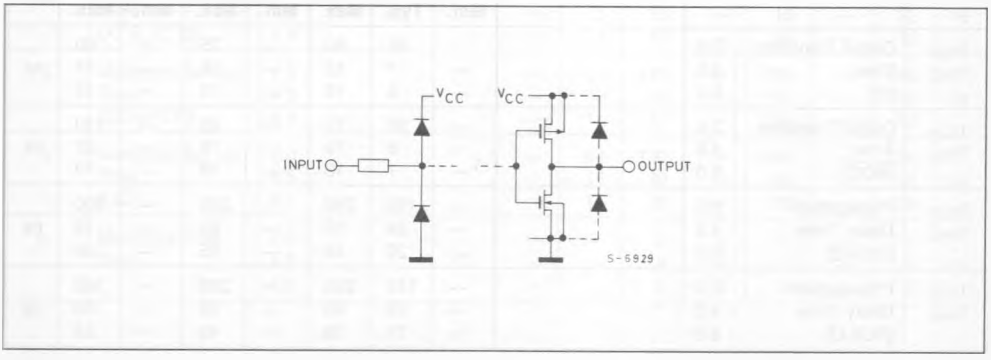
Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: ≅65°C derate to 300 mW by 10 mW/°C: 65°C to 85°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value		Unit
V_{CC}	Supply Voltage		2 to 6		V
V_I	Input Voltage		0 to V_{CC}		V
V_O	Output Voltage		0 to V_{CC}		V
T_A	Operating Temperature	74HC Series 54HC Series	− 40 to 85 −55 to 125		°C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V V_{CC} = 4.5 V V_{CC} = 6 V	0 to 1000 0 to 500 0 to 400		ns

INPUT AND OUTPUT EQUIVALENT CIRCUIT



DC SPECIFICATIONS

Symbol	Parameter	V_{CC}	Test Condition		$T_A = 25°C$ 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
					Min	Typ	Max	Min	Max	Min	Max	
V_{IH}	High Level Input Voltage	2.0 4.5 6.0			1.5 3.15 4.2	— — —	— — —	1.5 3.15 4.2	— — —	1.5 3.15 4.2	— — —	V
V_{IL}	Low Level Input Voltage	2.0 4.5 6.0			— — —	— — —	0.5 1.35 1.8	— — —	0.5 1.35 1.8	— — —	0.5 1.35 1.8	V
V_{OH}	High Level Output Voltage	2.0	V_{IN}	I_{OH}	1.9	2.0	—	1.9	—	1.9	—	V
		4.5 6.0	V_{IH} or V_{IL}	−20 μA	4.4 5.9	4.5 6.0	— —	4.4 5.9	— —	4.4 5.9	— —	
		4.5 6.0	Q_A-Q_H	−6.0 mA −7.8 mA	4.18 5.68	4.31 5.8	— —	4.13 5.63	— —	4.10 5.60	— —	
		4.5 6.0	RCO	−4.0 mA −5.2 mA	4.18 5.68	4.31 5.8	— —	4.13 5.63	— —	4.10 5.60	— —	
V_{OL}	Low Level Output Voltage	2.0	V_{IN}	I_{OL}	—	0	0.1	—	0.1	—	0.1	V
		4.5 6.0	V_{IH} or V_{IL}	20 μA	— —	0 0	0.1 0.1	— —	0.1 0.1	— —	0.1 0.1	
		4.5 6.0	Q_A-Q_H	6.0 mA 7.8 mA	— —	0.17 0.18	0.26 0.26	— —	0.33 0.33	— —	0.40 0.40	
		4.5 6.0	RCO	4.0 mA 5.2 mA	— —	0.17 0.18	0.26 0.26	— —	0.33 0.33	— —	0.40 0.40	
I_{OZ}	3-State Off Leak Current	6.0	$V_{IN} = V_{IL}$ or V_{IH} $V_{OUT} = V_{CC}$ or GND		—	—	±0.5	—	±5.0	—	±10	μA
I_{IN}	Input Leakage Current	6.0	$V_{IN} = V_{CC}$ or GND		—	—	±0.1	—	±1.0	—	±1.0	
I_{CC}	Quiescent Supply Current	6.0	$V_{IN} = V_{CC}$ or GND		—	—	4.0	—	40.0	—	80.0	

AC ELECTRICAL CHARACTERISTICS ($C_L = 50pF$, Input $t_r = t_f = 6ns$)

Symbol	Parameter	V_{CC}	Test Condition	$T_A = 25°C$ 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time (Q)	2.0 4.5 6.0		— — —	25 7 6	60 12 10	— — —	75 15 13	— — —	90 18 15	ns
t_{TLH} t_{THL}	Output Transition Time ($\overline{RCO}$)	2.0 4.5 6.0		— — —	30 8 7	75 15 13	— — —	95 19 16	— — —	110 22 19	ns
t_{PLH} t_{PHL}	Propagation Delay Time (CCK-Q)	2.0 4.5 6.0		— — —	136 34 29	260 52 44	— — —	325 65 55	— — —	390 78 66	ns
t_{PLH} t_{PHL}	Propagation Delay Time (RCK-Q)	2.0 4.5 6.0		— — —	116 29 25	225 45 38	— — —	280 56 48	— — —	340 68 58	ns

AC ELECTRICAL CHARACTERISTICS (Continued)

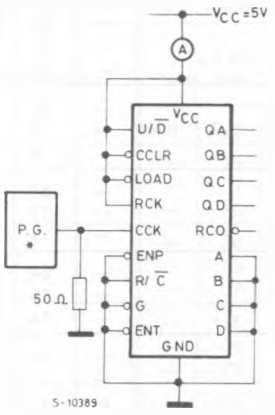
Symbol	Parameter	V_{CC}	Test Condition	$T_A = 25°C$ 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{PLH} t_{PHL}	Propagation Delay Time (CCK-$\overline{RCO}$)	2.0		—	160	305	—	385	—	460	ns
		4.5		—	40	61	—	77	—	92	
		6.0		—	34	52	—	66	—	78	
t_{PLH} t_{PHL}	Propagation Delay Time (R/$\overline{C}$-Q)	2.0		—	100	195	—	245	—	295	ns
		4.5		—	25	39	—	49	—	59	
		6.0		—	21	33	—	42	—	50	
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{ENT}$-$\overline{RCO}$)	2.0		—	116	225	—	280	—	340	ns
		4.5		—	29	45	—	56	—	68	
		6.0		—	25	38	—	48	—	58	
t_{PHL}	Propagation Delay Time ($\overline{CCLR}$-Q)	2.0		—	148	285	—	355	—	430	ns
		4.5		—	37	57	—	71	—	86	
		6.0		—	31	48	—	60	—	73	
t_{PHL}	Propagation Delay Time ($\overline{CCLR}$-$\overline{RCO}$)	2.0		—	172	325	—	405	—	490	ns
		4.5		—	43	65	—	81	—	98	
		6.0		—	37	55	—	69	—	83	
f_{MAX}	Maximum Clock Frequency	2.0		4	8	—	3	—	3	—	MHz
		4.5		20	30	—	16	—	13	—	
		6.0		24	35	—	19	—	15	—	
$t_{W(H)}$ $t_{W(L)}$	Minimum Pulse Width (CCK, RCK)	2.0		—	30	75	—	95	—	110	ns
		4.5		—	8	15	—	19	—	22	
		6.0		—	7	13	—	16	—	19	
$t_{W(L)}$	Mimum Pulse Width ($\overline{CCLR}$)	2.0		—	30	75	—	95	—	110	ns
		4.5		—	8	15	—	19	—	22	
		6.0		—	7	13	—	16	—	19	
t_{REM}	Minimum Removal Time ($\overline{CCLR}$)	2.0		—	—	5	—	5	—	5	ns
		4.5		—	—	5	—	5	—	5	
		6.0		—	—	5	—	5	—	5	
t_s	Minimum Set-up Time ($\overline{LOAD}$,$\overline{ENT}$,$\overline{ENP}$)	2.0		—	96	225	—	280	—	340	ns
		4.5		—	24	45	—	56	—	68	
		6.0		—	20	38	—	48	—	58	
t_s	Minimum Set-up Time (A, B, C, D)	2.0		—	20	75	—	95	—	110	ns
		4.5		—	5	15	—	19	—	22	
		6.0		—	4	13	—	16	—	19	
t_s	Minimum Set-up Time (CCK-RCK)	2.0		—	52	125	—	155	—	190	ns
		4.5		—	13	25	—	31	—	38	
		6.0		—	11	21	—	26	—	32	
t_s	Minimum Set-up Time (U/$\overline{D}$)	2.0		—	64	150	—	190	—	225	ns
		4.5		—	16	30	—	38	—	45	
		6.0		—	14	26	—	33	—	38	
t_h	Minimum Hold Time	2.0		—	—	0	—	0	—	0	ns
		4.5		—	—	0	—	0	—	0	
		6.0		—	—	0	—	0	—	0	

AC ELECTRICAL CHARACTERISTICS (Continued)

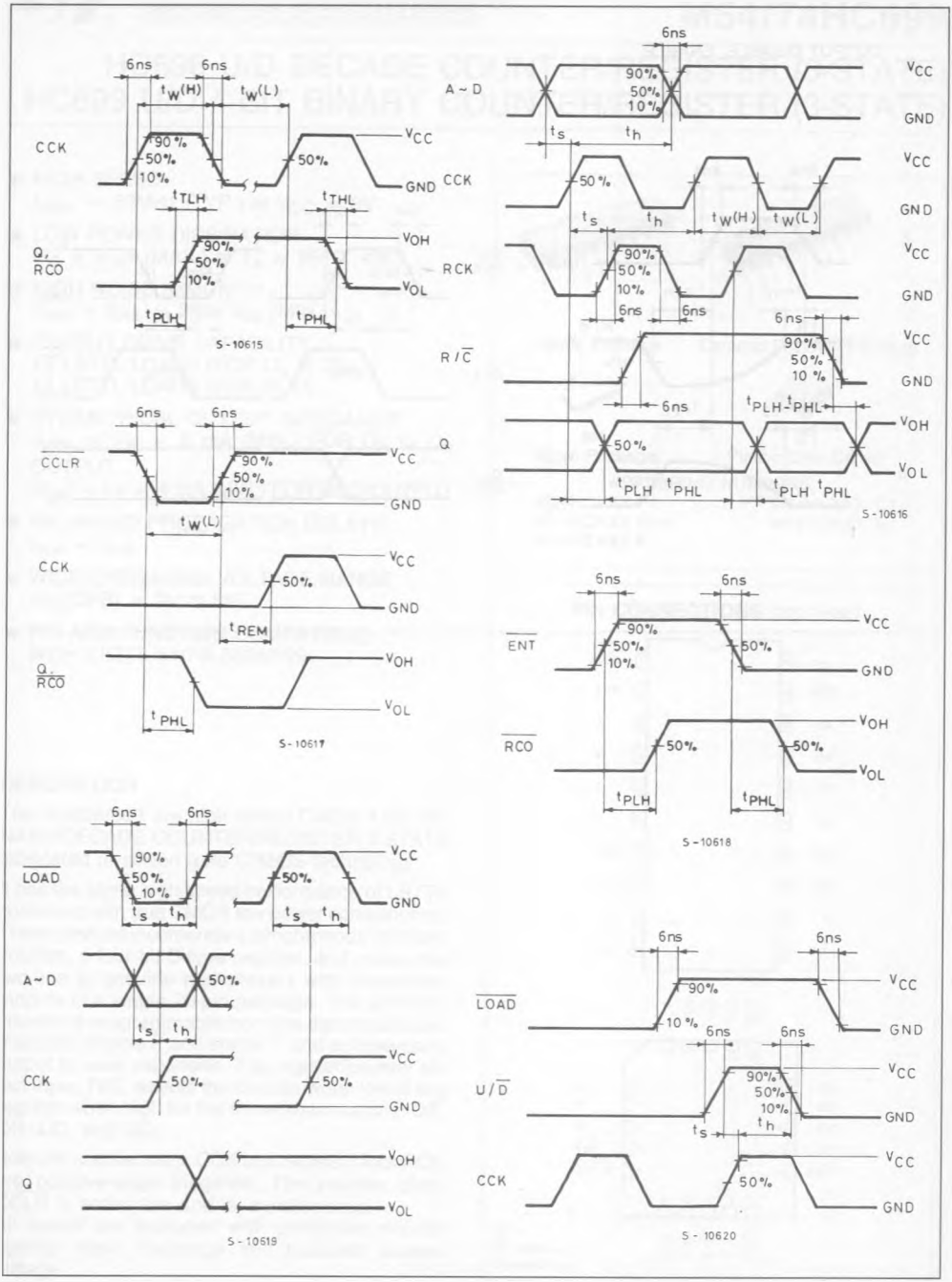
Symbol	Parameter	V_{CC}	Test Condition	T_A = 25°C 54HC and 74HC			– 40 to 85°C 74HC		– 55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{PZL} t_{PZH}	3-State Output Enable Time	2.0	R_L = 1kΩ	—	64	130	—	165	—	195	ns
		4.5		—	16	26	—	33	—	39	
		6.0		—	14	22	—	28	—	33	
t_{PLZ} t_{PHZ}	3-State Output Disable Time	2.0	R_L = 1kΩ	—	92	185	—	230	—	280	ns
		4.5		—	23	37	—	46	—	56	
		6.0		—	20	31	—	39	—	48	
C_{IN}	Input Capacitance			—	5	10	—	10	—	10	pF
C_{PD} (*)	Power Dissipation Capacitance		HC696	—	90	—	—	—	—	—	pF
			HC697	—	92	—	—	—	—	—	

Note (*) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit).
Average operating current can be obtained from the equation:
$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$

TEST CIRCUIT I_{CC} (Opr.)

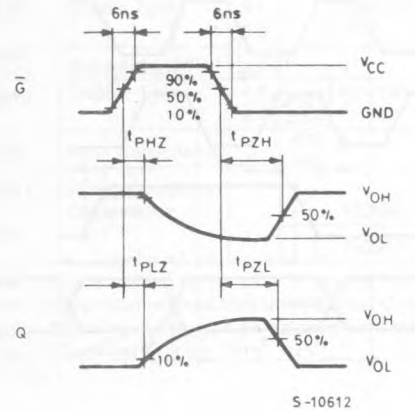


SWITCHING CHARACTERISTICS TEST WAVEFORM

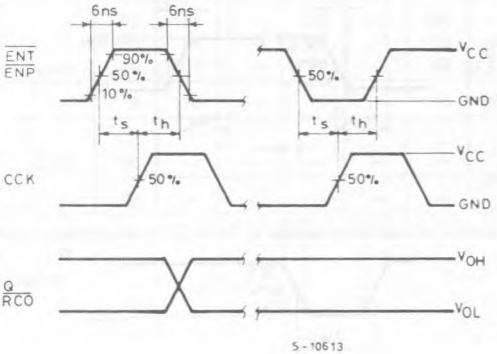


SWITCHING CHARACTERISTICS TEST WAVEFORM (Continued)

OUTPUT DISABLE, ENABLE



S-10612



S-10613