

PROGRAMMABLE DIVIDER/TIMER

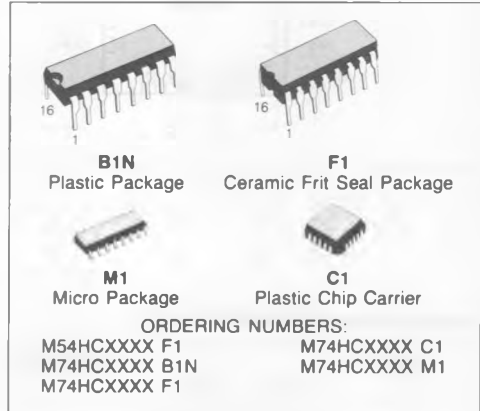
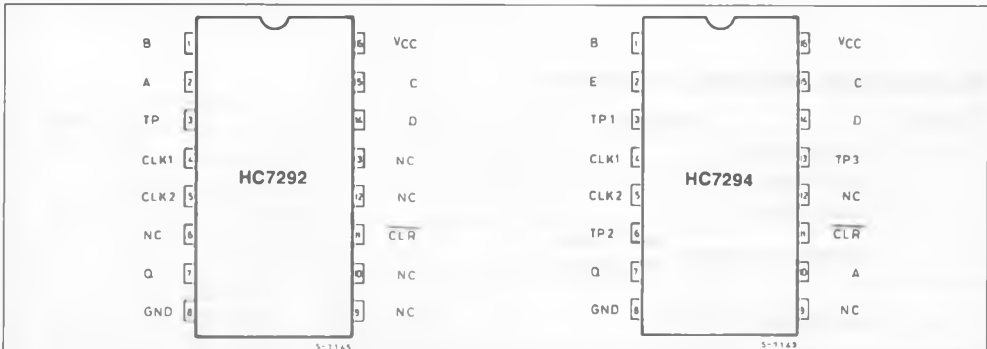
- LOW POWER DISSIPATION
 $I_{CC} = 4 \mu A$ (MAX.) at $T_A = 25^\circ C$
- HIGH NOISE IMMUNITY
 $V_{NIH} = V_{NIL} = 28\% V_{CC}$ (MIN.)
- OUTPUT DRIVE CAPABILITY
 10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
 $|I_{OH}| = |I_{OL}| = 4 \text{ mA}$ (MIN.)
- BALANCED PROPAGATION DELAYS
 $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
 V_{CC} (OPR) = 2V to 6V
- PIN AND FUNCTION COMPATIBLE
 WITH 54/74LS292/294

DESCRIPTION

The 54/74HC7292 and 54/74HC7294 are high speed CMOS PROGRAMMABLE DIVIDER/TIMER fabricated with silicon C²MOS technology. They achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

These devices are programmable frequency divider. Both types have two clock inputs, either one may be used for clock gating. (See the function table). The HC7292 can divide from 2^2 to 2^{31} , and the HC7294 can divide from 2^2 to 2^{15} . Both types feature an active-low clear input to initialize the state of all flip-flops. To facilitate incoming inspection, test points are provided. (TP1, TP2 and TP3 on the HC7292 and TP on the HC7294). All inputs are equipped with protection circuits against static discharge and transient excess voltage.

PIN CONNECTION (top view)

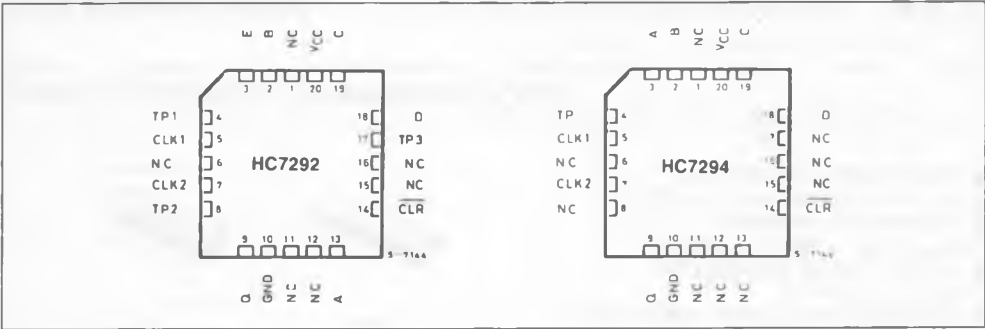


Note: HC7292 and HC7294 all have outputs "Totem pole"

TRUTH TABLE

CLEAR	CLOCK1	CLOCK2	Q OUTPUT MODE
L	X	X	CLEARED TO L
H		L	UP COUNT
H	L		
H	H	X	NO CHANGE
H	X	H	

CHIP CARRIER



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{CC}	Supply Voltage	− 0.5 to 7	V
V _I	DC Input Voltage	− 0.5 to V _{CC} + 0.5	V
V _O	DC Output Voltage	− 0.5 to V _{CC} + 0.5	V
I _{IK}	DC Input Diode Current	± 20	mA
I _{OK}	DC Output Diode Current	± 20	mA
I _O	DC Output Source Sink Current Per Output Pin	± 25	mA
I _{CC} or I _{GND}	DC V _{CC} or Ground Current	± 50	mA
P _D	Power Dissipation	500 (*)	mW
T _{stg}	Storage Temperature	− 65 to 150	°C

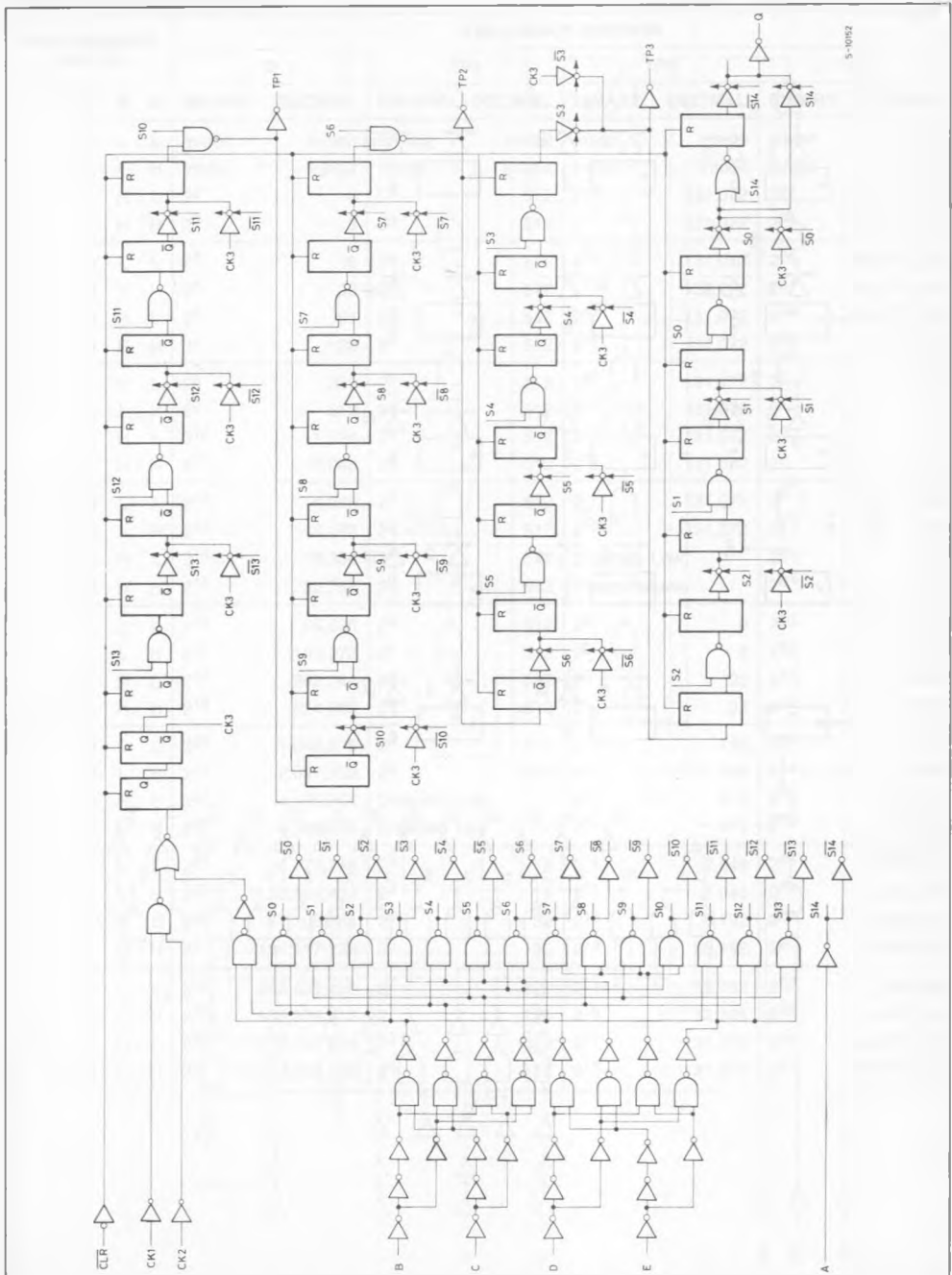
Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: ≅ 65°C derate to 300 mW by 10 mW/°C: 65°C to 85°C

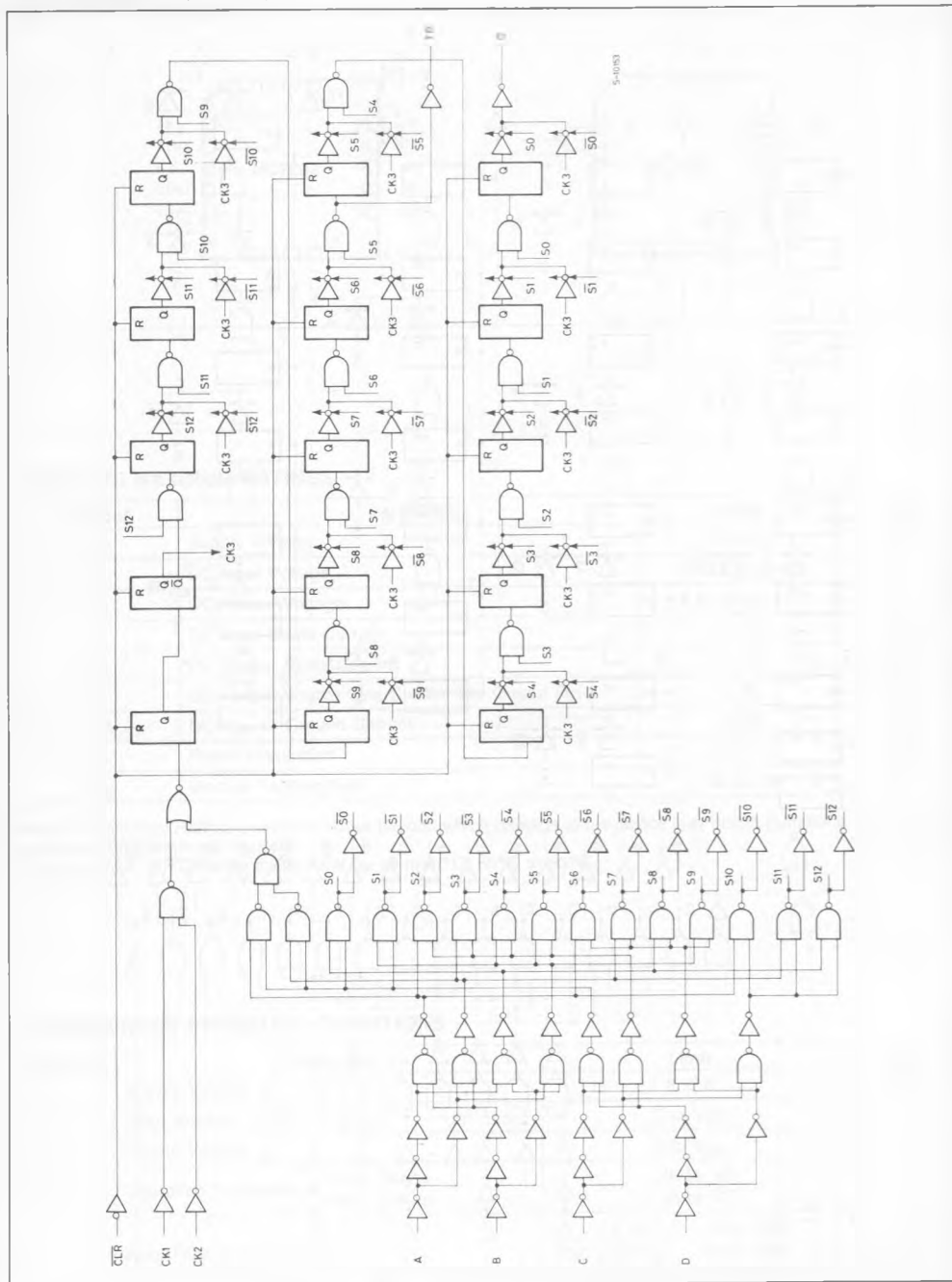
RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Limit	Unit
V _{CC}	Supply Voltage	2 to 6	V
V _I	Input Voltage	0 to V _{CC}	V
V _O	Output Voltage	0 to V _{CC}	V
T _A	Operating Temperature	74HC Series 54HC Series	°C
t _r , t _f	Input Rise and Fall Time	V _{CC} { 2 V 4.5V 6 V	ns

LOGIC DIAGRAM (HC7292)



LOGIC DIAGRAM (HC7294)



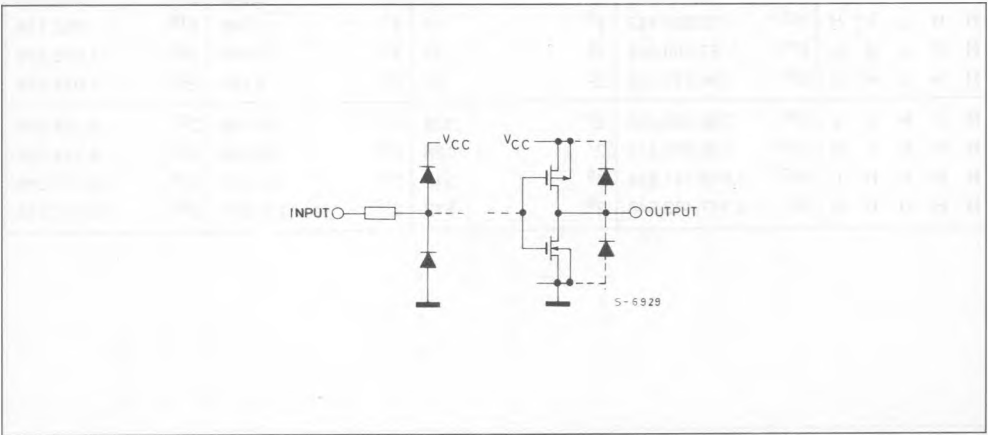
FUNCTION TABLE (HC7292)

PROGRAMMING INPUTS					FREQUENCY DIVISION							
					Q		TP1		TP2		TP3	
E	D	C	B	A	BINARY	DECIMAL	BINARY	DECIMAL	BINARY	DECIMAL	BINARY	DECIMAL
L	L	L	L	L	Inhibit	Inhibit	Inhibit	Inhibit	Inhibit	Inhibit	Inhibit	Inhibit
L	L	L	L	H	Inhibit	Inhibit	Inhibit	Inhibit	Inhibit	Inhibit	Inhibit	Inhibit
L	L	L	H	L	2 ²	4	2 ⁹	512	2 ¹⁷	131,072	2 ²⁴	16,777,216
L	L	L	H	H	2 ³	8	2 ⁹	512	2 ¹⁷	131,072	2 ²⁴	16,777,216
L	L	H	L	L	2 ⁴	16	2 ⁹	512	2 ¹⁷	131,072	2 ²⁴	16,777,216
L	L	H	L	H	2 ⁵	32	2 ⁹	512	2 ¹⁷	131,072	2 ²⁴	16,777,216
L	L	H	H	L	2 ⁶	64	2 ⁹	512	2 ¹⁷	131,072	2 ²⁴	16,777,216
L	L	H	H	H	2 ⁷	128	2 ⁹	512	2 ¹⁷	131,072	2 ²⁴	16,777,216
L	H	L	L	L	2 ⁸	256	2 ⁹	512	2 ¹⁷	131,072	2 ²	4
L	H	L	L	H	2 ⁹	512	2 ⁹	512	2 ¹⁷	131,072	2 ²	4
L	H	L	H	L	2 ¹⁰	1,024	2 ⁹	512	2 ¹⁷	131,072	2 ⁴	16
L	H	L	H	H	2 ¹¹	2,048	2 ⁹	512	2 ¹⁷	131,072	2 ²	16
L	H	H	L	L	2 ¹²	4,096	2 ⁹	512	2 ¹⁷	131,072	2 ⁶	64
L	H	H	L	H	2 ¹³	8,192	2 ⁹	512	2 ¹⁷	131,072	2 ⁶	64
L	H	H	H	L	2 ¹⁴	16,384	2 ⁹	512	Disabled Low		2 ⁸	256
L	H	H	H	H	2 ¹⁵	32,768	2 ⁹	512	Disabled Low		2 ⁸	256
H	L	L	L	L	2 ¹⁶	65,536	2 ⁹	512	2 ³	8	2 ¹⁰	1,024
H	L	L	L	H	2 ¹⁷	131,072	2 ⁹	512	2 ³	8	2 ¹⁰	1,024
H	L	L	H	L	2 ¹⁸	262,144	2 ⁹	512	2 ⁵	32	2 ¹²	4,096
H	L	L	H	H	2 ¹⁹	524,288	2 ⁹	512	2 ⁵	32	2 ¹²	4,096
H	L	H	L	L	2 ²⁰	1,048,576	2 ⁹	512	2 ⁷	128	2 ¹⁴	16,384
H	L	H	L	H	2 ²¹	2,097,152	2 ⁹	512	2 ⁷	128	2 ¹⁴	16,384
H	L	H	H	L	2 ²²	4,194,304	Disabled Low		2 ⁹	512	2 ¹⁶	65,536
H	L	H	H	H	2 ²³	8,388,608	Disabled Low		2 ⁹	512	2 ¹⁶	65,536
H	H	L	L	L	2 ²⁴	16,777,216	2 ³	8	2 ¹¹	2,048	2 ¹⁸	262,144
H	H	L	L	H	2 ²⁵	33,554,432	2 ³	8	2 ¹¹	2,048	2 ¹⁸	262,144
H	H	L	H	L	2 ²⁶	67,108,864	2 ⁵	32	2 ¹³	8,192	2 ²⁰	1,048,576
H	H	L	H	H	2 ²⁷	134,217,728	2 ⁵	32	2 ¹³	8,192	2 ²⁰	1,048,576
H	H	H	L	L	2 ²⁸	268,435,456	2 ⁷	128	2 ¹⁵	32,768	2 ²²	4,194,304
H	H	H	L	H	2 ²⁹	536,870,912	2 ⁷	128	2 ¹⁵	32,768	2 ²²	4,194,304
H	H	H	H	L	2 ³⁰	1,073,741,824	2 ⁹	512	2 ¹⁷	131,072	2 ²⁴	16,777,216
H	H	H	H	H	2 ³¹	2,147,483,648	2 ⁹	512	2 ¹⁷	131,072	2 ²⁴	16,777,216

FUNCTION TABLE (HC7294)

PROGRAMMING INPUTS				FREQUENCY DIVISION			
				Q		TP	
D	C	B	A	BINARY	DECIMAL	BINARY	DECIMAL
L	L	L	L	Inhibit	Inhibit	Inhibit	Inhibit
L	L	L	H	Inhibit	Inhibit	Inhibit	Inhibit
L	L	H	L	2 ²	4	2 ⁹	512
L	L	H	H	2 ³	8	2 ⁹	512
L	H	L	L	2 ⁴	16	2 ⁹	512
L	H	L	H	2 ⁵	32	2 ⁹	512
L	H	H	L	2 ⁶	64	2 ⁹	512
L	H	H	H	2 ⁷	128	Disabled Low	
H	L	L	L	2 ⁸	256	2 ²	4
H	L	L	H	2 ⁹	512	2 ³	8
H	L	H	L	2 ¹⁰	1,024	2 ⁴	16
H	L	H	H	2 ¹¹	2,048	2 ⁵	32
H	H	L	L	2 ¹²	4,096	2 ⁶	64
H	H	L	H	2 ¹³	8,192	2 ⁷	128
H	H	H	L	2 ¹⁴	16,384	2 ⁸	256
H	H	H	H	2 ¹⁵	32,768	2 ⁹	512

INPUT AND OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	V _{CC}	Test Condition	T _A = 25°C 54HC and 74HC			- 40 to 85°C 74HC		- 55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V _{IH}	High Level Input Voltage	2.0 4.5 6.0		1.5 3.15 4.2	— — —	— — —	1.5 3.15 4.2	— — —	1.5 3.15 4.2	— — —	V
V _{IL}	Low Level Input Voltage	2.0 4.5 6.0		— — —	— — —	0.5 1.35 1.8	— — —	0.5 1.35 1.8	— — —	0.5 1.35 1.8	V
V _{OH}	High Level Output Voltage	2.0	V _I	I _O	1.9	2.0	—	1.9	—	1.9	V
		4.5	V _{IH}	— 20 µA	4.4	4.5	—	4.4	—	4.4	
		6.0	V _{IH} or V _{IL}	— 20 µA	5.9	6.0	—	5.9	—	5.9	
V _{OL}	Low Level Output Voltage	2.0	V _{IH} or V _{IL}	— 4.0 mA	4.18	4.31	—	4.13	—	4.10	V
		4.5		— 5.2 mA	5.68	5.8	—	5.63	—	5.60	
		6.0		— 5.2 mA	—	—	—	—	—	—	
I _I	Input Leakage Current	6.0	V _I = V _{CC} or GND	—	—	± 0.1	—	± 1.0	—	± 1.0	µA
I _{CC}	Quiescent Supply Current	6.0	V _I = V _{CC} or GND	—	—	4	—	40	—	80	µA

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V, T_A = 25°C, C_L = 15pF, Input t_r = t_f = 6ns)

Symbol	Parameter		54HC and 74HC			Unit
			Min.	Typ.	Max.	
t _{TLH} t _{THL}	Output Transition Time Q OUTPUT			4	8	ns
t _{TLH} t _{THL}	Output Transition Time TP OUTPUTS			29	45	ns
t _{PLH} t _{PHL}	Propagation Delay Time (CK-Q)	HC7292		58	89	ns
		HC7294		53	81	
t _{PHL}	Propagation Delay Time (CLEAR-Q)	HC7292		49	75	ns
		HC7294		45	69	
f _{MAX}	Maximum Clock Frequency	HC7292	28	56		MHz
		HC7294	35	61		

AC ELECTRICAL CHARACTERISTICS ($C_L = 50\text{pF}$, Input $t_r = t_f = 6\text{ns}$)

Symbol	Parameter	V_{CC}	Test Condition	$T_A = 25^\circ\text{C}$ 54HC and 74HC			- 40 to 85°C 74HC		- 55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time Q OUTPUT	2.0 4.5 6.0		— — —	30 8 7	75 15 13	— — —	95 19 16		110 22 19	ns
t_{TLH} t_{THL}	Output Transition Time TP OUTPUT	2.0 4.5 6.0		— — —	132 33 28	255 51 43	— — —	320 64 55		385 77 65	ns
t_{PLH} t_{PHL}	Propagation Delay Time (CK-Q)*	2.0 4.5 6.0	B = "H" A = C = D = E = "L"	— — —	264 66 56	500 100 85	— — —	635 127 110		750 150 127	ns
t_{PLH} t_{PHL}	Propagation Delay Time (CK-Q)**	2.0 4.5 6.0	B = "H" A = C = D = E = "L"	— — —	236 59 50	455 91 77	— — —	571 115 100		676 136 115	ns
t_{PHL}	Propagation Delay Time (CLR-Q)*	2.0 4.5 6.0		— — —	224 56 48	425 85 73	— — —	535 107 92		640 128 109	ns
t_{PHL}	Propagation Delay Time (CLR-Q)**	2.0 4.5 6.0		— — —	204 51 43	390 78 67	— — —	490 98 84		585 117 99	ns
f_{MAX}	Maximum Clock Frequency*	2.0 4.5 6.0		5 25 29	13 51 60	— — —	4 20 24	— — —	3.4 17 20	— — —	MHz
f_{MAX}	Maximum Clock Frequency**	2.0 4.5 6.0		6 32 38	14 55 65	— — —	5 26 31	— — —	4.2 21 25	— — —	MHz
$t_{W(H)}$ $t_{W(L)}$	Minimum Pulse Width CK)	2.0 4.5 6.0		— — —	36 9 8	100 20 17	— — —	125 25 21		150 30 26	ns
$t_{W(L)}$	Minimum Pulse Width CLEAR*	2.0 4.5 6.0		— — —	60 15 13	150 30 26	— — —	190 38 33		225 45 38	ns
$t_{W(L)}$	Minimum Pulse Width CLEAR**	2.0 4.5 6.0		— — —	72 18 15	175 35 30	— — —	220 44 37		265 53 45	ns
t_{REM}	Minimum Removal Time CLEAR	2.0 4.5 6.0		— — —	— — —	25 5 5	— — —	30 6 6	— — —	40 8 7	ns
C_{IN}	Input Capacitance			—	5	10	—	10		10	pF
C_{PD} (*)	Power Dissipation Capacitance		M54/74HC7292	—	22	—	—	—			pF
			M54/74HC7294	—	23	—	—	—			

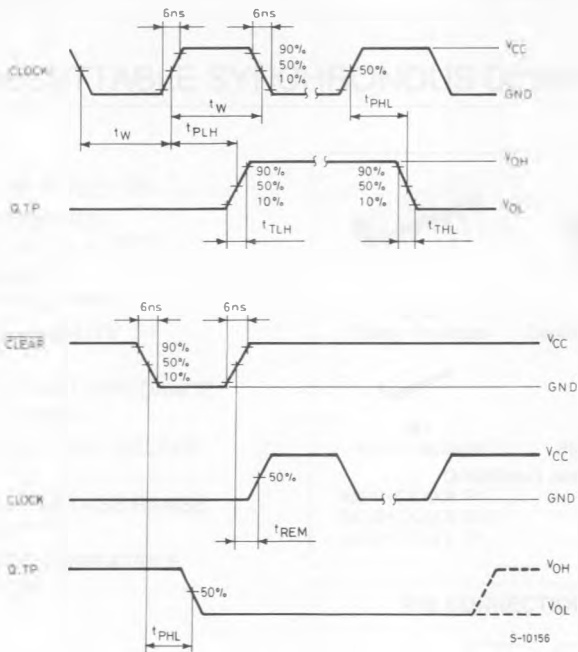
Note (*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the following equation: $I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$

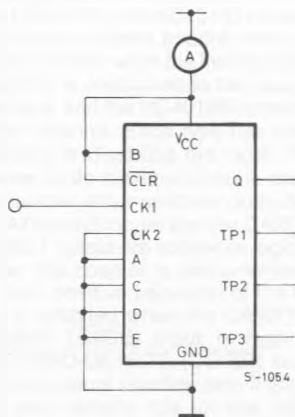
* M54/74HC7292

** M54/74HC7294

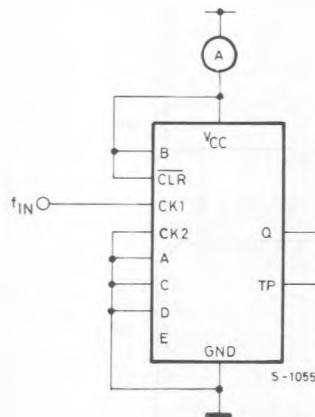
SWITCHING CHARACTERISTICS TEST WAVEFORM

TEST CIRCUIT I_{CC} (Opr.)

HC792



HC794



INPUT TRANSITION TIME IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST