SGS-THOMSON MICROELECTRONICS

# M54HC73
# M74HC73

## DUAL J-K FLIP FLOP WITH CLEAR

- HIGH SPEED
  $f_{MAX}$ = 60 MHz (TYP.) at $V_{CC}$ = 5V
- LOW POWER DISSIPATION
  $I_{CC}$ = 2 $\mu$A (MAX.) at $T_A$ = 25°C
- HIGH NOISE IMMUNITY
  $V_{NIH}$ = $V_{NIL}$ = 28% $V_{CC}$ (MIN.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}|$ = $I_{OL}$ = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH}$ = $t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  $V_{CC}$ (OPR) = 2V to 6V
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS73

**B1N**
Plastic Package

**F1**
Ceramic Frit Seal Package*

**M1**
Micro Package

**C1**
Plastic Chip Carrier

ORDERING NUMBERS:
M54HC73 F1
M74HC73 B1N
M74HC73 F1
M74HC73 C1
M74HC73 M1

### DESCRIPTION

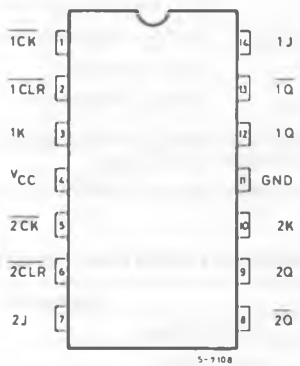
The M54/74HC73 is a high speed CMOS DUAL J-K FLIP FLOP WITH CLEAR fabricated in silicon gate C²MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low power consumption. Depending on the logic level applied to J and K inputs, this device changes state on the negative going transition of clock input pulse ($\overline{CK}$). The clear function is accomplished independently of the clock condition when the clear input ($\overline{CLR}$) is taken low. All inputs are equipped with protection circuits against static discharge and transient excess voltage.

### TRUTH TABLE

| INPUTS | | | | OUTPUTS | | FUNCTION |
|---|---|---|---|---|---|---|
| $\overline{CLR}$ | J | K | $\overline{CK}$ | Q | $\overline{Q}$ | |
| L | X | X | X | L | H | CLEAR |
| H | L | L | ↓ | Qn | $\overline{Qn}$ | NO CHANGE |
| H | L | H | ↓ | L | H | — |
| H | H | L | ↓ | H | L | — |
| H | H | H | ↓ | $\overline{Qn}$ | Qn | TOGGLE |
| H | X | X | ↑ | Qn | $\overline{Qn}$ | NO CHANGE |

X: DON'T CARE

**PIN CONNECTIONS** (top view)

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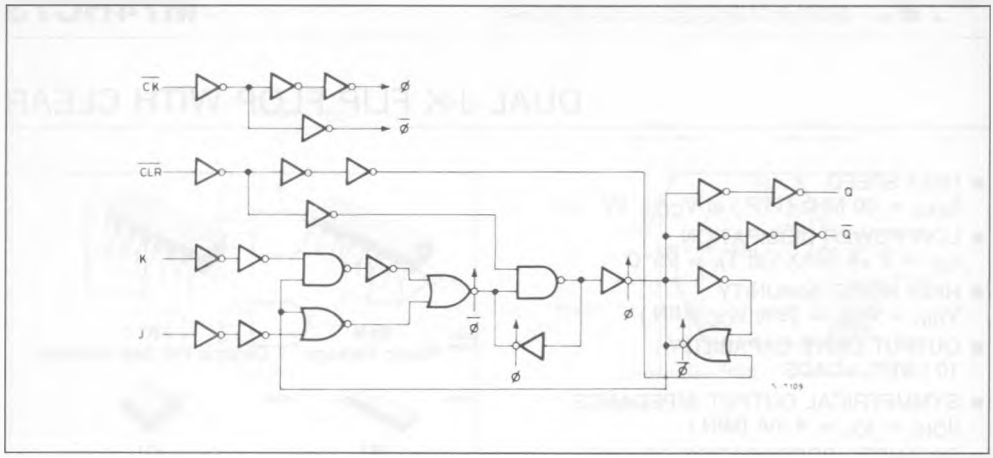
**LOGIC DIAGRAM** (1/2 of device show)




## ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{CC}$ | Supply Voltage | −0.5 to 7 | V |
| $V_I$ | DC Input Voltage | −0.5 to $V_{CC}$ + 0.5 | V |
| $V_O$ | DC Output Voltage | −0.5 to $V_{CC}$ + 0.5 | V |
| $I_{IK}$ | DC Input Diode Current | ± 20 | mA |
| $I_{OK}$ | DC Output Diode Current | ± 20 | mA |
| $I_O$ | DC Output Source Sink Current Per Output Pin | ± 25 | mA |
| $I_{CC}$ or $I_{GND}$ | DC $V_{CC}$ or Ground Current | ± 50 | mA |
| $P_D$ | Power Dissipation | 500 (*) | mW |
| $T_{stg}$ | Storage Temperature | −65 to 150 | °C |

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: ≡65°C derate to 300 mW by 10 mW/°C: 65°C to 85°C

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Value | | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | 2 to 6 | | V |
| $V_I$ | Input Voltage | 0 to $V_{CC}$ | | V |
| $V_O$ | Output Voltage | 0 to $V_{CC}$ | | V |
| $T_A$ | Operating Temperature 74HC Series<br>54HC Series | − 40 to 85<br>−55 to 125 | | °C |
| $t_r$, $t_f$ | Input Rise and Fall Time | $V_{CC}$ | 2 V: 0 to 1000<br>4.5V: 0 to 500<br>6 V: 0 to 400 | ns |

## DC SPECIFICATIONS

| Symbol | Parameter | $V_{CC}$ | Test Condition | | $T_A = 25°C$ 54HC and 74HC | | | −40 to 85°C 74HC | | −55 to 125°C 54HC | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | Min. | Typ. | Max. | Min. | Max. | Min. | Max. | |
| $V_{IH}$ | High Level Input Voltage | 2.0 | | | 1.5 | — | — | 1.5 | — | 1.5 | — | V |
| | | 4.5 | | | 3.15 | — | — | 3.15 | — | 3.15 | — | |
| | | 6.0 | | | 4.2 | — | — | 4.2 | — | 4.2 | — | |
| $V_{IL}$ | Low Level Input Voltage | 2.0 | | | — | — | 0.5 | — | 0.5 | — | 0.5 | V |
| | | 4.5 | | | — | — | 1.35 | — | 1.35 | — | 1.35 | |
| | | 6.0 | | | — | — | 1.8 | — | 1.8 | — | 1.8 | |
| $V_{OH}$ | High Level Output Voltage | 2.0 | $V_I$ | $I_O$ | 1.9 | 2.0 | — | 1.9 | — | 1.9 | — | V |
| | | 4.5 | $V_{IH}$ or $V_{IL}$ | −20 μA | 4.4 | 4.5 | — | 4.4 | — | 4.4 | — | |
| | | 6.0 | | | 5.9 | 6.0 | — | 5.9 | — | 5.9 | — | |
| | | 4.5 | | −4.0 mA | 4.18 | 4.31 | — | 4.13 | — | 4.10 | — | |
| | | 6.0 | | −5.2 mA | 5.68 | 5.8 | — | 5.63 | — | 5.60 | — | |
| $V_{OL}$ | Low Level Output Voltage | 2.0 | $V_{IH}$ or $V_{IL}$ | 20 μA | — | 0 | 0.1 | — | 0.1 | — | 0.1 | V |
| | | 4.5 | | | — | 0 | 0.1 | — | 0.1 | — | 0.1 | |
| | | 6.0 | | | — | 0 | 0.1 | — | 0.1 | — | 0.1 | |
| | | 4.5 | | 4.0 mA | — | 0.17 | 0.26 | — | 0.33 | — | 0.40 | |
| | | 6.0 | | 5.2 mA | — | 0.18 | 0.26 | — | 0.33 | — | 0.40 | |
| $I_I$ | Input Leakage Current | 6.0 | $V_I = V_{CC}$ or GND | | — | — | ±0.1 | — | ±1 | — | ±1 | μA |
| $I_{CC}$ | Quiescent Supply Current | 6.0 | $V_I = V_{CC}$ or GND | | — | — | 2 | — | 20 | — | 40 | μA |

## AC ELECTRICAL CHARACTERISTICS ($V_{CC} = 5V$, $T_A = 25°C$, $C_L = 15pF$, Input $t_r = t_f = 6ns$)

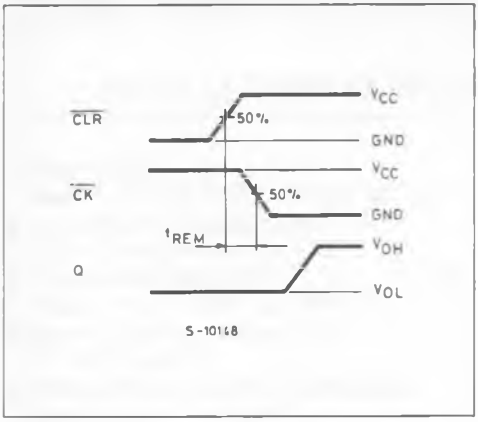
| Symbol | Parameter | 54HC and 74HC | | | Unit |
|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | |
| $t_{TLH}$ $t_{THL}$ | Output Transition Time | | 4 | 8 | ns |
| $t_{PLH}$ $t_{PHL}$ | Propagation Delay Time ($\overline{CK}$-Q, $\overline{Q}$) | | 16 | 25 | ns |
| $t_{PLH}$ $t_{PHL}$ | Propagation Delay Time ($\overline{CLR}$-Q, $\overline{Q}$) | | 20 | 32 | ns |
| $f_{MAX}$ | Maximum Clock Frequency | 33 | 60 | | MHz |

**AC ELECTRICAL CHARACTERISTICS** ($C_L = 50pF$, Input $t_r = t_f = 6ns$)

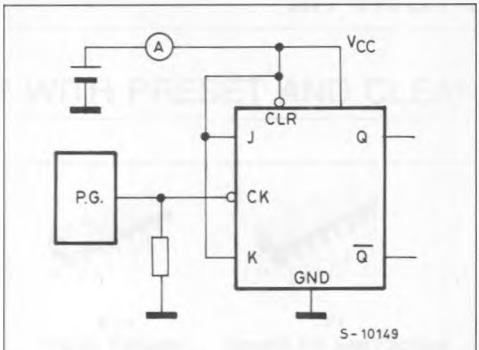
| Symbol | Parameter | $V_{CC}$ | Test Condition | $T_A = 25°C$ 54HC and 74HC | | | −40 to 85°C 74HC | | −55 to 125°C 54HC | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Min. | Typ. | Max. | Min. | Max. | Min. | Max. | |
| $t_{TLH}$ $t_{THL}$ | Output Transition Time | 2.0 | | — | 30 | 75 | — | 90 | — | 110 | ns |
| | | 4.5 | | — | 8 | 15 | — | 18 | — | 22 | |
| | | 6.0 | | — | 7 | 13 | — | 15 | — | 19 | |
| $t_{PLH}$ $t_{PHL}$ | Propagation Delay Time ($\overline{CK}$-Q, $\overline{Q}$) | 2.0 | | — | 76 | 150 | — | 190 | — | 225 | ns |
| | | 4.5 | | — | 19 | 30 | — | 38 | — | 45 | |
| | | 6.0 | | — | 16 | 26 | — | 33 | — | 38 | |
| $t_{PLH}$ $t_{PHL}$ | Propagation Delay Time ($\overline{CLR}$-Q, $\overline{Q}$) | 2.0 | | — | 96 | 185 | — | 230 | — | 280 | ns |
| | | 4.5 | | — | 24 | 37 | — | 46 | — | 56 | |
| | | 6.0 | | — | 20 | 31 | — | 39 | — | 48 | |
| $f_{MAX}$ | Maximum Clock Frequency | 2.0 | | 6 | 13 | — | 5 | — | 4 | — | MHz |
| | | 4.5 | | 30 | 52 | — | 24 | — | 20 | — | |
| | | 6.0 | | 35 | 61 | — | 28 | — | 23 | — | |
| $t_{W(L)}$ $t_{W(H)}$ | Minimum Pulse Width ($\overline{CK}$) | 2.0 | | — | 30 | 75 | — | 95 | — | 110 | ns |
| | | 4.5 | | — | 8 | 15 | — | 19 | — | 22 | |
| | | 6.0 | | — | 7 | 13 | — | 16 | — | 19 | |
| $t_{W(L)}$ | Minimum Pulse Width ($\overline{CL}$) | 2.0 | | — | 30 | 75 | — | 95 | — | 110 | ns |
| | | 4.5 | | — | 8 | 15 | — | 19 | — | 22 | |
| | | 6.0 | | — | 7 | 13 | — | 16 | — | 19 | |
| $t_s$ | Minimum Set-Up Time | 2.0 | | — | 35 | 100 | — | 125 | — | 150 | ns |
| | | 4.5 | | — | 9 | 20 | — | 25 | — | 30 | |
| | | 6.0 | | — | 8 | 17 | — | 21 | — | 26 | |
| $t_h$ | Minimum Hold Time | 2.0 | | — | — | 0 | — | 0 | — | 0 | ns |
| | | 4.5 | | — | — | 0 | — | 0 | — | 0 | |
| | | 6.0 | | — | — | 0 | — | 0 | — | 0 | |
| $t_{REM}$ | Minimum Removal Time | 2.0 | | — | 5 | 50 | — | 65 | — | 75 | ns |
| | | 4.5 | | — | 1 | 10 | — | 13 | — | 15 | |
| | | 6.0 | | — | 1 | 9 | — | 11 | — | 13 | |
| $C_{IN}$ | Input Capacitance | | | — | 5 | 10 | — | 10 | — | 10 | pF |
| $C_{PD}$ (*) | Power Dissipation Capacitance | | | — | 42 | — | — | — | — | — | pF |

Note (*) $C_{PD}$ is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit)
Average operating current can be obtained by the following equation $I_{CC}$ (Opr.) = $C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/2$ (per F/F)

## SWITCHING CHARACTERISTICS TEST WAVEFORM




## TEST CIRCUIT $I_{CC}$(Opr)




INPUT TRANSITION TIME IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

## SWITCHING CHARACTERISTICS TEST WAVEFORMS