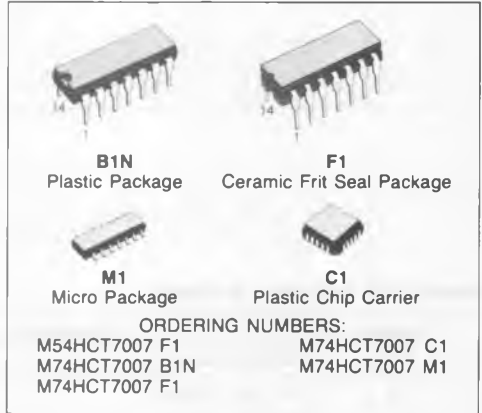


HEX BUFFER

- **LOW POWER DISSIPATION**
 $I_{CC} = 1\mu A$ (MAX.) at $T_A = 25^\circ C$
- **COMPATIBLE WITH TTL OUTPUTS**
 $V_{IH} = 2V$ (MIN) $V_{IL} = 0.8V$ (MAX)
- **OUTPUT DRIVE CAPABILITY**
 10 LSTTL LOADS
- **SYMMETRICAL OUTPUT IMPEDANCE**
 $|I_{OL}| I_{OL} = 4mA$ (MIN.)
- **BALANCED PROPAGATION DELAYS**
 $t_{PLH} = t_{PHL}$
- **PIN AND FUNCTION COMPATIBLE**
 WITH 54/74LS07

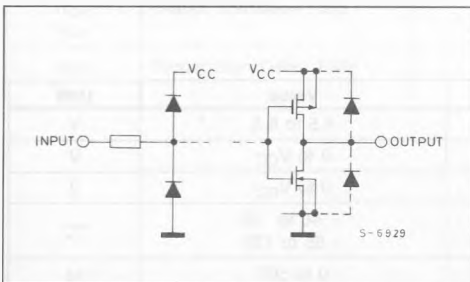
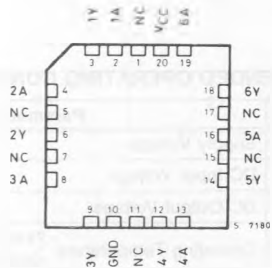
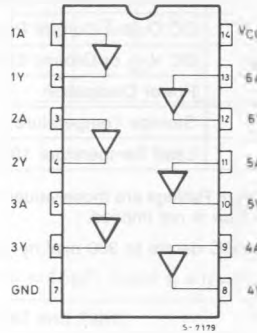

DESCRIPTION

The M54/74HCT7007 is a high speed CMOS HEX BUFFER fabricated in silicon gate C²MOS technology.

It has the same high speed performance of LSTTL combined with true CMOS low power consumption. All inputs are equipped with protection circuits against static discharge and transient excess voltage.

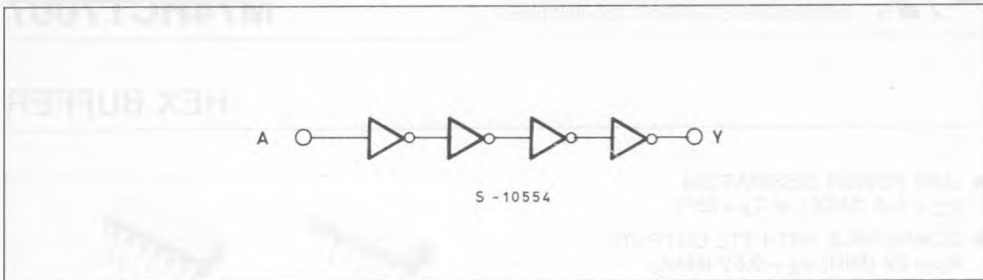
This integrated circuit has totally compatible, input and output characteristic, with standard 54/74 LSTTL logic families.

M54HCT/74HCT devices are designed to directly interface HSC²MOS systems with TTL and NMOS components. These devices are also plug in replacement for LSTTL devices giving a reduction of power consumption.

INPUT AND OUTPUT EQUIVALENT CIRCUIT

PIN CONNECTIONS (top view)


NC =
No Internal
Connection

CIRCUIT DIAGRAM (Per Circuit)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	- 0.5 to 7	V
V_I	DC Input Voltage	- 0.5 to $V_{CC} + 0.5$	V
V_O	DC Output Voltage	- 0.5 to $V_{CC} + 0.5$	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Current Per Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	- 65 to 150	$^{\circ}C$
T_L	Lead Temperature 10 sec	300	$^{\circ}C$

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: $\cong 65^{\circ}C$ derate to 300 mW by 10 mW/ $^{\circ}C$: $65^{\circ}C$ to $85^{\circ}C$

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	4.5 to 5.5	V
V_I	DC Input Voltage	0 to V_{CC}	V
V_O	DC Output Voltage	0 to V_{CC}	V
T_A	Operating Temperature	74HC Series 54HC Series	$^{\circ}C$
t_r, t_f	Input Rise and Fall Time	- 40 to 85 - 55 to 125	ns
		0 to 500	

DC SPECIFICATIONS

Symbol	Parameter	V _{CC}	Test Condition	T _A = 25°C 54HC and 74HC			- 40 to 85°C 74HC		- 55 to 125°C 54HC		Unit	
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.		
V _{IH}	High Level Input Voltage	4.5 to 5.5		2.0	—	—	2.0	—	2.0	—	V	
V _{IL}	Low Level Input Voltage	4.5 to 5.5		—	—	0.8	—	0.8	—	0.8	V	
V _{OH}	High Level Output Voltage	4.5	V _I	I _O	4.4	4.5	—	4.4	—	4.4	—	V
			V _{IH} or V _{IL}	- 20 μA								
V _{OL}	Low Level Output Voltage	4.5	V _I	I _O	—	0	0.1	—	0.1	—	0.1	V
			V _{IH} or V _{IL}	- 4.0 mA								
I _{IN}	Input Leakage Current	5.5	V _I = V _{CC} or GND	—	—	±0.1	—	±1	—	±1	μA	
												I _{CC}
ΔI _{CC}	Additional worst case supply current	5.5	Per Input pin V _{IN} = 2.4V Other Input at V _{CC} or GND I _O = 0	—	—	2.0	—	2.9	—	3.0	mA	

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V, T_A = 25°C, C_L = 15pF, Input t_r = t_f = 6ns)

Symbol	Parameter	54HC and 74HC			Unit
		Min.	Typ.	Max.	
t _{TLH} t _{THL}	Output Transition Time		4	8	ns
t _{PLH} t _{PHL}	Propagation Delay Time		14	22	ns

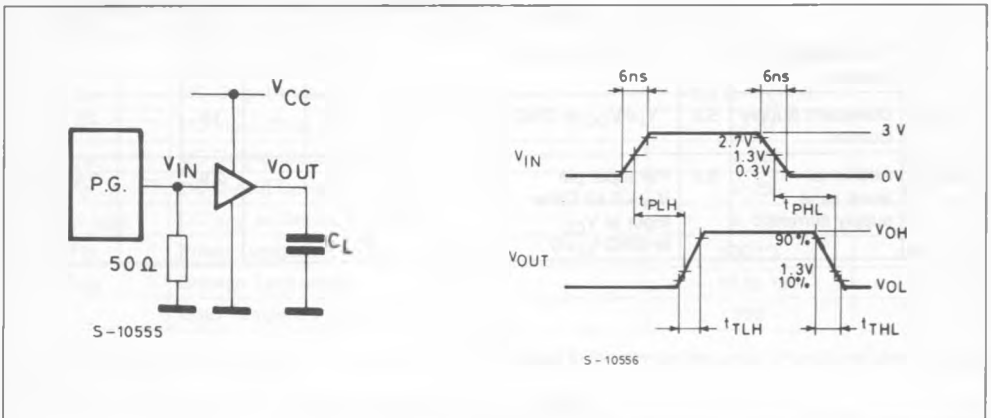
AC ELECTRICAL CHARACTERISTICS ($C_L = 50\text{pF}$, Input $t_r = t_f = 6\text{ns}$)

Symbol	Parameter	V_{CC}	Test Condition	$T_A = 25^\circ\text{C}$ 54HC and 74HC			$-40\text{ to }85^\circ\text{C}$ 74HC		$-55\text{ to }125^\circ\text{C}$ 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH}	Output Transition Time	4.5		—	8	15	—	19	—	22	ns
t_{PLH} t_{PHL}	Propagation Delay Time	4.5		—	16	26	—	33	—	39	ns
C_{IN}	Input Capacitance			—	5	10	—	10	—	10	pF
$C_{PD} (*)$	Power Dissipation Capacitance			—	28	—	—	—	—	—	pF

Note (*) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (Refer to Test circuit).

Average operating current can be obtained from the equation: $I_{CC(opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/6$ (per Buffer)

SWITCHING CHARACTERISTICS TEST CIRCUIT



TEST CIRCUIT I_{CC} (Opr.)

