SGS-THOMSON MICROELECTRONICS

M5913
M5914

COMBINED SINGLE CHIP PCM CODEC AND FILTER

- M5914 ASYNCHRONOUS CLOCK, 8th BIT SIGNALING, LOOP BACK TEST CAPABILITY
- M5913 SYNCHRONOUS CLOCKS ONLY
- AT&T D3/D4 AND CCITT COMPATIBLE
- TWO TIMING MODES :
  FIXED DATA RATE MODE : 1.536 MHz, 1.544 MHz, 2.048 MHz
  VARIABLE DATA MODE : 64 kHz - 4.096 MHz
- PIN SELECTABLE u-LAW OR A-LAW OPERATION
- NO EXTERNAL COMPONENTS FOR SAMPLE AND HOLD AND AUTO ZERO FUNCTIONS
- LOW POWER DISSIPATION :
  0.5 mW POWER DOWN 70 mW OPERATING
- EXCELLENT POWER SUPPLY REJECTION

DESCRIPTION

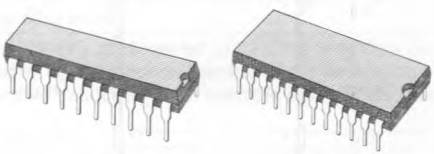
The M5913 and M5914 are fully integrated PCM (pulse code modulation) codecs and transmit/receive filter using CMOS silicon gate technology.

The primary applications for the M5913 and M5914 are telephone systems :

- Switching - M5913-Digital PBX's and Central Office Switching Systems
- Transmission - M5914-D3/D4 Channel Banks
- Concentration - M5913 and M5914-Subscriber Carrier and Concentrators.

The wide dynamic range of the M5913 and M5914 (78 dB) and the minimal conversion time make them ideal products for other applications such as :

Voice Store and Forward - Digital Echo Cancellers - Secure Communications Systems - Satellite Earth Stations.



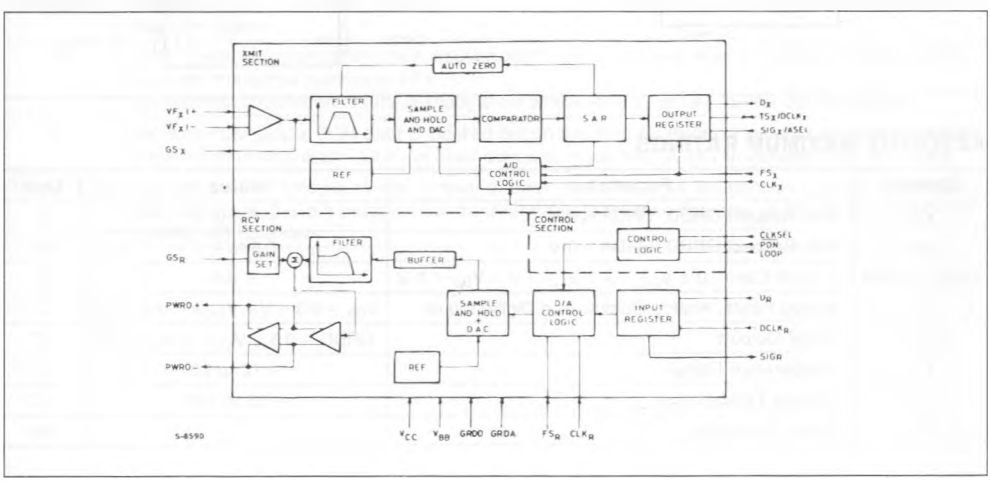
DIP20
(Plastic and Ceramic)

DIP24
(Plastic and Ceramic)

ORDER CODES :

M5913B1	M5913F1
M5914B1	M5914F1

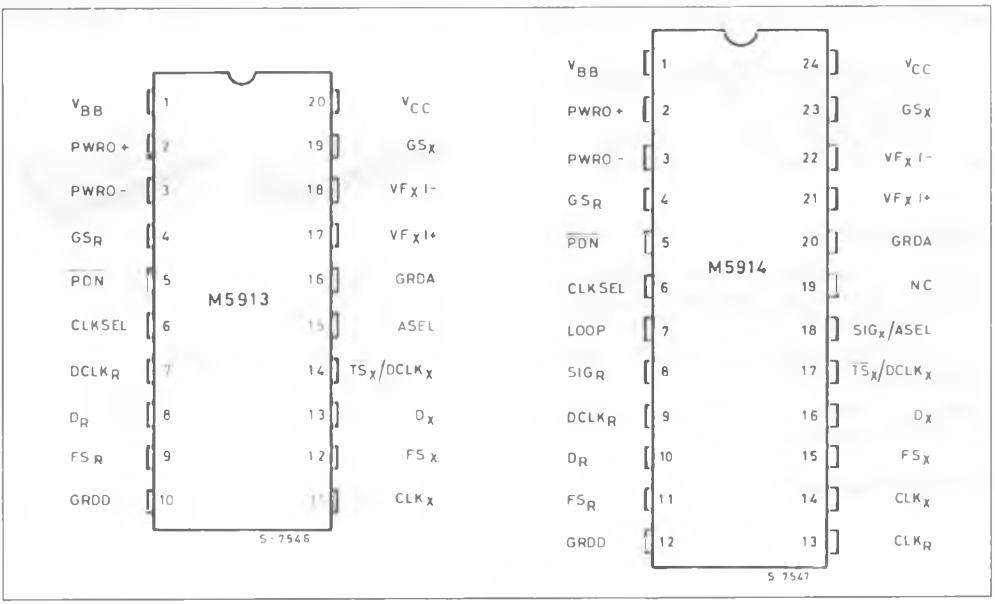
BLOCK DIAGRAM



PIN NAMES

V_{BB}	Power (– 5 V)	GS_X	Gain Control
PWRO+, PWRO–	Power Amplifier Outputs	$VF_XI–$, VF_XI+	Analog Inputs
GS_R	Gain Setting Input for Receive Channel	GRDA	Analog Ground
$\overline{PDN}$	Power Down Select	NC	No Connect
CLKSEL	Master Clock Select	SIG_X	Transmit Digital Signaling Input
LOOP	Analog Loop Back	$\overline{ASEL}$	μ or A-law Select
SIG_R	Signaling Bit Output	$\overline{TS}_X$	Digital Output - Timeslot Strobe
$DCLK_R$	Receive Data Rate Clock	$DCLK_X$	Transmit Data Rate Clock
D_R	Receive Channel Input	D_X	Transmit (digital) Output
FS_R	Receive Frame Synchronization Clock	FS_X	Transmit Frame Synchronization Clock
GRDD	Digital Ground	CLK_X	Transmit Master Clock
V_{CC}	Power (+ 5 V)	CLK_R	Receive Master Clock

PIN CONNECTION



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	With Respect GRDD, GRDA = 0 V	– 0.6 to 7	V
V_{BB}	With Respect GRDD, GRDA = 0 V	0.6 to – 7	V
GRDD, GRDA	In Such Case : $0 \leq V_{CC} \leq +7$ V, -7 V $\leq V_{BB} \leq 0$ V	± 0.3	V
$V_{I/O}$	Analog Inputs, Analog Outputs and Digital Inputs	$V_{BB} - 0.3 \leq V_{IN}/V_{OUT} \leq V_{CC} + 0.3$	V
$V_{O\ DIG}$	Digital Outputs	$GRDD - 0.3 \leq V_{OUT} \leq V_{CC} + 0.3$	V
T_{op}	Temperature Range	– 10 to 80	°C
T_{stg}	Storage Temperature	– 65 to 150	°C
P_{tot}	Power Dissipation	1	W

PIN DESCRIPTIONS

Symbol	Function
V_{BB}	Most negative supply. input voltage is – 5 V ± 5 %.
PWRO+	Non-inverting Output of Power Amplifier. Can drive transformer hybrids or high impedance loads directly in either a differential or single ended configuration.
PWRO–	Inverting Output of Power Amplifier. Functionally identical and complementary to PWRO+.
GS_R	Input to the Gain Setting Network on the Output Power Amplifier. Transmission level can be adjusted over a 12 dB range depending on the voltage at GS_R.
$\overline{PDN}$	Power Down Select. When $\overline{PDN}$ is TTL high, the device is active. When low. the device is powered down.
CLKSEL	Input which must be pinstrapped to reflect the master clock frequency at CLK_X, CLK_R. CLKSEL = V_{BB} ..... 2.048 MHz CLKSEL = GRDD ..... 1.544 MHz CLKSEL = V_{CC} ..... 1.536 MHz
LOOP	Analog Loopback. When this pin is TTL high, the receive output (PWRO+) is internally connected to VF_XI+, GS_R is internally connected top PWRO–, and VF_XI- 0s internally connected to GS_X. A 0 dBm0 digital signal input at D_R is returned as a + 3 dBm0 digital signal outupt at D_X.
SIG_R	Signaling Bit Output, Receive Channel. In fixed data rate mode, SIG_R outputs the logical state of the eighth bit of the PCM word in the most recent signaling frame.
$DCLK_R$	Selects the fixed or variable data rate mode. When $DCLK_R$ is connected to V_{BB}, the fixed data rate mode is selected. When $DCLK_R$ is not connected to V_{BB}, the device operates in the variable data rate mode. In this mode $DCLK_R$, becomes the receive data clock which operates a TTL levels from 64 kB to 4.096 MB data rates.
D_R	Receive PCM Input. PCM data is clocked in on this lead on eight consecutive negative transitions of the receive data clock ; CLK_R in the fixed data rate mode and $DCLK_R$ in variable data rate mode.
FS_R	8 KHz frame synchronization clock input/timeslot enable, receive channel. A multifunction input which in fixed data rate mode distinguishes between signaling and non-signaling frames by means of a double or single wide pulse respectively. In variable data rate mode this signal must remain high for the entire length of the timeslot. The receive channel enters the standby state whenever FS_R is TTL low for 30 milliseconds.
GRDD	Digital Ground for all Internal Logic Circuits. Not Internally Tied to GRDA.
CLK_R	Receive master and data clock for the fixed data rate mode : receive master clock only in variable data rate mode.
CLK_X	Transmit master and data clock for the fixed data rate mode, transmit master clock only in variable data rate mode.
FS_X	8 KHz frame synchronization clock input/timeslot enable, transmit channel. Operates independently but in an analogous manner to FS_R. The transmit channel enters the standby state whenever FS_X is TTL low for 30 milliseconds.
D_X	Transmit PCM output PCM data is clocked out on this lead on eight consecutive positive transitions of the transmit data clock : CLK_X in fixed data rate mode and $DCLK_X$ in variable data rate mode.
$\overline{TS_X}/DCLK_X$	Transmit channel timeslot strobe (output) or data clock (input) for the transmit channel. In variable data rate mode, this pin becomes the transmit data clock which operates at TTL levels from 64 KB to 4.096 MB data rates.

PIN DESCRIPTIONS (continued)

Symbol	Function
SIG_X/ASEL	A dual purpose selects μ-law and pin. When connected to V_{BB}. A-law operation is selected. When it is not connected to V_{BB} this pin is a TTL level input for signaling operation. This input is transmitted as the eighth bit of the PCM word during signaling frames on the D_X lead.
NC	No Connect
GRDA	Analog Ground Return for all Internal Voice Circuits. Not internally connected to GRDD.
VF_XI+	Non-inverting analog input to uncommitted transmit operational amplifier.
VF_XI-	Inverting analog input to uncommitted transmit operational amplifier.
GS_X	Output terminal of on-chip uncommitted op amp. Internally, this is the voice signal input to the transmit filter.
V_{CC}	Most Positive Supply. Input Voltage is + 5 V ± 5 %.

FUNCTIONAL DESCRIPTION

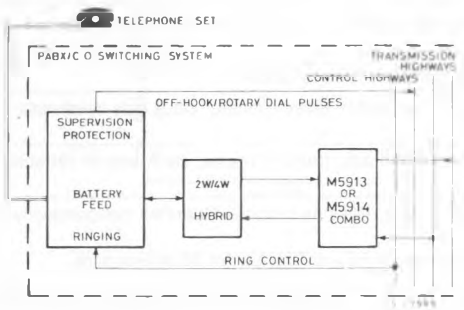
The M5913 and M5914 provide the analog-to-digital and the digital-to-analog conversions and the transmit and receive filtering necessary to interface a full duplex (4 wires) voice telephone circuit with the PCM highways of a time division multiplexed (TDM) system. They are intended be used at the analog termination of a PCM line or trunk.

The following major functions are provided :

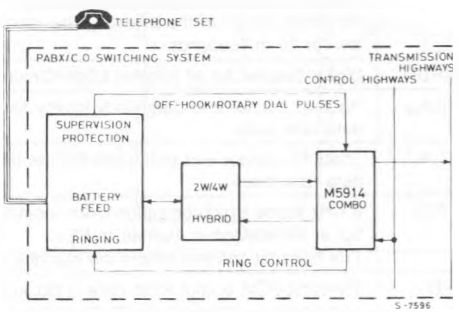
- Bandpass filtering of the analog signals prior to encoding and after decoding
- Encoding and decoding of voice and call progress information
- Encoding and decoding of the signaling and supervision information

Figure 3 : Typical Line Terminations.

SWITCHING

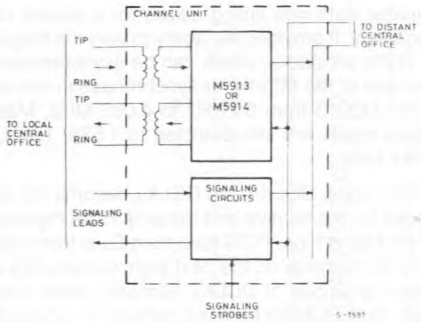


Functional block diagram of a line circuit with separate signaling control highways.

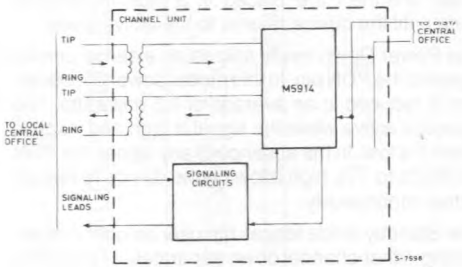


Functional block diagram of a line circuit with borrowed 8th bit signaling

CHANNEL BANKS



A typical CCITT channel unit.



A typical 4-wire channel unit with signaling using borrowed 8th bit.

GENERAL OPERATION

SYSTEM RELIABILITY FEATURES

The combo-chip can be powered up by pulsing FS_X and/or FS_R while a TTL high voltage is applied to PDN, provided that all clocks and supplies are connected. The M5913 and M5914 have internal resets on power up (or when V_{BB} or V_{CC} are re-applied) in order to ensure validity of the digital outputs and thereby maintain integrity of the PCM highway.

On the transmit channel, digital outputs D_X and $\overline{TS}_X$ are held in a high impedance state for approximately four frames (500µs) after power up or application of V_{BB} or V_{CC}. After this delay, DX, $\overline{TS}_X$, and signaling will be functional and will occur in the proper timeslot. The analog circuits on the transmit side require approximately 40 milliseconds to reach their equilibrium value due to the autozero circuit setting time. Thus, valid digital information, such as for on/off hook detection, is available almost immediately, while analog information is available after some delay.

On the receive channel, the digital output SIG_R is also held low for a maximum of four frames after power up or application of V_{BB} or V_{CC}. SIG_R will remain low thereafter until it is updated by a signaling frame.

To further enhance system reliability, $\overline{TS}_X$ and $\overline{D}_X$ will be placed in a high impedance state approximately 20µs after an interruption of CLK_X. Similarly, SIG_R will be held low approximately 20µs after an interruption of CLK_R. These interruptions could possibly occur with some kind of fault condition.

POWER DOWN AND STANDBY MODES

To minimize power consumption, two power down modes are provided in which most M5913/M5914

Table 1 : Power-down Methods.

Device Status	Power-down Method	Digital Outputs Status
Power Down Mode	$\overline{PDN}$ = TTL low	$\overline{TS}_X$ and D_X are placed in a high impedance state and SIG_R is placed in a TTL low state within 10 µs.
Standby Mode	FS_X and FS_R are TTL low.	$\overline{TS}_X$ and D_X are placed in a high impedance state and SIGR is placed in a TTL low state 30 milliseconds after FS_X and FS_R are removed.
Only transmit is on standby.	FS_X is TTL low.	$\overline{TS}_X$ and D_X are placed in a high impedance state within 30 milliseconds.
Only receive is on standby.	FS_R is TTL low.	SIG_R is placed in a TTL low state within 30 milliseconds.

functions are disabled. Only the power down, clock, and frame sync buffers, which are required to power up the device, are enabled in these modes. As shown in Table 1, the digital outputs on the appropriate channels are placed in a high impedance state until the device returns to the active mode.

The Power Down mode utilizes an external control signal to the PDN pin. In this mode, power consumption is reduced to an average of 0.5 milliwatts. The device is active when the signal is high and inactive when it is low. In the absence of any signal, the PDN pin floats to TTL high allowing the device to remain active continuously.

The Standby mode leaves the user an option of powering either channel down separately or powering the entire device down by selectively removing FS_X and/or FS_R. With both channels in the standby state, power consumptions is reduced to an average of 1 milliwatts. If transmit only operation is desired, FS_X should be applied to the device while FS_R is held low. Similarly, if receive only operation is desired, FS_R should be applied while FS_X is held low.

FIXED DATA RATE MODE

Fixed data rate timing, is selected by connecting $DCLK_R$ to V_{BB}. It employs master clocks CLK_X and CLK_R, frame synchronization clocks FS_X and FS_R, and output $\overline{TS}_X$.

CLK_X and CLK_R serve both as master clocks to operate the codec and filter sections and bit clocks to clock the data in and out from the PCM highway. FS_X and FS_R are 8 kHz inputs which set the sampling frequency and distinguish between signaling and non-signaling frames by their pulse width. A frame synchronization pulse which is one master clock wide designates a non-signaling frame, while a double wide sync pulse enables the signaling function. TS_X is a timeslot strobe/buffer enable output which gates the PCM word onto the PCM highway when an external buffer is used to drive the line.

Data is transmitted on the highway at D_X on the first eight positive transitions of CLK_X following the rising edge of FS_X. Similarly on the receive side, data is received on the first eitht falling edges of CLK_R. The frequency of CLK_X and CLK_R is selected by the CLKSEL pin to be either 1.536, 1.544 or 2.048 MHz. No other frequency of operation is allowed in the fixed data rate mode.

VARIABLE DATA RATE MODE

Variable data rate timing is selected by connecting $DCLK_R$ to the bit clock for the receive PCM highway rather than to V_{BB}. It employs master clocks CLK_X and CLK_R, bit clocks $DCLK_R$ and $DCLK_X$ and frame synchronization clocks FS_R and FS_X.

Variable data rate timing allows for a flexible data frequency. It provides the ability to vary the frequency of the bit clocks, which can be asynchronous in the case of the M5914, or synchronous in the case of the M5913 from 64 KHz to 4.096 MHz. Master clocks inputs are still restricted to 1.536, 1.544, or 2.048 MHz.

In this mode, $DCLK_R$ and $DCLK_X$ become the data clocks for the receive and transmit PCM highways. While FS_X is high, PCM data from D_X is transmitted onto the highway on the next eight consecutive positive transitions of $DCLK_X$. Similary, while FS_R is high, each PCM bit from the highway is received by D_R on the next eight consecutive negative transition of $DCLK_R$.

On the transmit side, the PCM word will be repeated in all remaining timeslots in the 125 s frame as long as $DCLK_X$ is pulsed and FS_X is held high. This feature allows the PCM word to be transmitted to the PCM highway more than once per frame, if desired, and is only available in the variable data rate mode. Conversely, signaling is only allowed in the fixed data rate mode since the variable mode provides no means with which to specify a signaling frame.

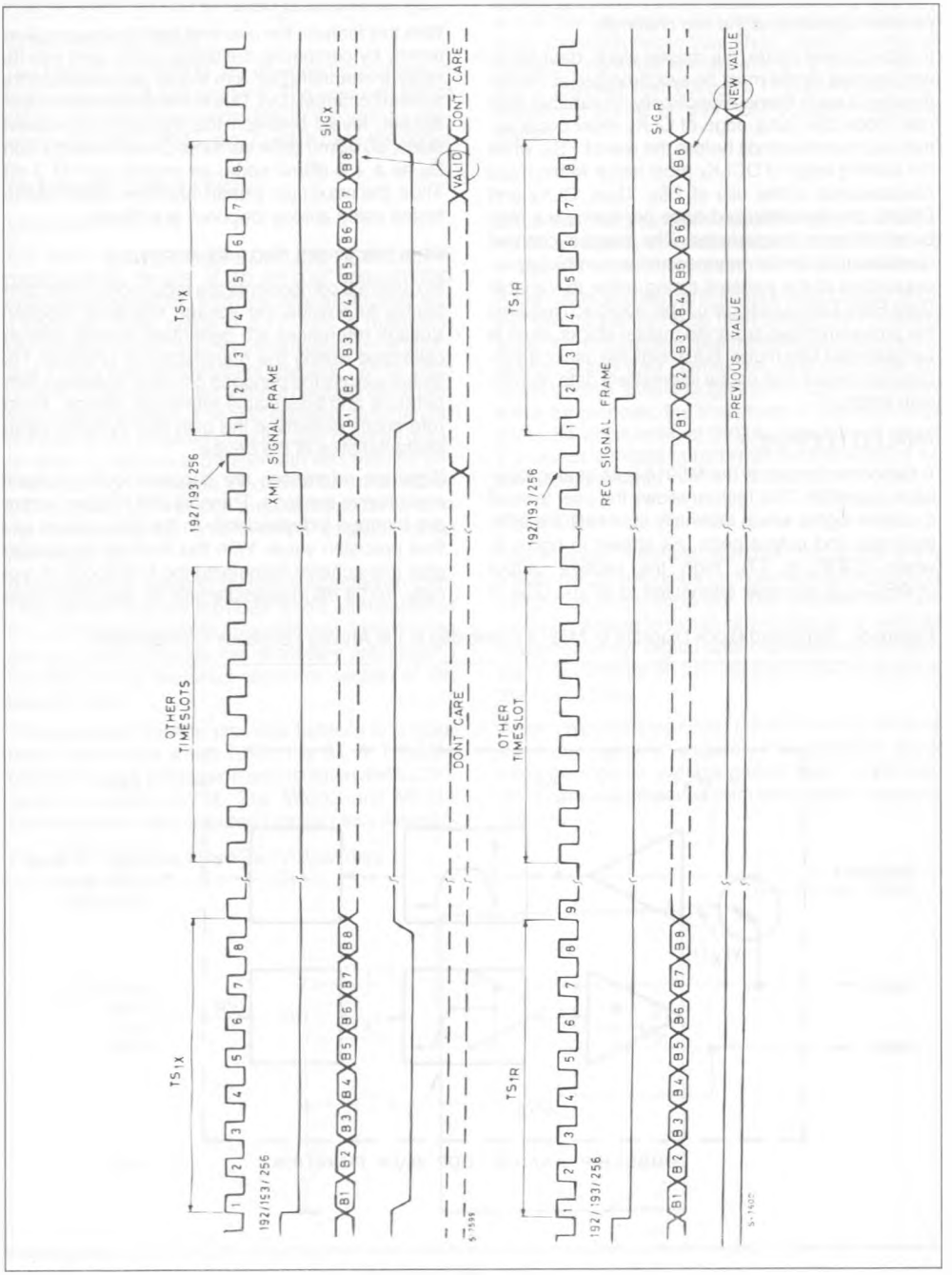
SIGNALING

Signaling can only be performed with the 24-pin device in the fixed data rate timing mode ($DCLK_R$ = V_{BB}). Signaling frames on the transmit and receive sides are independent of one another and are selected by a double-width frame sync pulse on the appropriate channel. During a transmit signaling frame, the codec will encode the incoming analog signal and substitute the signal present on SIG_X for the least significant bit of the encoded PCM word. Similarly, in a receive signaling frame, the codec will decode the seven most significant bits according to CCITT recommendation G.733 and output the logical state of the LSB on the SIG_R lead until it is updated in the next signaling frame. Timing relationships for signaling operation are shown in figure 4.

ASYNCHRONOUS OPERATION

The M5914 can be operated with asynchronous clocks in either the fixed or variable data rate modes. In order to avoid crosstalk problems associated with special interrupt circuitry the design of the M5913/M5914 combochip includes separate digital-

Figure 4 : Signaling Timing (used only with fixed data rate mode).



to-analog converters and voltage references on the transmit and receive sides to allow completely independent operation of the two channels.

In either timing mode, the master clock, data clock, and timeslot strobe must be synchronized at the beginning of each frame. Specifically, in variable data rate mode the rising edge of CLK_X must occur within t_{FSD} nanoseconds before the rise of FS_X, while the leading edge of $DCLK_X$ must occur within t_{TSDX} nanoseconds of the rise of FS_X. Thus, CLK_X and $DCLK_X$ are synchronized once per frame but may be of different frequencies. The receive channel operates in a similar manner and is completely independent of the transmit timing (refer to Variable Data Rate Timing Diagram). This approach requires the provision of two separate master clocks, even in variable data rate mode, but avoids the use of a synchronizer which can cause intermittent data conversion errors.

ANALOG LOOPBACK

A distinctive feature of the M5914 is its analog loopback capability. This feature allows the user to send a control signal which internally connects the analog input and output ports. As shown in figure 5, when LOOP is TTL high the receive output (PWRO+) is internally connected to VF_XI+, GS_R in internally connected to PWRO- and VF_XI- is internally connected to GS_X.

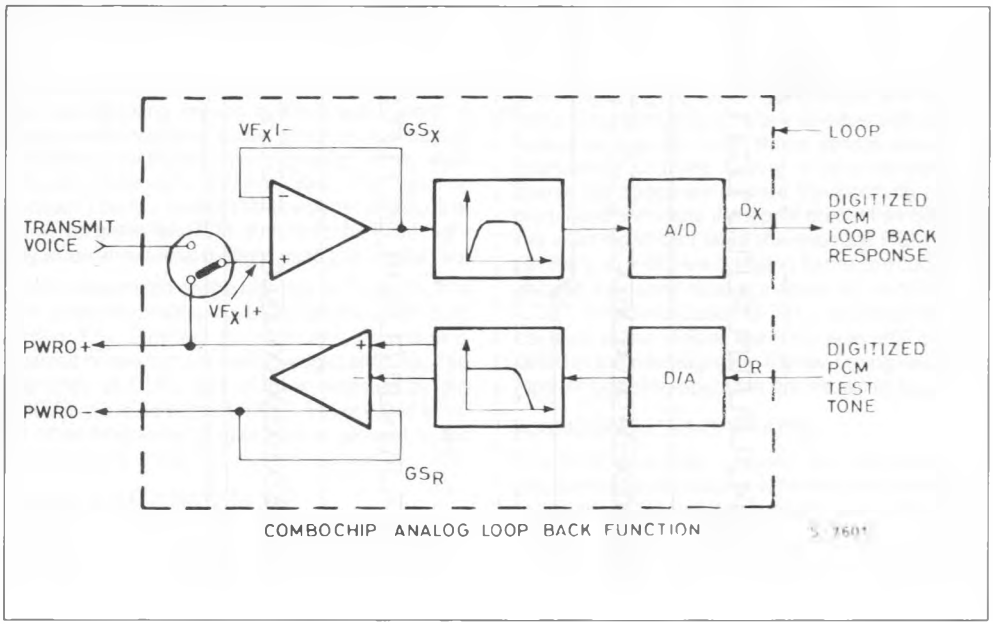
With this feature, the user can test the line circuit remotely by comparing the digital codes sent into the receive channel (D_R) with those generated on the transmit channel (D_X). Due to the difference in transmission levels between the transmit and receive sides, a0 dBm0 code sent into D_R will emerge from D_X as a + 3 dBm0 code. an implicit gain of 3 dB. Thus, the maximum signal input level which can be tested using analog loopback is 0 dBm0.

PRECISION VOLTAGE REFERENCE

No external components are required with the combochip to provide the voltage reference function. Voltage references are generated on-chip and are calibrated during the manufacturing process. The technique use the bandgap principle to derive a temperature and bias stable reference voltage. These references determine the gain and dynamic range characteristics of the device.

Separate references are supplied to the transmit and receive sections. Transmit and receive section are trimmed independently in the filter stages to a final precision value. With this method the combochip can achieve manufacturing tolerances of typically ±0.04 dB in absolute gain for each half chan-

Figure 5 : Simplified Block Diagram of M5914 Combship in the Analog Loopback Configuration.



nel, providing the user a significant margin for error in other board components.

CONVERSION LAWS

The M5913 and M5914 are designed to operate in both μ-law and A-law systems. The user can select either conversion law according to the voltage present on the SIG_X/ASEL pin. In each case the coder and decoder process a companded 8-bit PCM word following CCITT recommendation G.711 for μ-law and A-law conversion. If A-law operation is desired, SIG_X should be tied to V_{BB}. Thus, signaling is not allowed during A-law operation. If μ= 255-law operation is selected, then SIG_X is a TTL level input which modifies the LSB on the PCM output in signaling frames.

TRANSMIT OPERATION

TRANSMIT FILTER

The input section provides gain adjustment in the passband by means of an on-chip uncommitted operational amplifier. This operational amplifier has a common mode range of 2.17 volts, a maximum DC offset of 25 mV, a minimum voltage gain of 5000, and a unity gain bandwidth of typically 1 MHz. Gain of up to 20 dB can be set without degrading the performance of the filter. The load impedance to ground (GRDA) at the amplifier output (GS_X) must be greater than 10 kilohms in parallel with less than 50 pF. The input signal on lead VF_XI+ can be either AC or DC coupled. The input op amp can also be used in the inverting mode or differential amplifier mode (see figure 6).

A low pass anti-aliasing section is included on-chip. This section typically provides 35 dB attenuation at the sampling frequency. No external components are required to provide the necessary anti-aliasing function for the switched capacitor section of the transmit filter.

The passband section provides flatness and stopband attenuation which fulfills the AT & T D3/D4 channel bank transmission specification and CCITT recommendation G.712. The M5913 and M5914 specifications meet or exceed digital class 5 central office switching systems requirements. The transmit filter transfer characteristics and specifications will be within the limits shown in the relative table.

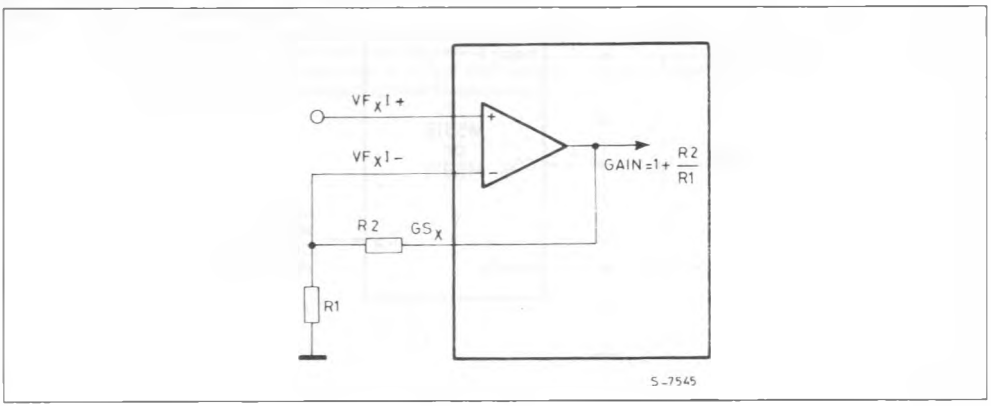
A high pass section configuration was chosen to reject low frequency noise from 50 and 60 Hz power lines, 17 Hz European electric railroads, ringing frequencies and their harmonics, and other low frequency noise. Even though there is high rejection at these frequencies, the sharpness of the band edge gives low attenuation at 200 Hz. This feature allows the use of low-cost transformer hybrids without external components.

ENCODING

The encoder internally samples the output of the transmit filter and holds each sample on an internal sample and hold capacitor. The encoder then performs an analog to digital conversion on a switched capacitor array. Digital data representing the sample is transmitted on the first eight data clock bits of the next frame.

An on-chip autozero circuit corrects for DC-offset on the input signal to encoder. This autozero circuit uses the sign bit averaging technique. In this way, all DC offset is removed from the encoder input waveform.

Figure 6 : Transmit Filter Gain Adjustment.



RECEIVE OPERATION

DECODING

The PCM word at the D_R lead is serially fetched on the first eight data clock bits of the frame. A D/A conversion is performed on the digital word and the corresponding analog sample is held on an internal sample and hold capacitor. This sample is then transferred to the receive filter.

RECEIVE FILTER

The receive section of the filter provides passband flatness and stopband rejection which fulfills both the AT & T D3/D4 specification and CCITT recommendation G.712. The filter contains the required compensation for the (sin X)/X response of such decoders. The receive filter characteristics and specifications are shown in the relative table.

RECEIVE OUTPUT POWER AMPLIFIERS

A balanced output amplifier is provided in order to allow maximum flexibility in output configuration. Either of the two outputs can be used single ended (referenced to GRDA) to drive single ended loads. Alternatively, the differential output will drive a bridged load directly. The output stage is capable of driving loads as low as 300Ω single ended to a level of 12 dBM or 600Ω differentially to a level of 15 dBM.

The receive channel transmission level may be adjusted between specified limits by manipulation of the GS_R input. GS_R is internally connected to an analog gain setting network. When GS_R is strapped to PWRO–, the receive level is maximized ; when it is tied to PWRO+, the level is minimized. The output transmission level interpolates between 0 and –12 dB as GS_R is interpolated (with potentiometer) between PWRO– and PWRO+. The use of the output gain set is illustrated in figure 7.

Transmission levels are specified relative to the receive channel output under digital milliwatt conditions, that is, when the digital input at D_R is the eight-code sequence specified in CCITT recommendation G.711.

OUTPUT GAIN SET : DESIGN CONSIDERATIONS

(refer to figure 7)

PWRO+ and PWRO– are low impedance complementary outputs. The voltages at the nodes are :

Vo+ at PWRO+

Vo at PWRO

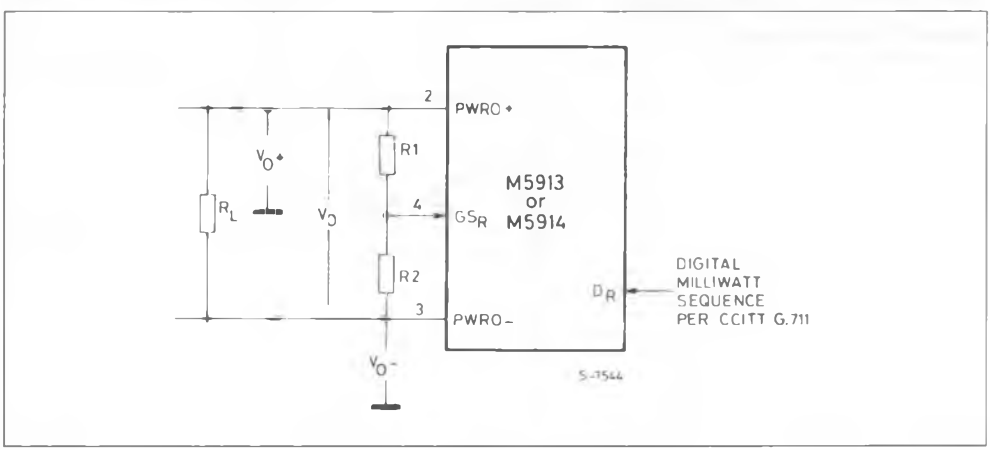
Vo = Vo+ Vo– (total differential response)

R1 and R2 are a gain setting resistor network with the center tap connected to the GS_R input. A value greater than 10 KΩ and less than 100KΩ for R1 + R2 is recommended because :

a) The parallel combination of R1 + R2 and R_L sets the total loading.

b) The total capacitance at the GS_R input and the parallel combination of R1 and R2 define a time constant which has to be minimized to avoid inaccuracies.

Figure 7 : Gain Setting Configuration.



If V_A represents the output voltage without any gain setting resistor network connected, you can have :

$$Vo = AV_A$$

where $A = \frac{1 + (R_1/R_2)}{4 + (R_1/R_2)}$

For design purposes, a useful form is R1/R2 as a function of A.

$$R1/R2 = \frac{4A - 1}{1 - A}$$

(allowable values for A are those which make R1/R2 positive)

Examples are :

If A = 1 (maximum output), then

R1/R2 = ∞ or $V(GS_R)$ = Vo ;

i.e., GS_R is tied to PWRO-

If A = 1/2, then

R1/R2 = 2

If A = 1/4 (minimum output) then

R1/R2 = 0 or $V(GS_R)$ = Vo+ ;

i.e., GS_R is tied to PWRO+

DC CHARACTERISTICS (T_{amb} = 0 °C to 70 °C, V_{CC} = + 5 ± 5 %, V_{BB} = – 5 V ± 5 %, GRDA = 0 V, unless otherwise specified) Typical values are for T_{amb} = 25 °C and nominal power supply values.

DIGITAL INTERFACE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{IL}	Low Level Input Current	GRDD ≤ V_{IN} ≤ V_{IL} (note[1])			10	µA
I_{IH}	High Level Input Current	V_{IH} ≤ V_{IN} ≤ V_{CC}			10	µA
V_{IL}	Input Low Voltage, Except CLKSEL				0.8	V
V_{IH}	Input High Voltage, Except CLKSEL		2.0			V
V_{OL}	Output Low Voltage	I_{OL} = 3.2 mA at D_X $\overline{TS_X}$ and SIG_R			0.4	V
V_{OH}	Output High Voltage	I_{OH} = 9.6 mA at D_X I_{OH} = 1.2 mA at SIG_R	2.4			V
V_{ILO}	Input Low Voltage, CLKSEL[2]		V_{BB}		V_{BB}+0.5	V
V_{IIO}	Input Intermediate Voltage, CLKSEL		GRDD – 0.5		0.5	V
V_{IHO}	Input High Voltage, CLKSEL		V_{CC}–0.5		V_{CC}	V
C_{OX}	Digital Output Capacitance[3]			5		pF
C_{IN}	Digital Input Capacitance			5	10	pF

Notes : 1. V_{IN} is the voltage on any digital pin.

2. SIG_X and $DCLK_R$ are TTL level inputs between GRDD and V_{CC} ; they are also pinstraps for mode selection when tied to V_{BB} Under these conditions V_{ILO} is the input low voltage requirement.

3. Timing parameters are guaranteed based on a 100 pF load capacitance. Up to eight digital outputs may be connected to a common PCM highway without buffering, assuming a board capacitance of 60 pF.

DC CHARACTERISTIC (continued)

POWER DISSIPATION All measurements made at f_{DCLK} = 2.048 MHz, outputs unloaded.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{CC1}	V_{CC} Operating Current			6	10	mA
I_{BB1}	V_{BB} Operating Current			6	9	mA
I_{CC0}	V_{CC} Power Down Current	PDN ≤ V_{IL} ; after 10 µs		40	300	µA
I_{BB0}	V_{BB} Power Down Current	PDN ≤ V_{IL} ; after 10 µs		40	300	µA
I_{CCS}	V_{CC} Standby Current	FS_X, FS_R ≤ V_{IL} ; after 30 ms		300	600	µA
I_{BBS}	V_{BB} Standby Current	FS_X, FS_R ≤ V_{IL} ; after 30 ms		40	300	µA
P_{D1}	Operating Power Dissipation			60	100	mW
P_{D0}	Power Down Dissipation	PDN ≤ V_{IL} ; after 10 µs		0.4	3	mW
P_{ST}	Standby Power Dissipation	FS_X, FS_R ≤ V_{IL} ; after 30 ms		1.7	5	mW

Notes : 1. V_{IN} is the voltage on any digital pin.
2. SIG_X and $DCLK_R$ are TTL level inputs between GRDD and V_{CC} ; they are also pinstraps for mode selection when tied to V_{BB}. Under these conditions V_{ILO} is the input low voltage requirement.
3. Timing parameters are guaranteed based on a 100 pF based on a 100 pF load capacitance. Up to eight digital outputs may be connected to a common PCM highway without buffering, assuming a board capacitance of 60 pF.

ANALOG INTERFACE, TRANSMIT FILTER INPUT STAGE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{BX1}	Input Leakage Current VF_XI+, VF_XI-	– 2.17 V ≤ V_{IN} ≤ 2.17 V			100	nA
R_{IXI}	Input Resistance, VF_XI+, VF_XI-		10			MΩ
V_{OSXI}	Input Offset Voltage, VF_XI+, VF_XI-				25	mV
CMRR	Common Mode Rejection, VF_XI+, VF_XI-	– 2.17 ≤ V_{IN} ≤ 2.17 V	55			dB
A_{VOL}	DC Open Loop Voltage Gain, GS_X	R_L = 10 KΩ	5000	20.000		
f_C	Open Loop Unity Gain Bandwidth, GS_X			1		MHz
V_{OXI}	Output Voltage Swing GS_X	R_L ≥ 10 kΩ	2.17		– 2.17	V
C_{LXI}	Load Capacitance, GS_X				50	pF
R_{LXI}	Minimum Load Resistance, GS_X		10			kΩ

DC CHARACTERISTIC (continued)

ANALOG INTERFACE. RECEIVE FILTER DRIVER AMPLIFIER STAGE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
R_{ORA}	Output Resistance. PWRO+. PWRO–			1		Ω
V_{OSRA}	Single Ended Output DC Offset, PWRO+, PWRO–	Relative to GRDA	– 150	75	150	mV
C_{LRA}	Load Capacitance. PWRO+. PWRO–				100	pF

AC CHARACTERISTICS - TRANSMISSION PARAMETERS

Unless otherwise noted, the analog input is a 0 dBm0, 1020 Hz sine wave[1]. Input amplifier is set for unity gain, noninverting. The digital input is a PCM bit stream generated by passing a 0 dBm0, 1020 Hz sine wave through an ideal encoder. Receive output is measured single ended. maximum gain configuration[2]. All output levels are (sin X)/X corrected.

GAIN AND DYNAMIC RANGE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
EmW	Encoder Milliwatt Response (transmit gain tolerance)	T_{amb} = 25 °C : V_{BB} = – 5 V ; V_{CC} = 5 V	– 0.15	± 0.04	0.15	dBmO
EmW_{TS}	EmW Variation with Temperature and Supplies	± 5 % Supplies. 0 to 70 °C Relative to Nominal Condition	– 0.12		0.12	dB
DmW	Digital Milliwatt Response (receive gain tolerance)	T_{amb} = 25 °C. V_{BB} = – 5 V : V_{CC} = 5 V	– 0.15	± 0.04	0.15	dBmO
DmW_{TS}	DmW Variation with Temperature and Supplies	± 5 %, 0 to 70 °C	– 0.08		0.08	dB
0 TLP_{1X}	Zero Transmission Level Point Transmit Channel (0dBm0) μ-law	600 Ω Load 900 Ω Load		2.76 1.00		dBm dBm
0 TLP_{2X}	Zero Transmission Level Point Transmit Channel (0 dBm0) A-law	600 Ω Load 900 Ω Load		2.79 1.03		dBm dBm
$0TLP_{1R}$	Zero Receive Level Point Receive Channel (0 dBm0) μ-law	600 Ω Load 900 Ω Load		5.76 4.00		dBm dBm
$0TLP_{2R}$	Zero Receive Level Point Receive Channel (0 dBm0) A-law	600 Ω Load 900 Ω Load		5.79 4.03		dBm dBm

Note : 1. 0 dBm0 is defined as the zero reference point of the channel under test (0 TLP). This corresponds to an analog signal input of 1.064 V_{rms} or an output of 1.503 V_{rms} (μ-Law) dual 1.068 V_{rms} or an output 1.516 V_{rms} (A-Law).

2. Unity gain input amplifier : GS_X is connected to VF_XI. Signal input VF_XI+ : Maximum gain output amplifier : GS_R is connected to PWRO. output to PWRO+.

AC CHARACTERISTIC (continued)

GAIN TRACKING

Reference Level = – 10 dBm0

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$GT1_X$	Transmit Gain Tracking Error Sinusoidal Input ; μ-law	3 to – 40 dBm0 – 40 to – 50 dBm0 – 50 to – 55 dBm0			± 0.2 ± 0.4 ± 1.0	dB dB dB
$GT2_X$	Transmit Gain Tracking Error Sinusoidal Input ; A-law	3 to – 40 dBm0 – 40 to – 50 dBm0 – 50 to – 55 dBm0			± 0.2 ± 0.4 ± 1.0	dB dB dB
$GT1_R$	Receive Gain Tracking Error Sinusoidal Input ; μ-law	3 to – 40 dBm0 – 40 to – 50 dBm0 – 50 to – 55 dBm0			± 0.2 ± 0.4 ± 1.0	dB dB dB
$GT2_R$	Receive Gain Tracking Error Sinusoidal Input ; A-law	3 to – 40 dBm0 – 40 to – 50 dBm0 – 50 to – 55 dBm0			± 0.2 ± 0.4 ± 1.0	dB dB dB

NOISE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
N_{XC1}	Transmit Noise, C-message Weighted	VF_XI+ = GRDA VF_XI- = GS_X		0	13	dBrnc0
N_{XC2}	Transmit Noise, C-message Weighted with Eighth Bit Signaling	VF_XI+ = GRDA VF_XI- = GS_X ; 6 th Frame Signaling		13	18	dBrnc0
N_{XP}	Transmit Noise, Psophometrically Weighted	VF_XI+ = GRDA VF_XI- = GS_X		(1)*	– 80	dBm0p
N_{RC1}	Receive Noise C-message Weighted : Quiet Code	D_R = 11111111 Measure at PWRO+		1	9	dBrnc0
N_{RC2}	Receiver Noise, C-message Weighted : Sign Bit Toggle	Input to D_R is Zero Code with Sign Bit Toggle at 1 kHz Rate		1	10	dBrnc0
N_{RP}	Receive Noise, Psophometrically Weighted	D_R = Lowest Positive Decode Level		– 90	– 81	dBm0p
N_{SF}	Single Frequency NOISE End to End Measurement	CCITT G.712.4.2			– 50	DBM0
$PSRR_1$	V_{CC} Power Supply Rejection, Transmit Channel	Idle Channel ; 200 mV P-P Signal on Supply ; 0 to 50 kHz, Measure at D_X		– 40		dB
$PSRR_2$	V_{BB} Power Supply Rejection, Transmit Channel	Idle Channel ; 200 mV P-P Signal on Supply ; 0 to 50 kHz, Measure at D_X		– 40		dB
$PSRR_3$	V_{CC} Power Supply Rejection, Receive Channel	Idle Channel ; 200 mV P-P Signal on Supply ; Measure Narrow Band at PWRO+ Single Ended, 0 to 50 kHz		– 40		dB
$PSRR_4$	V_{BB} Power Supply, Rejection Receive Channel	Idle Channel ; 200 mV P-P Signal on Supply ; Measure Narrow Band at PWRO+ Single Ended, 0 to 50 kHz		– 40		dB

(1) * Noise free : DX PCM Code stable at 01010101.

AC CHARACTERISTIC (continued)

NOISE (continued)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
CT_{TR}	Crosstalk, Transmit to Receive, Single Ended Outputs	VF_XI+ = 0 dBm0, 1.02 kHz, D_R = Lowest Positive Decode Level, Measure at PWRO+			– 80	dB
CT_{RT}	Crosstalk, Receive to Transmit, Single Ended Outputs	D_B = 0 dBm0, 1.02 kHz, VF_XI+ = GRDA, measure at D_X			– 80	dB

DISTORTION

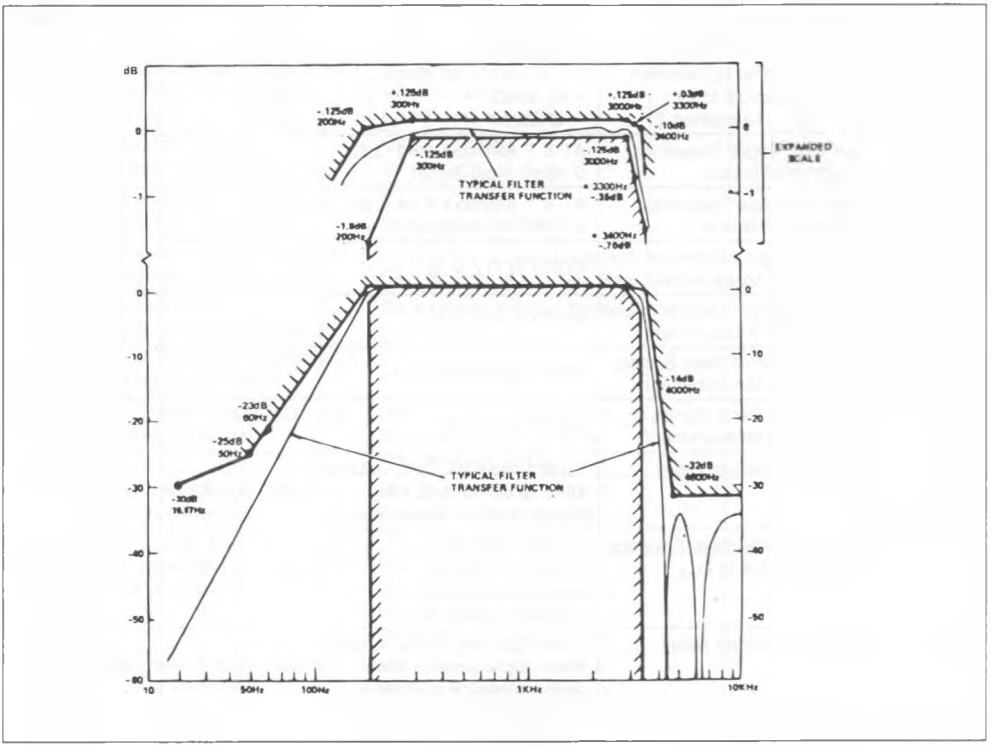
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$SD1_X$	Transmit Signal to Distortion, μ-law Sinusoidal Input ; CCITT G, 712-method 2	0 ≤ VF_XI+ ≤ – 30 dBm0 – 40 dBm0 – 45 dBm0	36 30 25			dB dB dB
$SD2_X$	Transmit Signal to Distortion, A-law Sinusoidal Input CCITT G, 712-method 2	0 ≤ VF_XI+ ≤ – 30 dBm0 – 40 dBm0 – 45 dBm0	36 30 25			dB dB dB
$SD1_R$	Transmit Signal to Distortion, μ-law Sinusoidal Input ; CCITT G, 712-method 2	0 ≤ VF_XI+ ≤ – 30 dBm0 – 40 dBm0 – 45 dBm0	36 30 25			dB dB dB
$SD2_R$	Receive Signal to Distortion, A-law Sinusoidal Input ; CCITT G, 712-method 2	0 ≤ VF_XI+ ≤ – 30 dBm0 – 40 dBm0 – 45 dBm0	36 30 25			dB dB dB
DP_{X1}	Transmit Single Frequency Distortion Products	AT & T Adivisory # 64 (3.8) 0 dBm0 Input Signal			– 46	dB
DP_{R1}	Receive Single Frequency Distortion Products	AT & T Adivisory # 64 (3.8) 0 dBm0 Input Signal			– 46	dB
IMD_1	Intermodulation Distortion, End to End Measurement	CCITT G.712 (7.1)			– 35	dB
IMD_2	Intermodulation Distortion, End to End Measurement	CCITT G.712 (7.2)			– 49	dB
SOS	Spurious out of Band Signals, End to End Measurement	CCITT G.712 (6.1)			– 30	dBm0
SIS	Spurious in Band Signals, End to End Measurement	CCITT G.712 (9)			– 40	dBm0
D_{AX}	Transmit Absolute Delay	Fixed Data Rate CLK_X = 2.048 MHz ; 0 dBm0, 1.02 kHz Signal at VF_XI+ Measure at D_X		300		μs
D_{DX}	Transmit Differential Envelope Delay Relative to D_{AX}	f = 500 – 600 Hz f = 600 – 1000 Hz f = 1000 – 2600 Hz f = 2600 – 2800 Hz		170 95 45 80		μs μs μs μs
D_{AR}	Receive Absolute Delay	Fixed data rate, CLK_R = 2.048 MHz ; digital input is DMW codes. Measure at PWRO+			190	μs
D_{DR}	Receive Differential Envelope Delay Relative to D_{AR}	f = 500 – 600 Hz f = 600 – 1000 Hz f = 1000 – 2600 Hz f = 2600 – 2800 Hz		10 10 85 110		μs μs μs μs

AC CHARACTERISTIC (continued)

TRANSMIT FILTER TRANSFER CHARACTERISTICS
Input amplifier is set for unity gain, noninverting ; maximum gain output.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
G_{RX}	Gain Relative to Gain at 1.02 kHz	0 dBm0 Signal Input at VF_{XI+}				
	16.67 Hz				– 30	dB
	50 Hz				– 25	dB
	60 Hz				– 23	dB
	200 Hz		– 1.8		– 0.125	dB
	300 to 3000 Hz		– 0.125		0.125	dB
	3300 Hz		– 0.35		0.03	dB
	3400 Hz		– 0.7		– 0.10	dB
	4000 Hz				– 14	dB
	4600 Hz and Above				– 32	dB

Figure 8 : Transmit Filter.

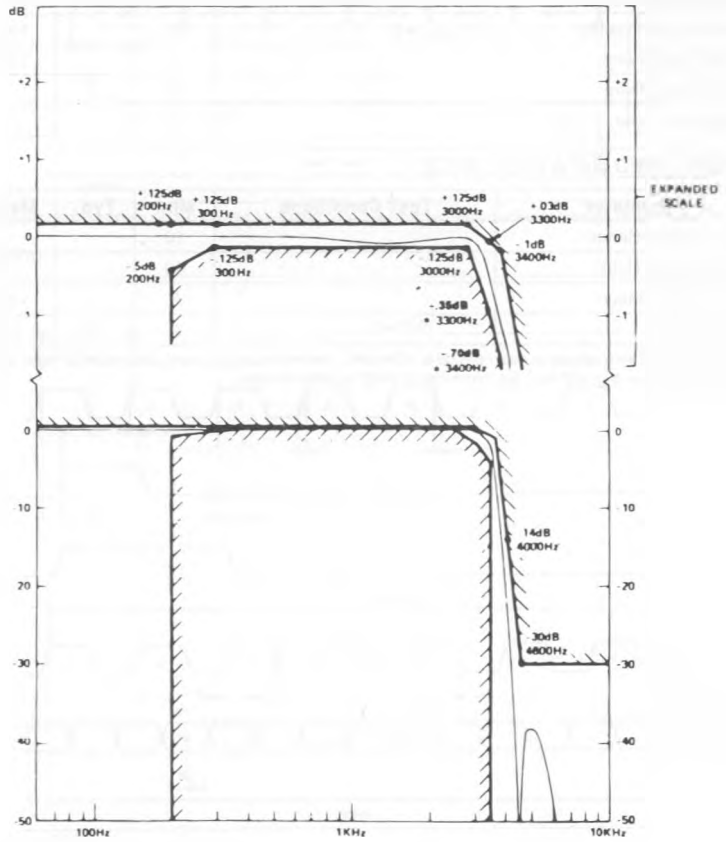


AC CHARACTERISTIC (continued)

RECEIVE FILTER TRANSFER CHARACTERISTICS

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
G_{RR}	Gain Relative to Gain at 1.02 kHz	0 dBm0 Signal Input at D_R				
	below 200 Hz				0.125	dB
	200 Hz		– 0.5		0.125	dB
	300 to 3000 Hz		– 0.125		0.125	dB
	3300 Hz		– 0.35		0.03	dB
	3400 Hz		– 0.7		– 0.1	dB
	4000 Hz				– 14	dB
	4600 Hz and Above				– 30	dB

Figure 9 : Receive Filter.



AC CHARACTERISTICS - TIMING PARAMETERS

CLOCK SECTION

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
t_{CY}	Clock Period, CLK_X, CLK_R	$f_{CLKX} = f_{CLKR} = 2.048$ MHz	488			ns
t_{CLK}	Clock Pulse Width	CLK_X, CLK_R	195			ns
t_{DCLK}	Data Clock Pulse Width[1]	64 kHz ≤ f_{DCLK} ≤ 2.048 MHz	195			ns
t_{CDC}	Clock Duty Cycle	CLK_X, CLK_R	40	50	60	%
t_r, t_f	Clock Rise and Fall Time		5		30	ns

TRANSMIT SECTION, FIXED DATA RATE MODE[2]

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
t_{DZX}	Data Enabled on TS Entry	0 < C_{LOAD} < 100 pF	0		145	ns
t_{DDX}	Data Delay from CLK_X	0 < C_{LOAD} < 100 pF	0		145	ns
t_{HZX}	Data Float on TS Exit	C_{LOAD} = 0	60		190	ns
t_{SON}	Timeslot X to Enable	0 < C_{LOAD} < 100 pF	0		145	ns
t_{SOFF}	Timeslot X to Disable	C_{LOAD} = 0	50		190	ns
t_{FSD}	Frame Sync Delay		0		120	ns
t_{SS}	Signal Setup Time		0			ns
t_{SH}	Signal Hold Time		0			ns

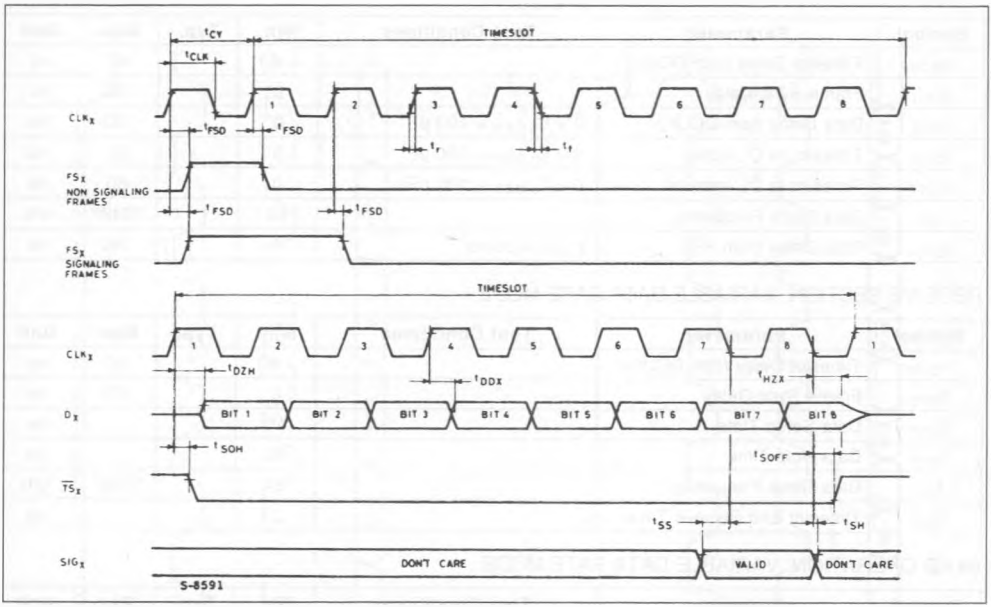
RECEIVE SECTION, FIXED DATA RATE MODE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
t_{DSR}	Receive Data Setup		10			ns
t_{DHR}	Receive Data Hold		60			ns
t_{FSD}	Frame Sync Delay		0		120	ns
t_{SIGR}	SIG_R Update		0		2	µs

Notes : 1. Devices are available wich operate at data rates up to 4.096 MHz ; the minimum data clock pulse width for these devices is 110 ns.
2. Timing parameters t_{DZX}, t_{HZX}, and t_{SOFF} are referenced to a high impedance state.

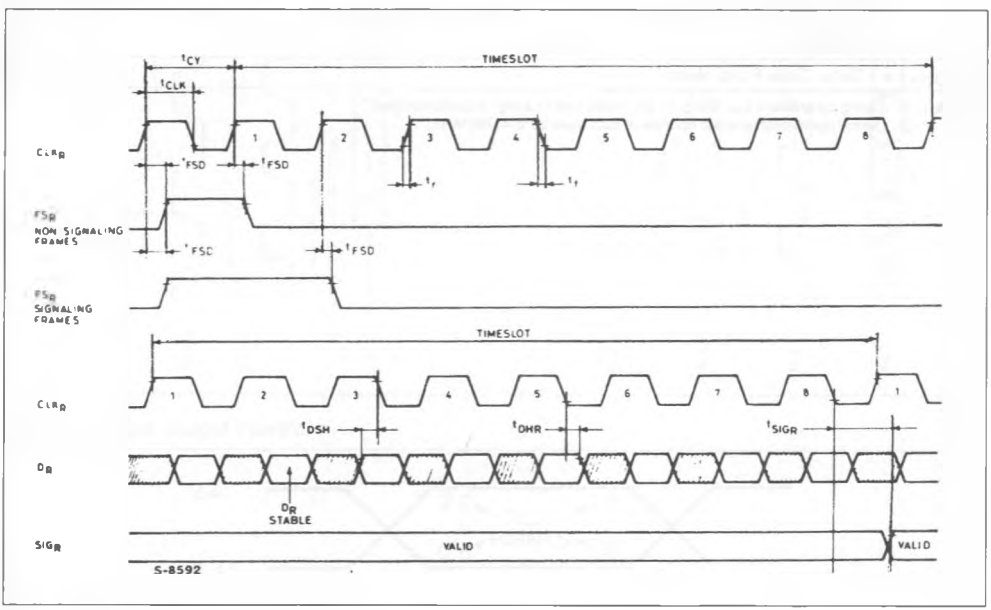
WAVEFORMS

Fixed Data Rata Timing - Transmit Timing



Note : All timing parameters referenced to V_{IH} and V_{IL} except t_{DZX}, t_{SOFF} and t_{HZX} which reference a high impedance state.

Receive Timing



Note : All timing parameters referenced to V_{IH} and V_{IL}.

AC CHARACTERISTICS (continued)

TRANSMIT SECTION, VARIABLE DATA RATE MODE[1]

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
t_{TSDX}	Timeslot Delay from $DCLK_X$		– 80		80	ns
t_{FSD}	Frame Sync Delay		0		120	ns
t_{DDX}	Data Delay from $DCLK_X$	$0 < C_{LOAD} < 100$ pF	0		100	ns
t_{DON}	Timeslot to D_X Active	$0 < C_{LOAD} < 100$ pF	0		50	ns
t_{DOFF}	Timeslot to D_X Inactive	$0 < C_{LOAD} < 100$ pF	0		80	ns
f_{DX}	Data Clock Frequency		64		2048[2]	kHz
t_{DFSX}	Data Delay from FS_X	$t_{TSDX} = 80$ ns	0		140	ns

RECEIVE SECTION, VARIABLE DATA RATE MODE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
t_{TSDR}	Timeslot Delay from $DCLK_R$		– 80		80	ns
t_{FSD}	Frame Sync Delay		0		120	ns
t_{DSR}	Data Setup Time		10			ns
t_{DHR}	Data Hold Time		60			ns
f_{DR}	Data Clock Frequency		64		2048[2]	kHz
t_{SER}	Timeslot End Receive Time		0			ns

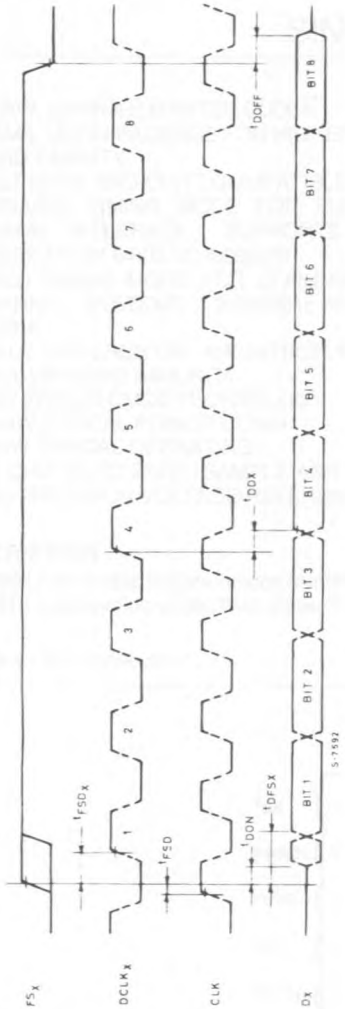
64 KB OPERATION, VARIABLE DATA RATE MODE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
t_{FSLX}	Transmit Frame Sync Minimum Downtime	FS_X is TTL high for remainder of frame	488			ns
t_{FSLR}	Receive Frame Sync Minimum Downtime	FS_R is TTL high for remainder of frame	1952			ns
t_{DCLK}	Data Clock Pulse Width				10	µs

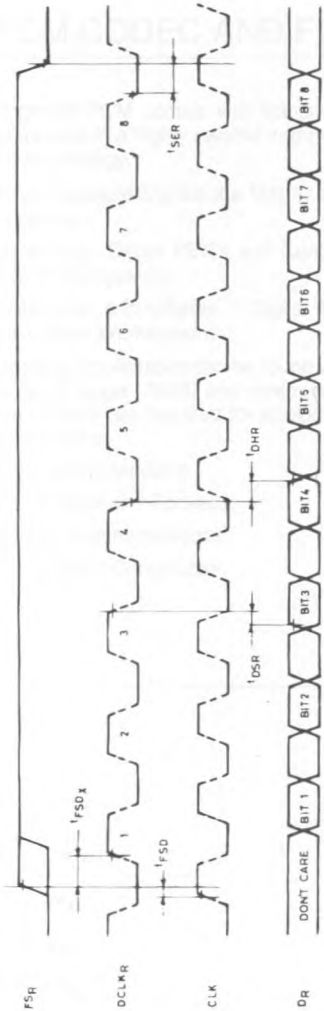
Notes : 1. Timing parameters t_{DON} and t_{DOFF} are referenced to a high impedance state.
2. Device are avalilable which operate at data rates up to 4.096 MHz.

VARIABLE DATA RATE TIMING

Transmit Timing



Receive Timing



AC Testing Input, Output Waveform.