M62358P,FP

8-BIT 12CH D-A CONVERTER WITH BUFFER AMPLIFIERS

DESCRIPTION

The M62358 is a 12-channel 8-bit voltage output digital to analog converter.

The M62358 includes data latch circuit and gain change circuit of output amplifiers.

Input data is a easy-to-use three-wires serial interface.It is able to cascading serial use with Do terminal.

Gain set up data change a case the each channel`s output voltage range is change ,and each channel`s output voltage range is able to change severally make use of gain set up data.

FEATURES

- All channel includes gain change latch circuit with output amplifiers.
- 14-bit serial data input
- Built-in reset circuit

APPLICATION

Conversion from digital control data to analog control data for home-use and industrial equipment.

Automatic adjustment by combination with EEPROM and microcomputer(replacement of conventional half-fixed resistor).

Signal gain control of DISPLAY-MONITOR or CTV.

PIN CONFIGURATION (TOP VIEW)

M62358P

Pin			Pin
LD	1	22	$\overline{R}$
CLK	2	21	VDD
DI	3	20	DO
Ao7	4	19	Ao6
Ao8	5	18	Ao5
Ao9	6	17	Ao4
Ao10	7	16	Ao3
Ao11	8	15	Ao2
Ao12	9	14	Ao1
GND	10	13	Vcc
VrefL	11	12	VrefU

Outline 22P4H

M62358FP

Pin			Pin
LD	1	24	$\overline{R}$
CLK	2	23	VDD
DI	3	22	DO
Ao7	4	21	Ao6
Ao8	5	20	Ao5
Ao9	6	19	Ao4
Ao10	7	18	Ao3
Ao11	8	17	Ao2
Ao12	9	16	Ao1
NC	10	15	NC
GND	11	14	Vcc
VrefL	12	13	VrefU

Outline 24P2-E

NC:NO CONNECTION

BLOCK DIAGRAM

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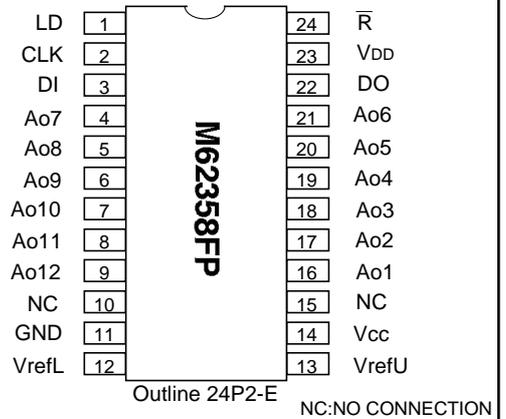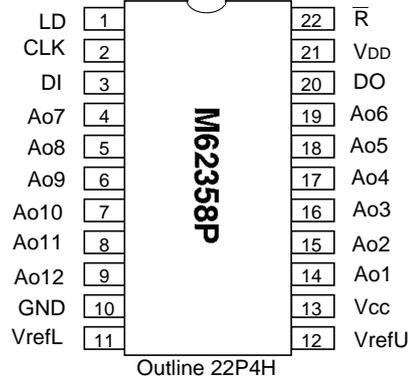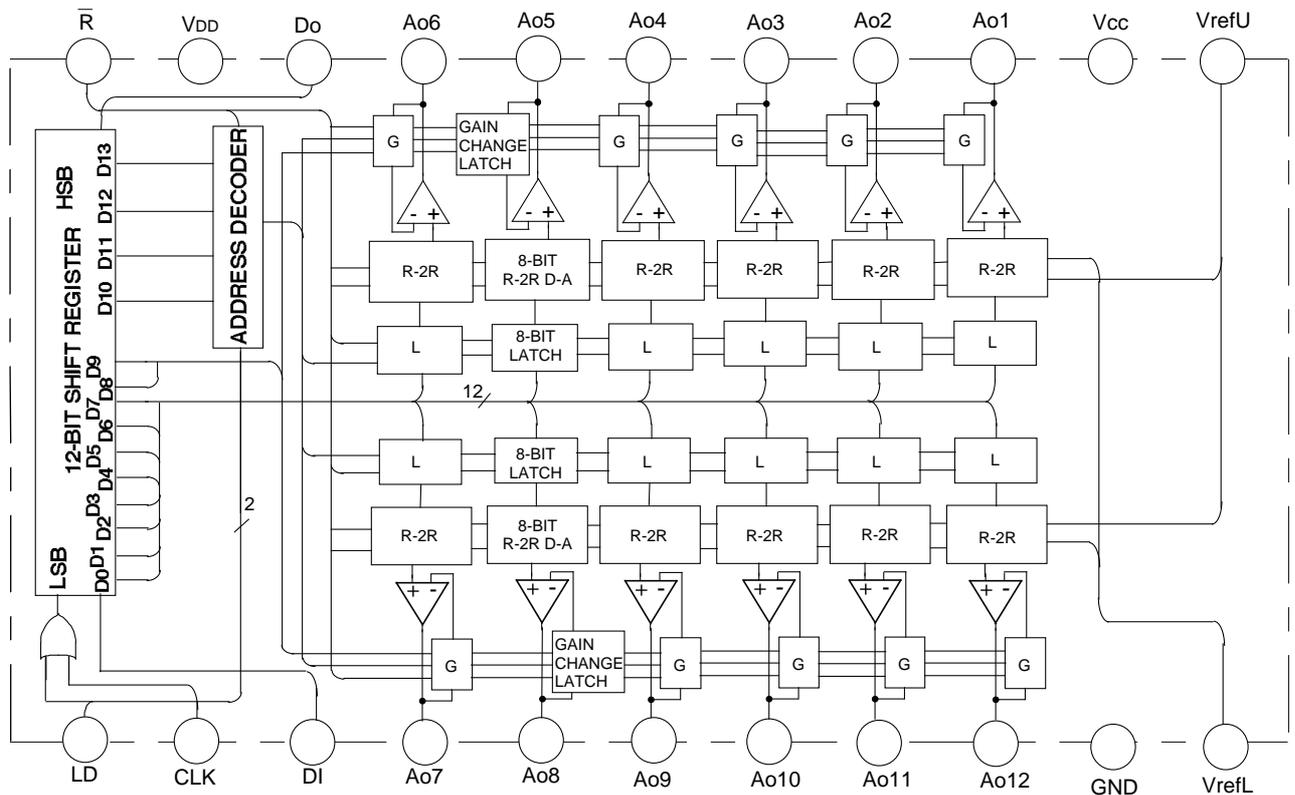
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EXPLANATION OF TERMINALS

Pin No.	Symbol	Function
③	DI	Serial data input terminal
⑳	DO	Serial data output terminal
②	CLK	Serial clock input terminal
①	LD	LD terminal input high level than latch circuit data load *1
㉑	VDD	Digital power supply terminal
⑬	Vcc	Analog power supply terminal
⑩	GND	Digital and Analog common GND
⑫	VrefU	D-A converter high level reference voltage input terminal
⑪	VrefL	D-A converter low level reference voltage input terminal
㉒	$\overline{R}$	Reset terminal
⑭	Ao1	8-bit D-A converter output terminal
⑮	Ao2	
⑯	Ao3	
⑰	Ao4	
⑱	Ao5	
⑲	Ao6	
④	Ao7	
⑤	Ao8	
⑥	Ao9	
⑦	Ao10	
⑧	Ao11	
⑨	Ao12	

*1 When the LD terminal is "H" input data has load.

ABSOLUTE MAXIMUM RATINGS(Ta=25°C, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		-0.3~13.5	V
V_{DD}	Supply voltage		-0.3~7	V
V_{refU}	D-A converter high level reference voltage		V_{DD}	V
V_{IN}	Input voltage		$-0.3 \sim V_{DD}+0.3$	V
I_{DO}	Output current		-5~+5	mA
I_{AO}	Buffer amplifier output current range		-5~+5	mA
T_{opr}	Operating temperature		-20~+85	°C
T_{stg}	Storage temperature		-40~+125	°C

RECOMMENDED OPERATING CONDITIONS

•Digital supply voltage V_{DD} 5V±10%
•Analog supply voltage Vcc V_{DD}~13V

ELECTRICAL CHARACTERISTICS

Digital part(Vcc=13V,V_{DD}=VrefU=5V, Ta=25°C,unless otherwise noted)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{DD}	Supply voltage		4.5		5.5	V
I_{DD}	Circuit current	CLK=1MHz in action			1	mA
V_{IL}	Input low voltage				$0.2V_{DD}$	V
V_{IH}	Input high voltage		$0.8V_{DD}$			V
V_{OL}	Output low voltage	I_{OL}=1.0mA			0.4	V
V_{OH}	Output high voltage	I_{OH}=-400µA	V_{DD}-0.4			V

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Analog part(V_{CC}=13V,V_{DD}=VrefU=5V,Ta=-20°C~+85°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{CC}	Supply voltage		V_{DD}		13	V
I_{CC}	Circuit current			3	6	mA
IrefU	D-A converter high level reference input current	All ch's set up at 107/256		2	4	mA
V_{refU}	D-A converter high level reference voltage range		3.5		V_{DD}	V
V_{refL}	D-A converter low level reference voltage range		0		1.5	V
V_{AO}	D-A converter output voltage range	I_{AO} =±500µA	0.1		Vcc-0.1	V
		I_{AO} =±1mA	0.2		Vcc-0.2	
I_{AO}	Buffer amplifier output current range				±2.5	mA
DNL	Differential nonlinearity	Guaranteed monotonic	-1.0		1.0	LSB
NL	Nonrineality		-1.5		1.5	LSB
EZ	Zero code error	VrefU=4.79V	-2		2	LSB
EF	Full scale error	VrefL=0.95V without load	-2		2	LSB
Eo	Gain error		-3		3	%
SR	Output slew rate			0.2		V/µs

TIMING CHART (MODEL)
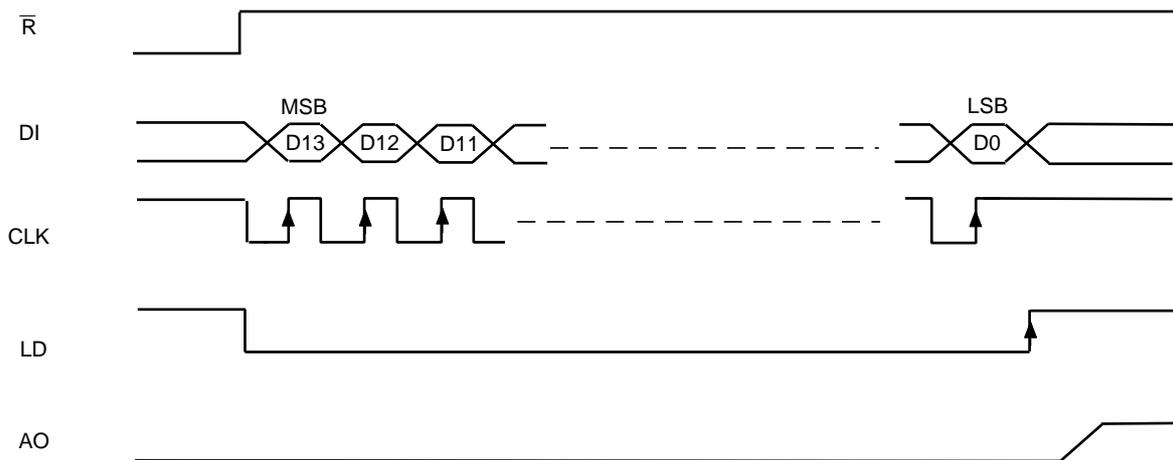
Input data is carried out LD signal Low besides CLK signal positive edge.
CLK,LD is keep generally High level.

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8-BIT 12CH D-A CONVERTER WITH BUFFER AMPLIFIERS

AC CHARACTERISTICS(Ta=-20~85°C,V_{CC}=13V,V_{DD}=VrefU=5V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits Min	Limits Typ	Limits Max	Unit
t_{CKL}	Clock "L"pulse width		200			ns
t_{CKH}	Clock "H"pulse width		200			ns
t_{CR}	Clock rise time				200	ns
t_{CF}	Clock fall time				200	ns
t_{DCH}	Data set up time		60			ns
t_{CHD}	Data hold time		100			ns
t_{CHL}	LD setup time		200			ns
t_{LDC}	LD hold time		100			ns
t_{LDH}	LD "H" pulse width		100			ns
t_{DO}	Data output delay time	C_L=100pF	70		350	ns
t_{LDD}	D-A output setting time	Without load			300	µs

TIMING CHART
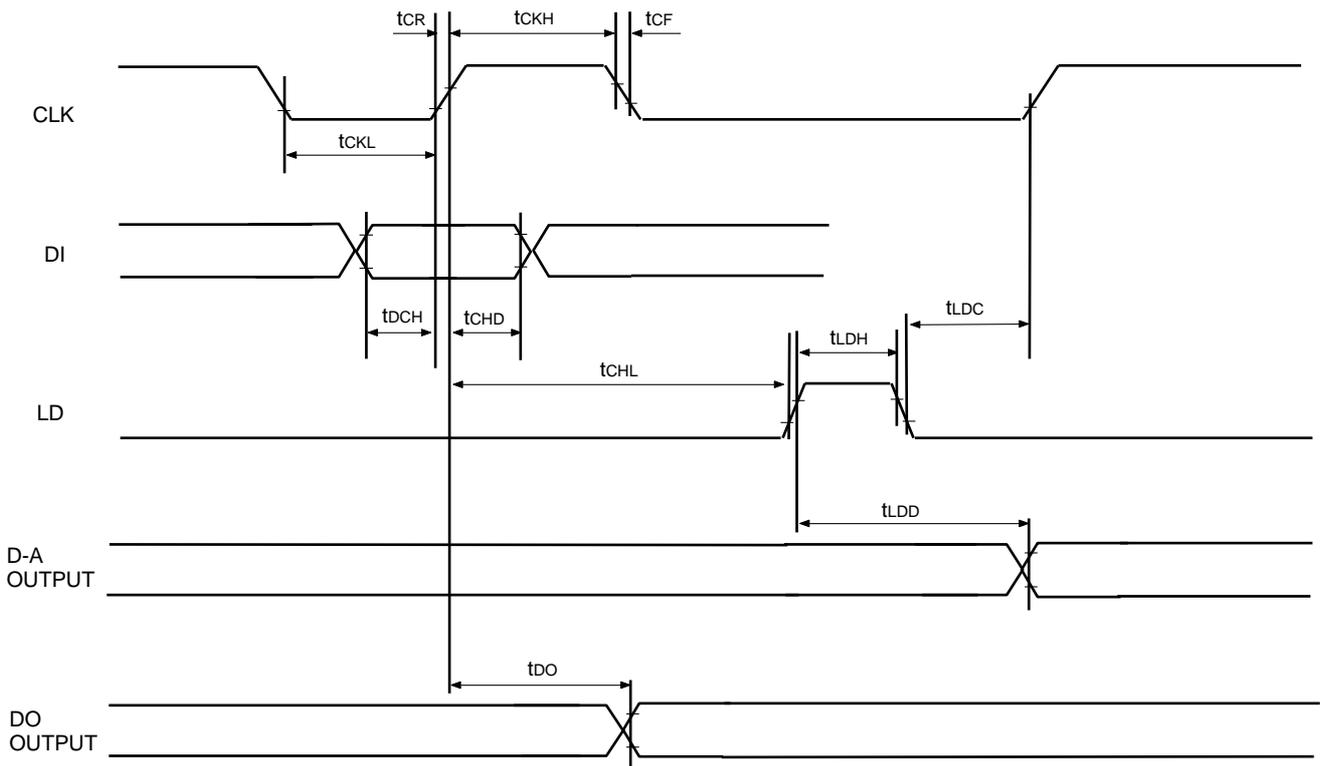
8-BIT 12CH D-A CONVERTER WITH BUFFER AMPLIFIERS

DIGITAL FORMAT

•14 bit serial data

•Data assignment

| D10 | D11 | D12 | D13 | :DAC select data |

| D8 | D9 | :GAIN set up data |

| D0 | D1 | D2 | D3 | D4 | D5 | D6 | D7 | :DAC set up data |
(LSB) (MSB)
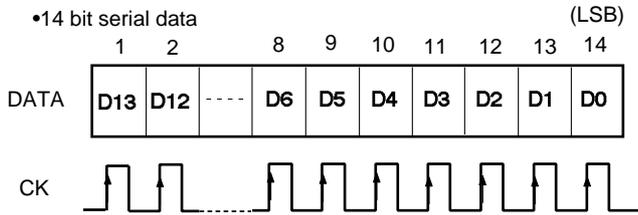
•DAC select data

D10	D11	D12	D13	DAC selection
0	0	0	0	Don't care
0	0	0	1	Ao1 selection
0	0	1	0	Ao2 selection
0	0	1	1	Ao3 selection
0	1	0	0	Ao4 selection
0	1	0	1	Ao5 selection
0	1	1	0	Ao6 selection
0	1	1	1	Ao7 selection
1	0	0	0	Ao8 selection
1	0	0	1	Ao9 selection
1	0	1	0	Ao10 selection
1	0	1	1	Ao11 selection
1	1	0	0	Ao12 selection
1	1	0	1	Don't care
1	1	1	0	Don't care
1	1	1	1	Don't care
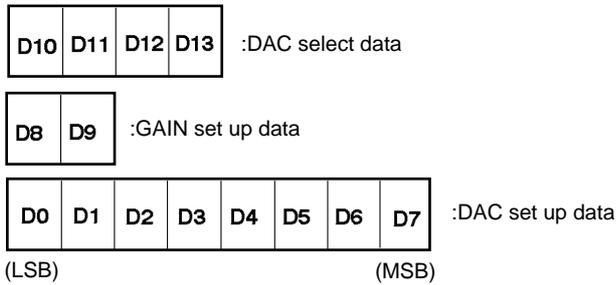
•GAIN set up data

D8	D9	K	DAC output range (VrefU=5V,VrefL=0V)
0	0	1	0~5V
1	0	1.6	0~8V
0	1	1.8	0~9V
1	1	2.4	0~12V

•DAC set up data

(LSB) (MSB)

| D0	D2	D3	D4	D5	D6	D7	DAC voltage
0	0	0	0	0	0	0	$1/256 \cdot (VrefU-VrefL) \cdot K + VrefL$
1	0	0	0	0	0	0	$2/256 \cdot (VrefU-VrefL) \cdot K + VrefL$
0	0	0	0	0	0	0	$3/256 \cdot (VrefU-VrefL) \cdot K + VrefL$
1	0	0	0	0	0	0	$4/256 \cdot (VrefU-VrefL) \cdot K + VrefL$
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
0	1	1	1	1	1	1	$255/256 \cdot (VrefU-VrefL) \cdot K + VrefL$
1	1	1	1	1	1	1	$256/256 \cdot (VrefU-VrefL) \cdot K + VrefL$

$$Ao = \frac{2^0 \times D0 + 2^1 \times D1 + 2^2 \times D2 + \cdots\cdots + 2^6 \times D6 + 2^7 \times D7 + 1}{256} \cdot (VrefU - VrefL) \cdot K + VrefL$$

K:Amplifiers gain

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APPLICATION CIRCUIT
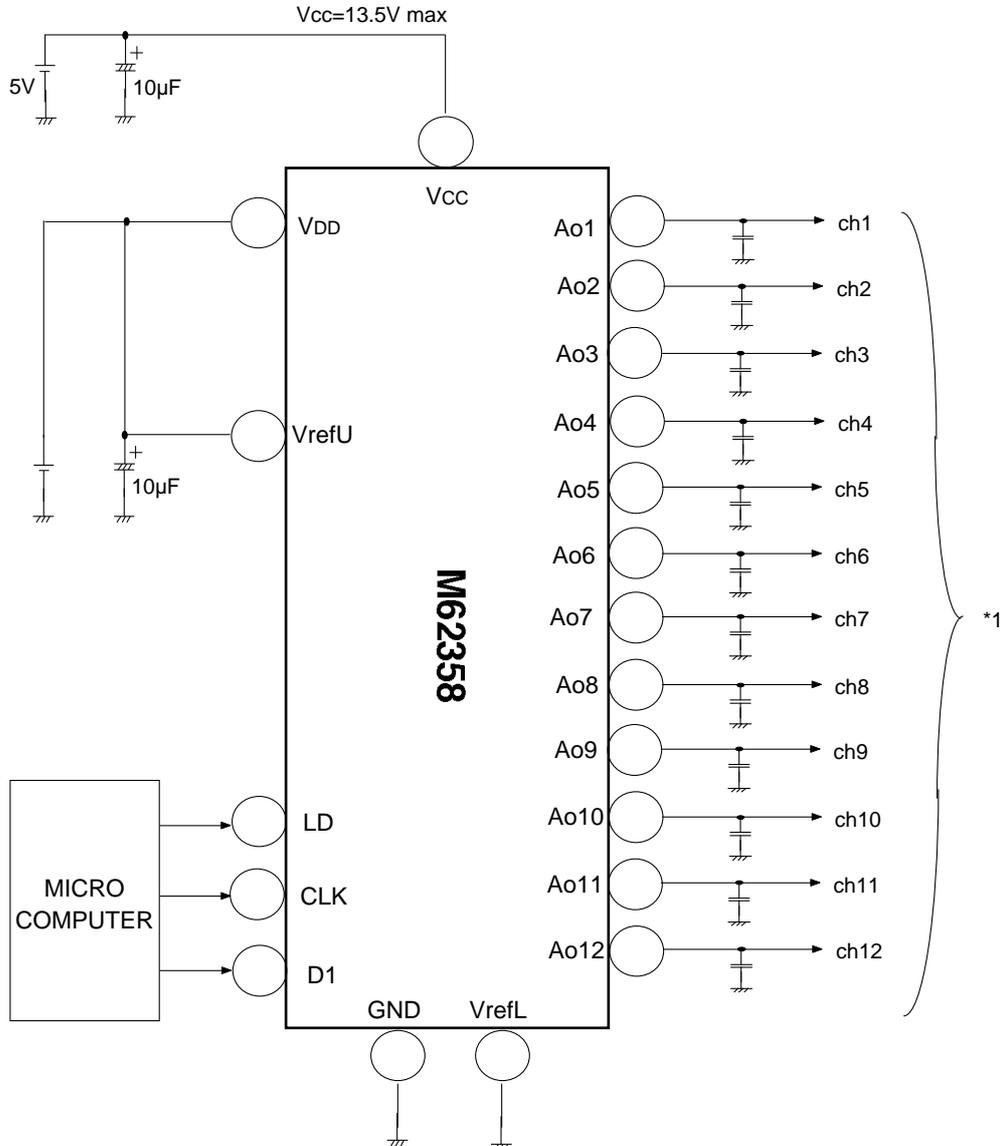
This IC`s output amplifier has an advantage to capacitive load.So it`s no problem at device action when connect capacitor among output to GND for every noise eliminate.

*1 If be used in a cathode-ray tube sets and high voltage sets,please connect capacitor among output to GND,about 0.1μF~1μF,because keep off effect of spark and electric discharge etc.

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