
Features

- Operating Voltage: 5V
- Access Time: 30, 45 ns
- Very Low Power Consumption
 - Active: 250 mW (Typ)
 - Standby: 1 μ W (Typ)
 - Data Retention: 0.5 μ W (Typ)
- Wide Temperature Range: -55°C to +125°C
- 400 Mils Width Package
- TTL Compatible inputs and Outputs
- Asynchronous
- Single 5V Supply
- Equal Cycle and Access Time
- Gated Inputs:
 - No Pull-up/down
 - Resistors Are Required
- QML Q and V with SMD 5962-89598

Description

The M65608E is a very low power CMOS static RAM organized as 131072 x 8 bits.

Atmel brings the solution to applications where fast computing is as mandatory as low consumption, such as aerospace electronics, portable instruments, or embarked systems.

Utilizing an array of six transistors (6T) memory cells, the M65608E combines an extremely low standby supply current (Typical value = 0.2 μ A) with a fast access time at 30 ns over the full military temperature range. The high stability of the 6T cell provides excellent protection against soft errors due to noise.

The M65608E is processed according to the methods of the latest revision of the MIL STD 883 (class B or S), ESA SCC 9000 or QML.



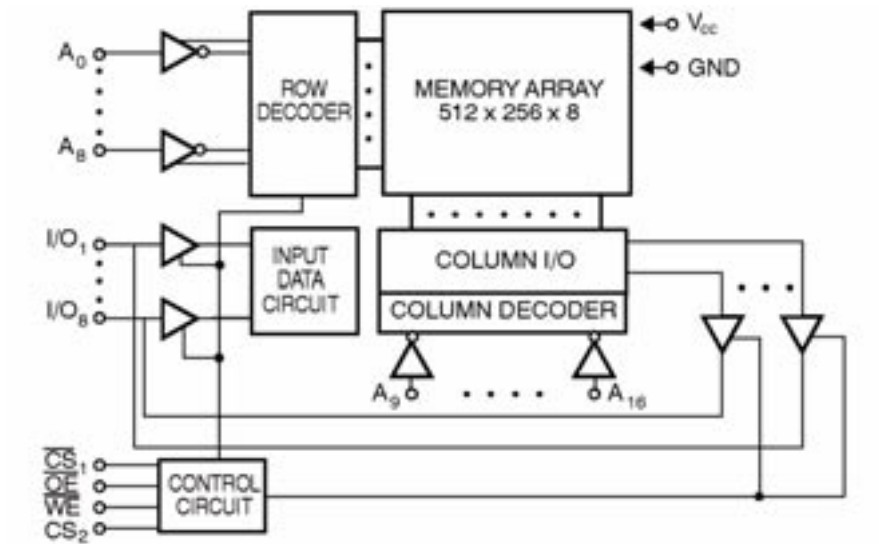
**Rad. Tolerant
128K x 8
Very Low Power
5V CMOS SRAM**

M65608E

Rev. 4151G-AERO-06/02

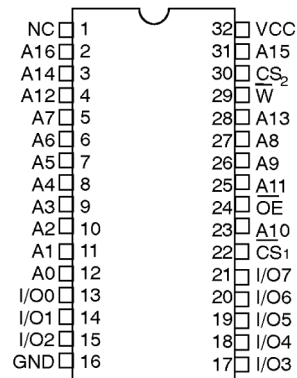


Block Diagram



Pin Configuration

32-lead DIL side-brazed 400 MILS
 32-lead Flatpack 400 MILS



Pin Description

Table 1. Pin Names

Names	Description
A0 - A16	Address inputs
I/O0 - I/O7	Data Input/Output
$\overline{\text{CS1}}$	Chip select 1
CS2	Chip select 2
$\overline{\text{WE}}$	Write Enable
$\overline{\text{OE}}$	Output Enable
VCC	Power
GND	Ground

Table 2. Truth Table

$\overline{\text{CS1}}$	CS2	$\overline{\text{W}}$	$\overline{\text{OE}}$	Inputs/ Outputs	Mode
H	X	X	X	Z	Deselect/ Power-down
X	L	X	X	Z	Deselect/ power-down
L	H	H	L	Data Out	Read
L	H	L	X	Data In	Write
L	H	H	H	Z	Output Disable

Note: L = low, H = high, X = H or L, Z = high impedance.



Electrical Characteristics

Absolute Maximum Ratings

Supply voltage to GND potential:.....-0.5V + 7.0V	*NOTE: Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
DC input voltage:GND - 0.5V to VCC + 0.5	
DC output voltage high Z state:GND - 0.5V to VCC + 0.5	
Storage temperature: -65°C to +150°C	
Output current into outputs (low): 20 mA	
Electro statics discharge voltage: > 2001V (MIL STD 883D method 3015.3)	

Military Operating Range

Operating Voltage	Operating Temperature
5V \pm 10%	-55°C to + 125°C

Recommended DC Operating Conditions

Parameter	Description	Minimum	Typical	Maximum	Unit
V _{CC}	Supply voltage	4.5	5.0	5.5	V
GND	Ground	0.0	0.0	0.0	V
V _{IL}	Input low voltage	GND - 0.5	0.0	0.8	V
V _{IH}	Input high voltage	2.2	–	VCC + 0.5	V

Capacitance

Parameter	Description	Minimum	Typical	Maximum	Unit
C _{in} ⁽¹⁾	Input low voltage	–	–	8	pF
C _{out} ⁽¹⁾	Output high voltage	–	–	8	pF

Note: 1. Guaranteed but not tested.

DC Parameters

DC Test Conditions

Table 3. DC Test Conditions

TA = -55°C to + 125°C; Vss = 0V; V_{CC} = 4.5V to 5.5V

Symbol	Description	Minimum	Typical	Maximum	Unit
IIX ⁽¹⁾	Input leakage current	-1	-	1	μA
IOZ ⁽¹⁾	Output leakage current	-1	-	1	μA
VOL ⁽²⁾	Output low voltage	-	-	0.4	V
VOH ⁽³⁾	Output high voltage	2.4	-	-	V

1. GND < V_{in} < V_{CC}, GND < V_{out} < V_{CC} Output Disabled.
2. V_{CC} min. IOL = 8 mA.
3. V_{CC} min. IOH = -0.4 mA.

Consumption

Symbol	Description	65608E-30	65608E-45	Unit	Value
ICCSB ⁽¹⁾	Standby supply current	2	2	mA	max
ICCSB1 ⁽²⁾	Standby supply current	300	300	μA	max
ICCOP ⁽³⁾	Dynamic operating current	130	100	mA	max

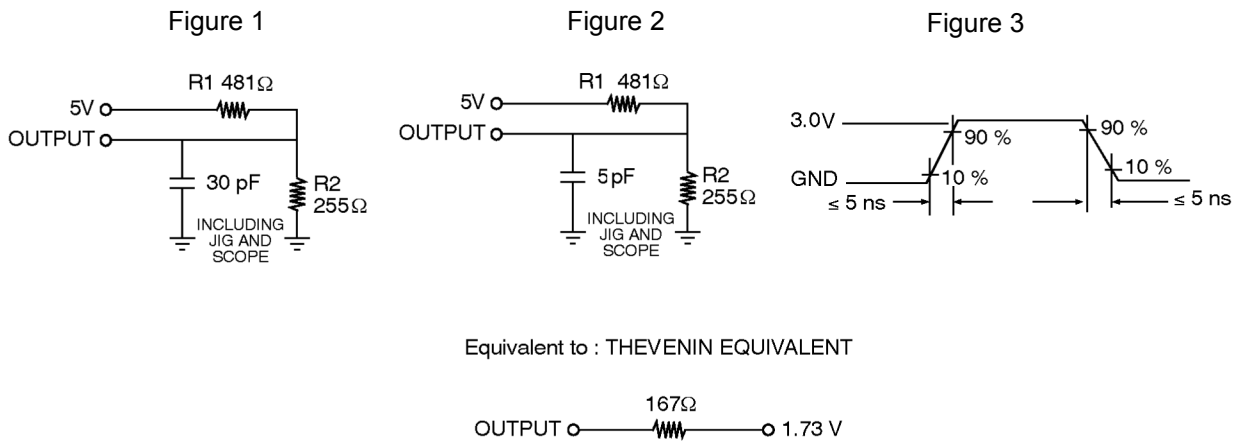
1. CS1 > V_{IH} or CS2 < V_{IL} and CS1 < V_{IL}.
2. CS1 > V_{CC} - 0.3V or, CS2 < GND + 0.3V and CS1 < 0.2V.
3. F = 1/TAVAV, I_{out} = 0 mA, W = OE = V_{IH}, V_{in} = GND or V_{CC}, V_{CC} max.

AC Parameters

AC Test Conditions

Input Pulse Levels:GND to 3.0V
 Input Rise/Fall Times:5 ns
 Input Timing Reference Levels:1.5V
 Output loading IOL/IOH (see Figure 1 and Figure 2)+30 pF

AC Test Loads Waveforms

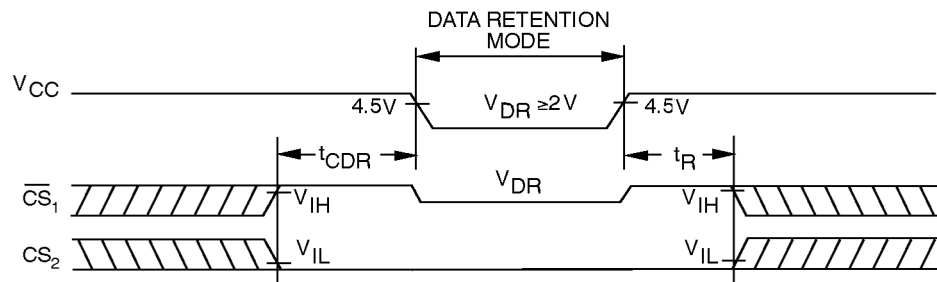


Data Retention Mode

Atmel CMOS RAM's are designed with battery backup in mind. Data retention voltage and supply current are guaranteed over temperature. The following rules ensure data retention:

1. During data retention chip select $\overline{CS1}$ must be held high within VCC to VCC - 0.2V or, chip select CS2 must be held down within GND to GND +0.2V.
2. Output Enable (\overline{OE}) should be held high to keep the RAM outputs high impedance, minimizing power dissipation.
3. During power up and power-down transitions $\overline{CS1}$ and \overline{OE} must be kept between VCC + 0.3V and 70% of VCC, or with CS2 between GND and GND -0.3V.
4. The RAM can begin operation > TR ns after VCC reaches the minimum operation voltages (4.5V).

Timing



Data Retention Characteristics

Parameter	Description	Minimum	Typical TA = 25 °C	Maximum	Unit
VCCDR	V _{CC} for data retention	2.0	–	–	V
TCDR	Chip deselect to data retention time	0.0	–	–	ns
TR	Operation recovery time	TAVAV ⁽¹⁾	–	–	ns
ICCDR1 ⁽²⁾	Data retention current at 2.0V	–	0.1	150	μA
ICCDR2 ⁽²⁾	Data retention current at 3.0V	–	0.2	200	μA

Notes: 1. TAVAV = Read Cycle Time
 2. CS1 = V_{CC} or CS2 = CS1 = GND, Vin = GND/V_{CC}, this parameter is only tested at V_{CC} = 2V.

Write Cycle

Symbol	Parameter	65608-30	65608-45	Unit	Value
TAVAV	Write cycle time	30	45	ns	min
TAVWL	Address set-up time	0	0	ns	min
TAVWH	Address valid to end of write	22	35	ns	min
TDVWH	Data set-up time	18	20	ns	min
TE1LWH	CS1 low to write end	22	35	ns	min
TE2HWH	CS2 high to write end	22	35	ns	min
TWLQZ	Write low to high Z ⁽¹⁾	8	15	ns	max
TWLWH	Write pulse width	22	35	ns	min
TWHAX	Address hold from to end of write	0	0	ns	min
TWHDX	Data hold time	0	0	ns	min
TWHQX	Write high to low Z ⁽¹⁾	0	0	ns	min

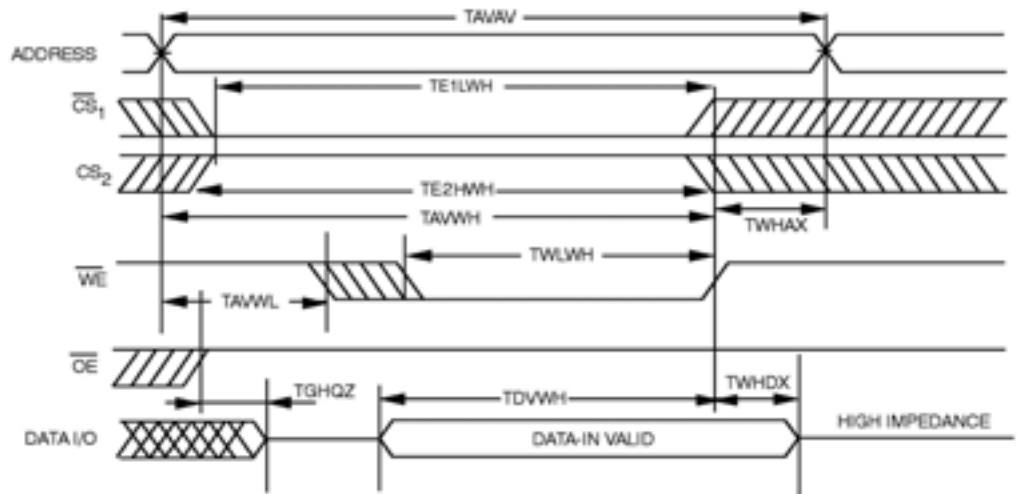
Note: 1. Parameters guaranteed, not tested, with output loading 5 pF.

Read Cycle

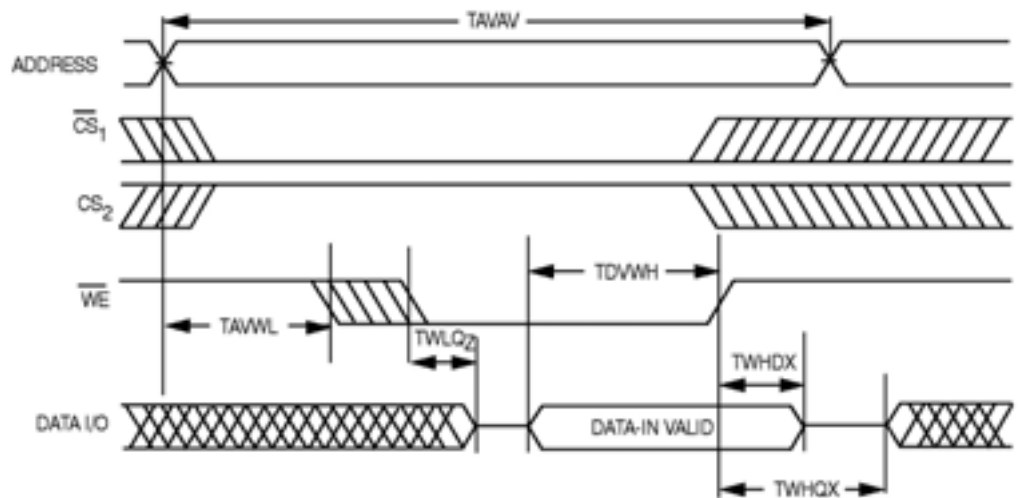
Symbol	Parameter	65608-30	65608-45	Unit	Value
TAVAV	Read cycle time	30	45	ns	min
TAVQV	Address access time	30	45	ns	max
TAVQX	Address valid to low Z ⁽¹⁾	5	5	ns	min
TE1LQV	Chip-select1 access time	30	45	ns	max
TE1LQX	CS1 low to low Z ⁽¹⁾	3	3	ns	min
TE1HQZ	CS1 high to high Z ⁽¹⁾	15	20	ns	max
TE2HQV	Chip-select2 access time	30	45	ns	max
TE2HQX	CS2 high to low Z ⁽¹⁾	3	3	ns	min
TE2LQZ	CS2 low to high Z ⁽¹⁾	18	20	ns	max
TGLQV	Output Enable access time	12	15	ns	max
TGLQX	OE low to low Z ⁽¹⁾	0	0	ns	min
TGHQZ	OE high to high Z ⁽¹⁾	8	15	ns	max

Note: 1. Parameters Guaranteed, not tested, with output loading 5 pF.

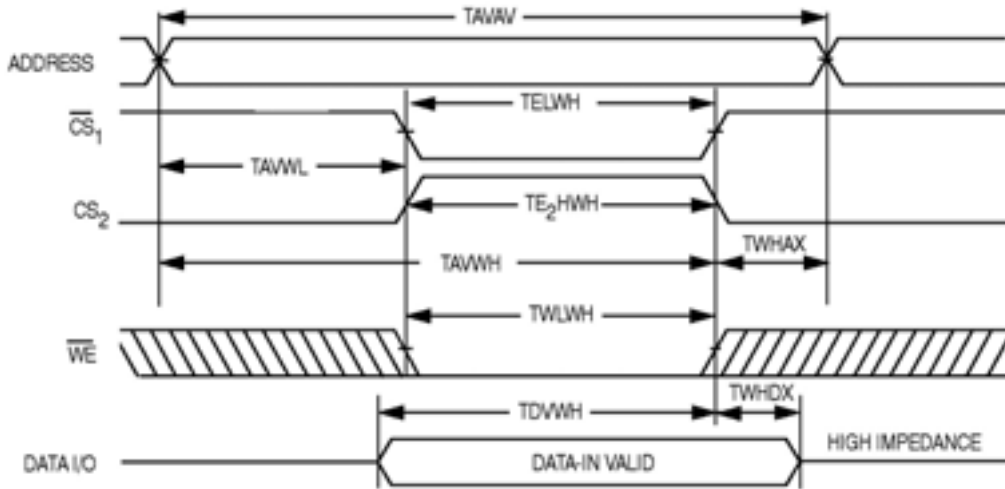
Write Cycle 1 \overline{WE} Controlled, OE High During Write



Write Cycle 2 \overline{WE} Controlled, OE Low

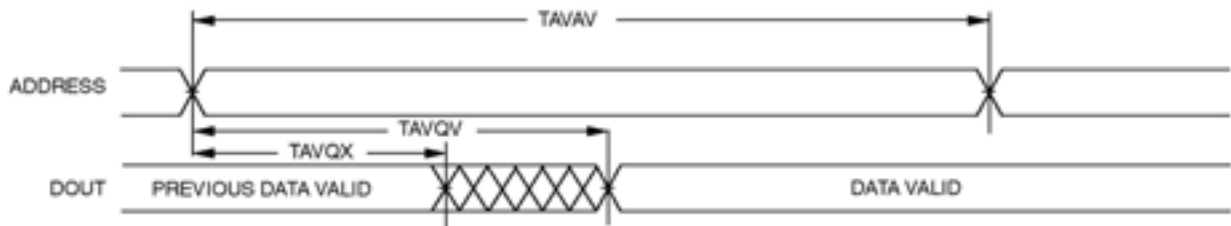


**Write Cycle 3 $\overline{CS1}$ or $CS2$,
Controlled**

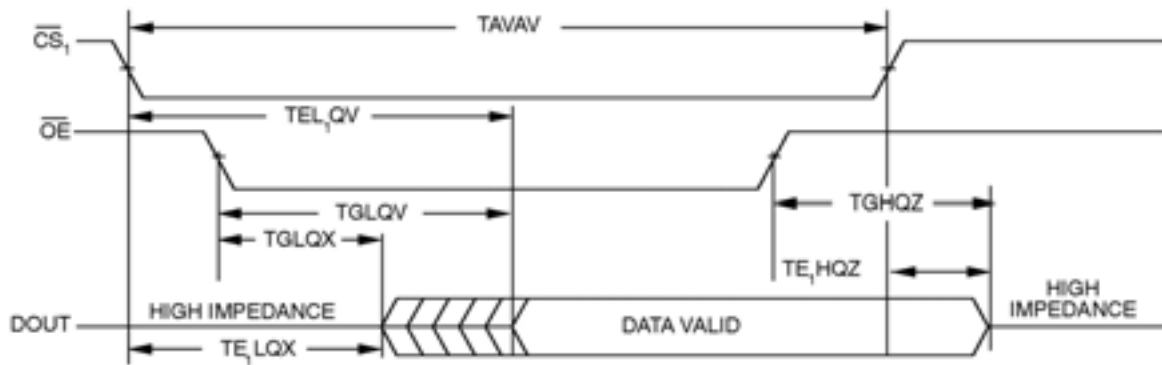


Note: The internal write time of the memory is defined by the overlap of $\overline{CS1}$ Low and $CS2$ HIGH and \overline{W} LOW. Both signals must be activated to initiate a write and either signal can terminate a write by going in activated. The data input setup and hold timing should be referenced to the activated edge of the signal that terminates the write. Data out is high impedance if $\overline{OE} = V_{IH}$.

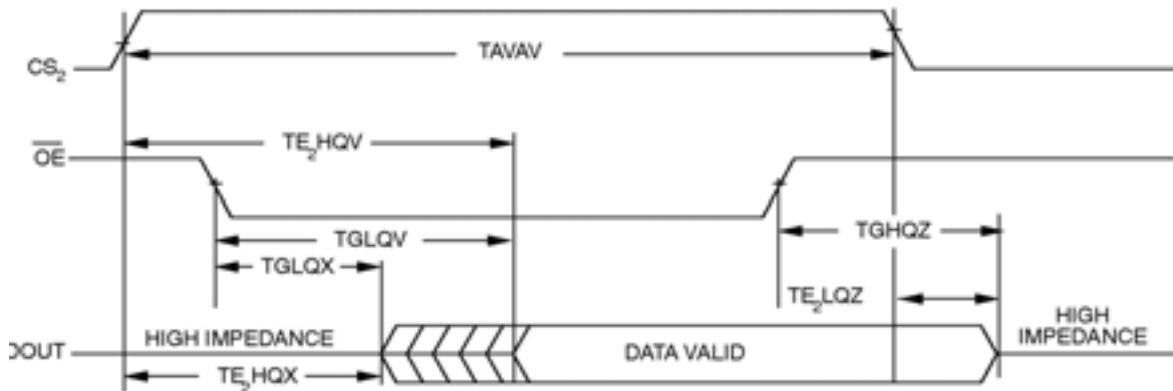
Read Cycle 1



Read Cycle 2



Read Cycle 3





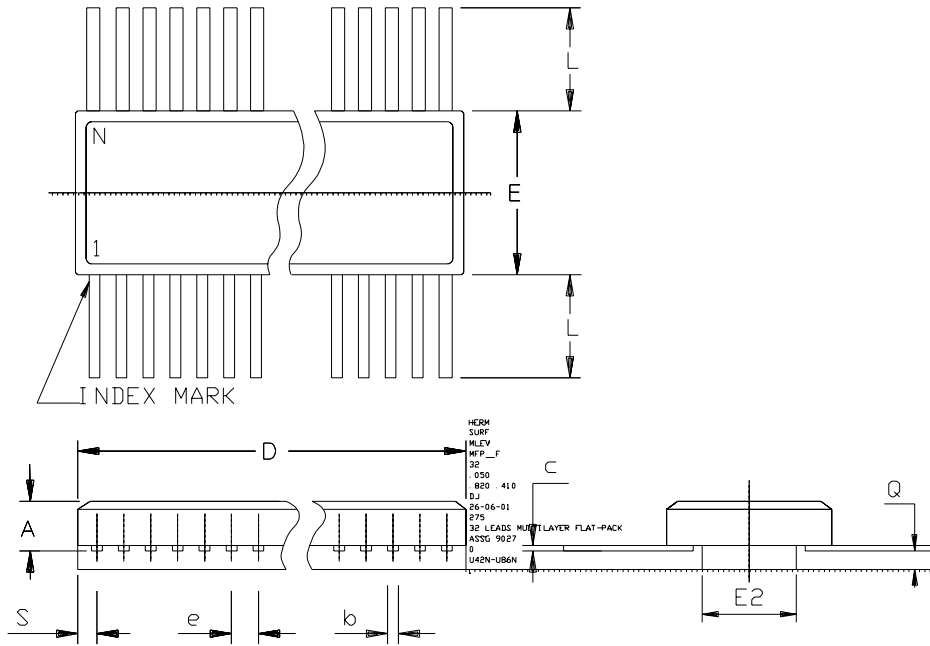
Ordering Information

Part Number	Temperature Range	Speed	Package	Flow
MMDJ-65608EV-30	-55° to +125°C	30 ns	FP32.4	Standard Mil
MMDJ-65608EV-45	-55° to +125°C	45 ns	FP32.4	Standard Mil
MMC9-65608EV-30	-55° to +125°C	30 ns	SB32.4	Standard Mil
MMC9-65608EV-45	-55° to +125°C	45 ns	SB32.4	Standard Mil
SMDJ-65608EV-30SB	-55° to +125°C	30 ns	FP32.4	SCC B
SMDJ-65608EV-45SB	-55° to +125°C	45 ns	FP32.4	SCC B
SMC9-65608EV-30SB	-55° to +125°C	30 ns	SB32.4	SCC B
SMC9-65608EV-45SB	-55° to +125°C	45 ns	SB32.4	SCC B
5962-8959847QTC	-55° to +125°C	30 ns	FP32.4	QML Q
5962-8959818MTC	-55° to +125°C	45 ns	FP32.4	QML Q
5962-8959847QZC	-55° to +125°C	30 ns	SB32.4	QML Q
5962-8959818MZC	-55° to +125°C	45 ns	SB32.4	QML Q
5962-8959847VTC	-55° to +125°C	30 ns	FP32.4	QML V
5962-8959818VTC	-55° to +125°C	45 ns	FP32.4	QML V
5962-8959847VZC	-55° to +125°C	30 ns	SB32.4	QML V
5962-8959818VZC	-55° to +125°C	45 ns	SB32.4	QML V
MMDJ-65608EV-30-E	25°C	30 ns	FP32.4	Engineering Samples
MMC9-65608EV-30-E ⁽¹⁾	25°C	30 ns	SB32.4	Engineering Samples
MM0-65608EV-30-E	25°C	30 ns	Die	Engineering Samples
5962-895647Q6A	-55° to +125°C	30 ns	Die	QML Q
5962-895647V6A	-55° to +125°C	30 ns	Die	QML V

Note: 1. Contact Atmel for availability.

Package Drawings

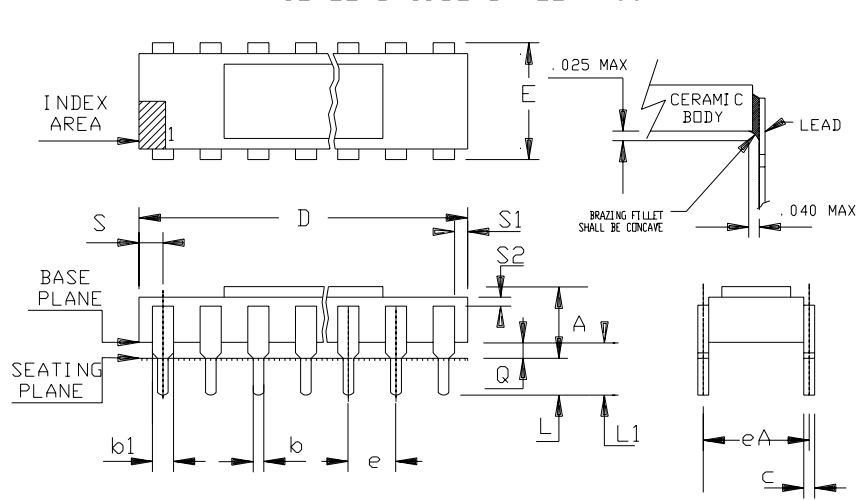
32-lead Flat Pack 400 Mils



	MM		INCH	
	Min	Max	Min	Max
A	1.78	2.72	.070	.107
b	0.38	0.48	.015	.019
c	0.076	0.15	.003	.007
D	20.62	21.03	.812	.828
E	10.26	10.57	.404	.416
E2	6.96	7.26	.274	.286
e	1.27 BSC		.050 BSC	
L	7.37	7.87	.290	.310
Q	0.51	0.76	.020	.030
S	---	1.14	---	.045
N	32		32	

Package Drawings

32-lead Side Braze 400 Mils



	MM		INCH	
	A	2.92	4.32	.115
b	0.40	0.51	.016	.020
b1	1.27 TYP		0.05 TYP	
c	0.23	0.30	.009	.012
D	40.13	41.15	1.580	1.620
E	10.16	10.67	.400	.420
eA	9.90	10.41	.390	.410
e	2.54	BSC	.100	BSC
L	3.43	4.20	.135	.165
L1	4.44	5.72	.175	.225
Q	1.02	1.52	.040	.060
S	-	1.65	-	.065
S1	0.13	-	.005	-
S2	0.13	-	.005	-



Atmel Headquarters

Corporate Headquarters

2325 Orchard Parkway
San Jose, CA 95131
TEL 1(408) 441-0311
FAX 1(408) 487-2600

Europe

Atmel Sarl
Route des Arsenaux 41
Case Postale 80
CH-1705 Fribourg
Switzerland
TEL (41) 26-426-5555
FAX (41) 26-426-5500

Asia

Room 1219
Chinachem Golden Plaza
77 Mody Road Tsimhatsui
East Kowloon
Hong Kong
TEL (852) 2721-9778
FAX (852) 2722-1369

Japan

9F, Tonetsu Shinkawa Bldg.
1-24-8 Shinkawa
Chuo-ku, Tokyo 104-0033
Japan
TEL (81) 3-3523-3551
FAX (81) 3-3523-7581

Atmel Operations

Memory

2325 Orchard Parkway
San Jose, CA 95131
TEL 1(408) 441-0311
FAX 1(408) 436-4314

Microcontrollers

2325 Orchard Parkway
San Jose, CA 95131
TEL 1(408) 441-0311
FAX 1(408) 436-4314

La Chantrerie
BP 70602
44306 Nantes Cedex 3, France
TEL (33) 2-40-18-18-18
FAX (33) 2-40-18-19-60

ASIC/ASSP/Smart Cards

Zone Industrielle
13106 Rousset Cedex, France
TEL (33) 4-42-53-60-00
FAX (33) 4-42-53-60-01

1150 East Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906
TEL 1(719) 576-3300
FAX 1(719) 540-1759

Scottish Enterprise Technology Park
Maxwell Building
East Kilbride G75 0QR, Scotland
TEL (44) 1355-803-000
FAX (44) 1355-242-743

RF/Automotive

Theresienstrasse 2
Postfach 3535
74025 Heilbronn, Germany
TEL (49) 71-31-67-0
FAX (49) 71-31-67-2340

1150 East Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906
TEL 1(719) 576-3300
FAX 1(719) 540-1759

Biometrics/Imaging/Hi-Rel MPU/ High Speed Converters/RF Data- com

Avenue de Rochepleine
BP 123
38521 Saint-Egreve Cedex, France
TEL (33) 4-76-58-30-00
FAX (33) 4-76-58-34-80

e-mail

literature@atmel.com

Web Site

<http://www.atmel.com>

© Atmel Corporation 2002.

Atmel Corporation makes no warranty for the use of its products, other than those expressly contained in the Company's standard warranty which is detailed in Atmel's Terms and Conditions located on the Company's web site. The Company assumes no responsibility for any errors which may appear in this document, reserves the right to change devices or specifications detailed herein at any time without notice, and does not make any commitment to update the information contained herein. No licenses to patents or other intellectual property of Atmel are granted by the Company in connection with the sale of Atmel products, expressly or by implication. Atmel's products are not authorized for use as critical components in life support devices or systems.

ATMEL® is a registered trademark of Atmel.

Other terms and product names may be the trademarks of others.



Printed on recycled paper.