

DUAL J-K FLIP FLOP WITH CLEAR

- **HIGH SPEED**
 $f_{MAX} = 58 \text{ MHz (TYP.) at } V_{CC} = 5V$
- **LOW POWER DISSIPATION**
 $I_{CC} = 2 \mu A \text{ (MAX.) at } T_A = 25^\circ C$
- **HIGH NOISE IMMUNITY**
 $V_{NIH} = V_{NIL} = 28\% V_{CC} \text{ (MIN.)}$
- **OUTPUT DRIVE CAPABILITY**
 10 LSTTL LOADS
- **SYMMETRICAL OUTPUT IMPEDANCE**
 $|I_{OH}| = I_{OL} = 4 \text{ mA (MIN.)}$
- **BALANCED PROPAGATION DELAYS**
 $t_{PLH} = t_{PHL}$
- **WIDE OPERATING VOLTAGE RANGE**
 $V_{CC} \text{ (OPR)} = 2V \text{ to } 6V$
- **PIN AND FUNCTION COMPATIBLE**
 WITH 54/74LS107

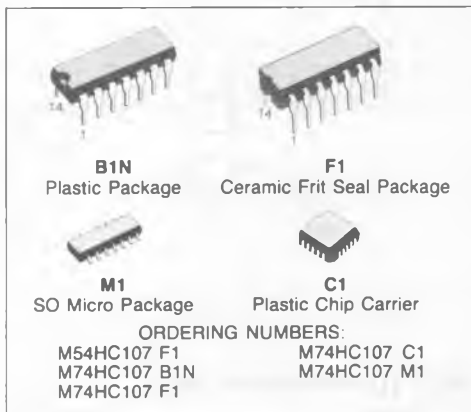
DESCRIPTION

The M54/74HC107 is a high speed CMOS DUAL J-K FLIP-FLOP fabricated in silicon gate C²MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low power consumption. These flip-flop are edge sensitive to the clock input and change state on the negative going transition of the clock pulse. Each one has independent J, K, CLOCK, and CLEAR inputs and Q and $\bar{Q}$ outputs. CLEAR is independent of the clock and accomplished by a logic low on the input. All inputs are equipped with protection circuits against static discharge and transient excess voltage.

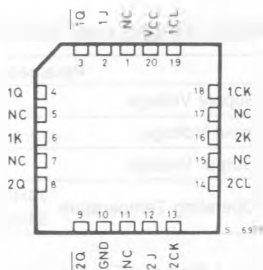
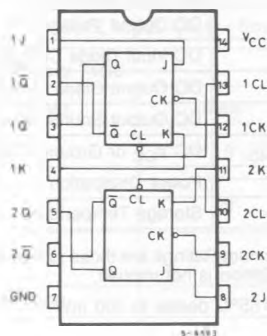
TRUTH TABLE

INPUTS				OUTPUTS	
CLEAR	CLOCK	J	K	Q	$\bar{Q}$
L	X	X	X	L	H
H		L	L	NO CHANGE	
H		L	H	L	H
H		H	L	H	L
H		H	H	TOGGLE	
H		X	X	NO CHANGE	

X: DON'T CARE

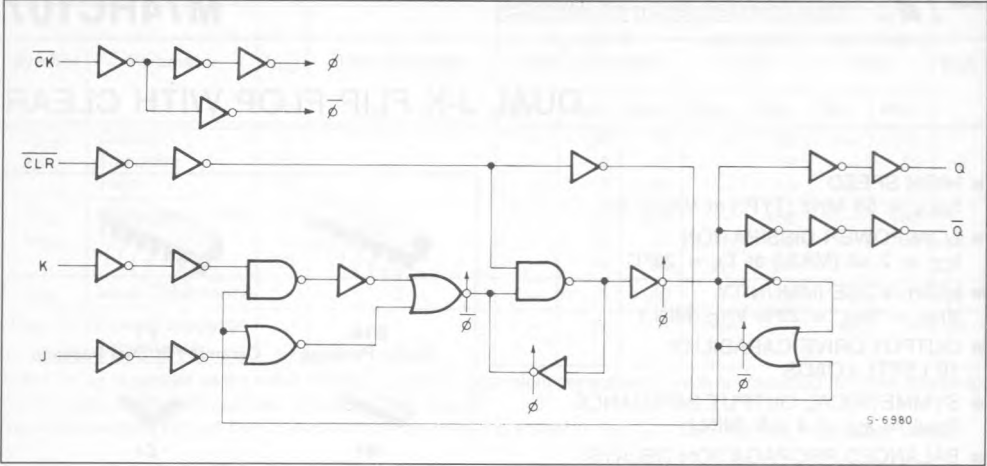


PIN CONNECTIONS (top view)



NC =
No Internal
Connection

LOGIC DIAGRAM (1/2 Package)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{CC}	Supply Voltage	− 0.5 to 7	V
V _I	DC Input Voltage	− 0.5 to V _{CC} + 0.5	V
V _O	DC Output Voltage	− 0.5 to V _{CC} + 0.5	V
I _{IK}	DC Input Diode Current	± 20	mA
I _{OK}	DC Output Diode Current	± 20	mA
I _O	DC Output Source Sink Current Per Output Pin	± 25	mA
I _{CC} or I _{GND}	DC V _{CC} or Ground Current	± 50	mA
P _D	Power Dissipation	500 (*)	mW
T _{stg}	Storage Temperature	− 65 to 150	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: ≡ 65°C derate to 300 mW by 10 mW/°C: 65°C to 85°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V _{CC}	Supply Voltage	2 to 6	V
V _I	Input Voltage	0 to V _{CC}	V
V _O	Output Voltage	0 to V _{CC}	V
T _A	Operating Temperature 74HC Series 54HC Series	− 40 to 85 − 55 to 125	°C
t _r , t _f	Input Rise and Fall Time	V _{CC} { 2 V 0 to 1000 4.5V 0 to 500 6 V 0 to 400	ns

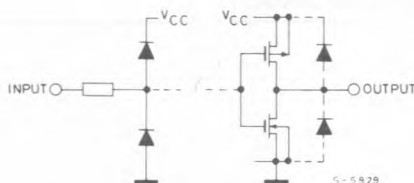
DC SPECIFICATIONS

Symbol	Parameter	V _{CC}	Test Condition	T _A = 25°C 54HC and 74HC			- 40 to 85°C 74HC		- 55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V _{IH}	High Level Input Voltage	2.0 4.5 6.0		1.5 3.15 4.2	— — —	— — —	1.5 3.15 4.2	— — —	1.5 3.15 4.2	— — —	V
V _{IL}	Low Level Input Voltage	2.0 4.5 6.0		— — —	— — —	0.5 1.35 1.8	— 1.35 1.8	0.5 1.35 1.8	— 1.35 1.8	0.5 1.35 1.8	V
V _{OH}	High Level Output Voltage	2.0	V _I	1.9	2.0	—	1.9	—	1.9	—	V
		4.5	V _{IH} or V _{IL}	4.4	4.5	—	4.4	—	4.4	—	
		6.0		5.9	6.0	—	5.9	—	5.9	—	
		4.5 6.0	— 4.0 mA — 5.2 mA	4.18 5.68	4.31 5.8	— —	4.13 5.63	— —	4.10 5.60	— —	
V _{OL}	Low Level Output Voltage	2.0	V _{IH} or V _{IL}	—	0	0.1	—	0.1	—	0.1	V
		4.5		—	0	0.1	—	0.1	—	0.1	
		6.0		—	0	0.1	—	0.1	—	0.1	
		4.5 6.0	4.0 mA 5.2 mA	— —	0.17 0.18	0.26 0.26	— —	0.33 0.33	— —	0.40 0.40	
I _I	Input Leakage Current	6.0	V _I = V _{CC} or GND	—	—	± 0.1	—	± 1	—	± 1	μA
I _{CC}	Quiescent Supply Current	6.0	V _I = V _{CC} or GND	—	—	2	—	20	—	40	μA

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V, T_A = 25°C, C_L = 15pF, Input t_r = t_f = 6ns)

Symbol	Parameter	54HC and 74HC			Unit
		Min.	Typ.	Max.	
t _{TLH} t _{THL}	Output Transition Time		4	8	ns
t _{PLH} t _{PHL}	Propagation Delay Time (CLOCK-Q, $\bar{Q}$)		18	29	ns
t _{PLH} t _{PHL}	Propagation Delay Time (CLEAR-Q, $\bar{Q}$)		24	36	ns
f _{MAX}	Maximum Clock Frequency	34	58		MHz

INPUT AND OUTPUT EQUIVALENT CIRCUIT



AC ELECTRICAL CHARACTERISTICS ($C_L = 50\text{pF}$, Input $t_r = t_f = 6\text{ns}$)

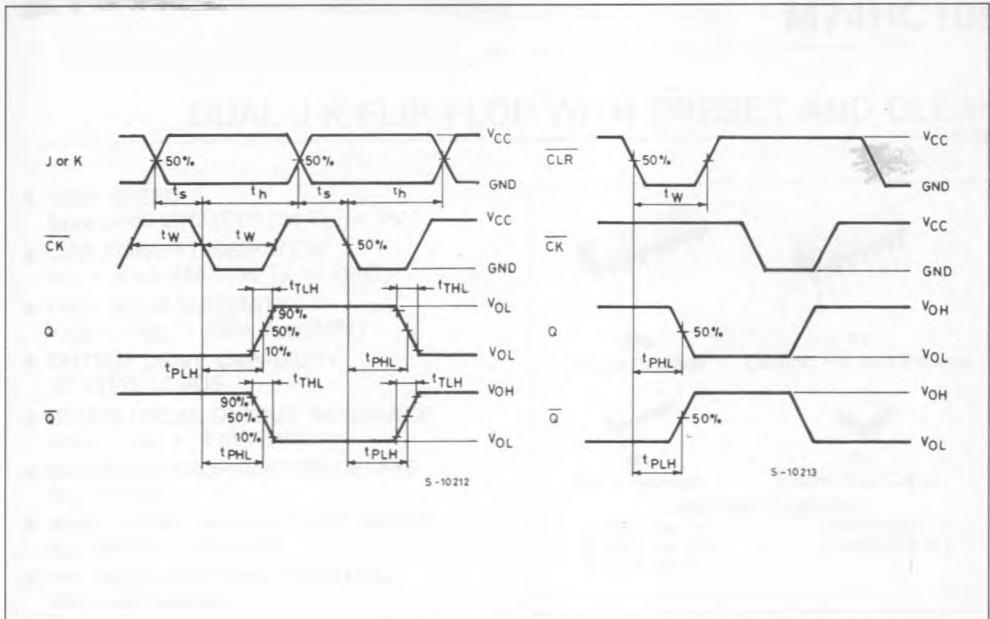
Symbol	Parameter	V_{CC}	Test Condition	$T_A = 25^\circ\text{C}$ 54HC and 74HC			-40 to 85°C 74HC		-55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0 4.5 6.0		— — —	30 8 7	75 15 13	— — —	95 19 16	— — —	110 22 19	ns
t_{PLH} t_{PHL}	Propagation Delay Time (CLOCK-Q, $\bar{Q}$)	2.0 4.5 6.0		— — —	77 21 18	165 33 28	— — —	205 41 35	— — —	250 50 43	ns
t_{PLH} t_{PHL}	Propagation Delay Time (CLEAR-Q, $\bar{Q}$)	2.0 4.5 6.0		— — —	116 29 25	220 44 37	— — —	275 55 47	— — —	330 66 56	ns
f_{MAX}	Maximum Clock Frequency	2.0 4.5 6.0		6 30 35	14 50 58	— — —	4.8 24 28	— — —	4.0 20 24	— — —	MHz
$t_{W(L)}$	Minimum Pulse Width (CLEAR)	2.0 4.5 6.0		— — —	40 10 9	100 20 17	— — —	125 25 21	— — —	150 30 26	ns
$t_{W(L)}$ $t_{W(H)}$	Minimum Pulse Width (CLOCK)	2.0 4.5 6.0		— — —	30 8 7	75 15 13	— — —	95 19 16	— — —	110 22 19	ns
t_s	Minimum Set-Up Time	2.0 4.5 6.0		— — —	30 8 7	75 15 13	— — —	95 19 16	— — —	110 22 19	ns
t_h	Minimum Hold Time	2.0 4.5 6.0		— — —	— — —	0 0 0	— — —	0 0 0	— — —	0 0 0	ns
t_{rem}	Minimum Removal Time (CLEAR)	2.0 4.5 6.0		— — —	— — —	25 5 5	— — —	30 6 6	— — —	40 8 7	ns
C_{IN}	Input Capacitance			—	5	10	—	10	—	10	pF
$C_{PD} (*)$	Power Dissipation Capacitance			—	46	—	—	—	—	—	pF

Note (*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load.

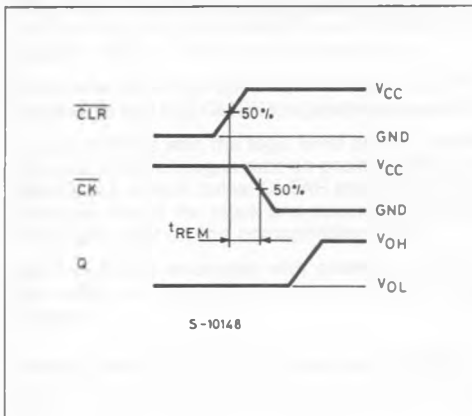
Average operating current can be obtained by the following equation.

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/2 \text{ per F/F}$$

SWITCHING CHARACTERISTICS TEST WAVEFORM



SWITCHING CHARACTERISTICS TEST WAVEFORMS

TEST CIRCUIT I_{CC} (Opr.)