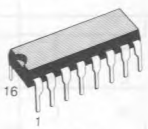
SGS-THOMSON MICROELECTRONICS

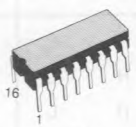
M54HC131
M74HC131

3 TO 8 LINE DECODER/LATCH

- LOW POWER DISSIPATION
  I_{CC} = 4 μA (MAX.) at T_A = 25°C
- HIGH NOISE IMMUNITY
  V_{NIH} = V_{NIL} = 28% V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}|$ = I_{OL} = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  t_{PLH} = t_{PHL}
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2V to 6V
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS131



B1N
Plastic Package



F1
Ceramic Frit Seal Package

M1
Micro Package

C1
Plastic Chip Carrier

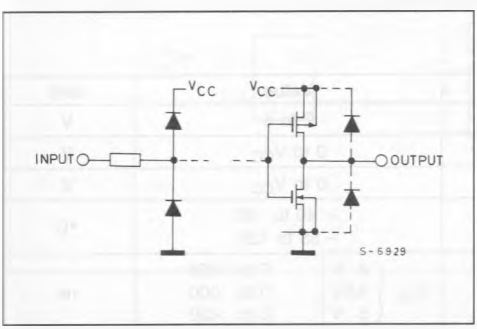
ORDERING NUMBERS:

M54HC131 F1	M74HC131 C1
M74HC131 B1N	M74HC131 M1
M74HC131 F1	

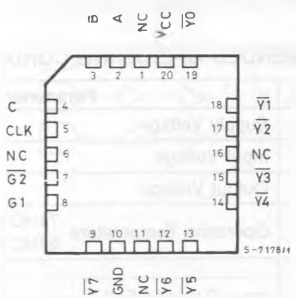
DESCRIPTION

The M54/74HC131 is a high speed CMOS 3 TO 8 LINE DECODER/LATCH fabricated in silicon gate C²MOS technology.
It has the same high speed performance of LSTTL combined with true CMOS low power consumption. This device is a DECODER/LATCH capable of selecting arbitrarily one of eight outputs by three binary inputs A, B, and C, in this case, the selected output is at logic "low".
Also, when ENABLE input G1 is set low or ENABLE input $\overline{G2}$ is set high, selection is inhibited regardless of other input signals and all the outputs are at high. All inputs are equipped with protection circuits against static discharge and transient excess voltage.

INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN CONNECTIONS (top view)



NC =
No Internal
Connection

TRUTH TABLE

INPUTS						OUTPUTS							
ENABLE			SELECT										
CLK	G1	$\overline{G2}$	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	X	H	X	X	X	H	H	H	H	H	H	H	H
X	L	X	X	X	X	H	H	H	H	H	H	H	H
↑	H	L	L	L	L	L	H	H	H	H	H	H	H
↑	H	L	L	L	H	H	L	H	H	H	H	H	H
↑	H	L	L	H	L	H	H	L	H	H	H	H	H
↑	H	L	L	H	H	H	H	H	L	H	H	H	H
↑	H	L	H	L	L	H	H	H	H	L	H	H	H
↑	H	L	H	L	H	H	H	H	H	H	L	H	H
↑	H	L	H	H	L	H	H	H	H	H	H	L	H
↑	H	L	H	H	H	H	H	H	H	H	H	H	L
L	H	L	X	X	X	Outputs corresponding to stored address L: all others H							

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	− 0.5 to 7	V
V_I	DC Input Voltage	− 0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	− 0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	− 65 to 150	°C

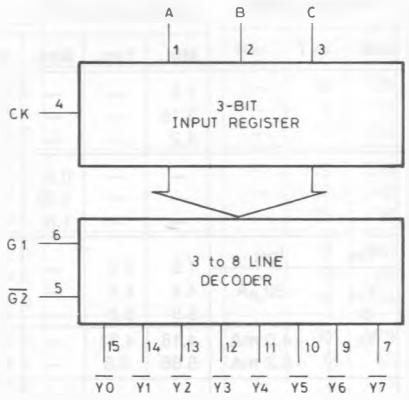
Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: ≡ 65°C derate to 300 mW by 10 mW/°C: 65°C to 85°C

RECOMMENDED OPERATING CONDITIONS

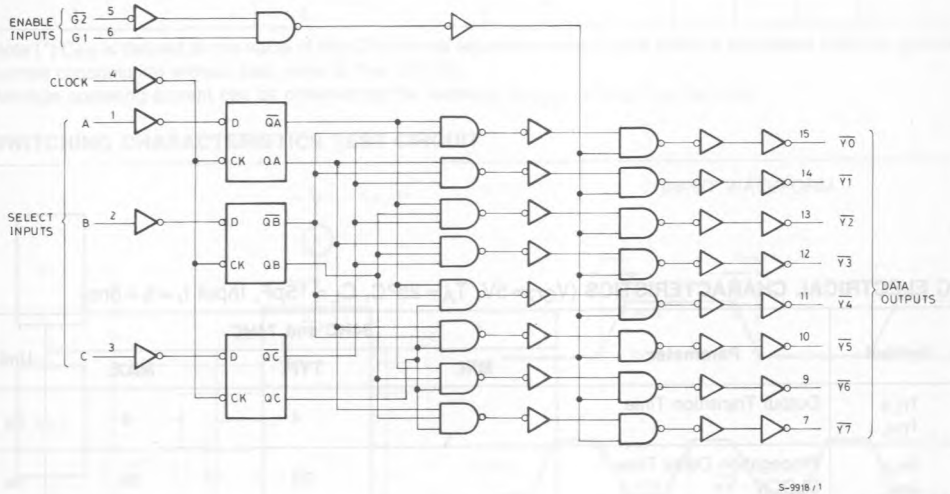
Symbol	Parameter	Value		Unit
V_{CC}	Supply Voltage	2 to 6		V
V_I	Input Voltage	0 to V_{CC}		V
V_O	Output Voltage	0 to V_{CC}		V
T_A	Operating Temperature 74HC Series 54HC Series	− 40 to 85 − 55 to 125		°C
t_r, t_f	Input Rise and Time	V_{CC} = 2 V	0 to 1000	ns
		V_{CC} = 4.5V	0 to 500	
		V_{CC} = 6 V	0 to 400	

BLOCK DIAGRAM



V_{CC} = 16
GND = 8

LOGIC DIAGRAM



DC SPECIFICATIONS

Symbol	Parameter	V_{CC}	Test Condition		$T_A = 25°C$ 54HC and 74HC			− 40 to 85°C 74HC		− 55 to 125°C 54HC		Unit
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5	—	—	1.5	—	1.5	—	V
		4.5			3.15	—	—	3.15	—	3.15	—	
		6.0			4.2	—	—	4.2	—	4.2	—	
V_{IL}	Low Level Input Voltage	2.0			—	—	0.5	—	0.5	—	0.5	V
		4.5			—	—	1.35	—	1.35	—	1.35	
		6.0			—	—	1.8	—	1.8	—	1.8	
V_{OH}	High Level Output Voltage	2.0	V_{IN}	I_{OH}	1.9	2.0	—	1.9	—	1.9	—	V
		4.5	V_{IH} or V_{IL}	− 20 μA	4.4	4.5	—	4.4	—	4.4	—	
		6.0			5.9	6.0	—	5.9	—	5.9	—	
		4.5		− 4.0 mA	4.18	4.31	—	4.13	—	4.10	—	
		6.0		− 5.2 mA	5.68	5.8	—	5.63	—	5.60	—	
V_{OL}	Low Level Output Voltage	2.0	V_{IH} or V_{IL}	20 μA	—	0	0.1	—	0.1	—	0.1	V
		4.5			—	0	0.1	—	0.1	—	0.1	
		6.0			—	0	0.1	—	0.1	—	0.1	
		4.5		4.0 mA	—	0.17	0.26	—	0.33	—	0.40	
		6.0		5.2 mA	—	0.18	0.26	—	0.33	—	0.40	
I_{IN}	Input Leakage Current	6.0	$V_{IN} = V_{CC}$ or GND		—	—	±0.1	—	±1	—	±1	μA
I_{CC}	Quiescent Supply Current	6.0	$V_{IN} = V_{CC}$ or GND		—	—	4.0	—	40.0	—	80.0	

AC ELECTRICAL CHARACTERISTICS ($V_{CC} = 5V$, $T_A = 25°C$, $C_L = 15pF$, Input $t_r = t_f = 6ns$)

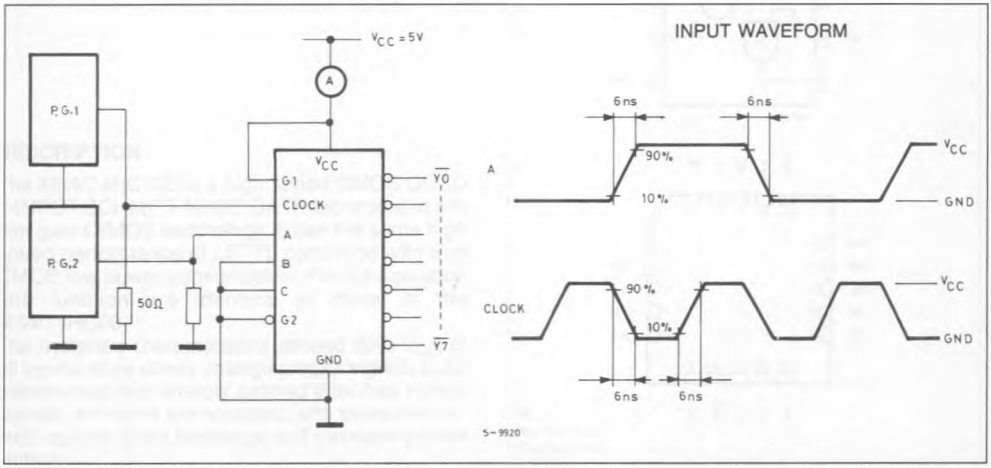
Symbol	Parameter	54HC and 74HC			Unit
		MIN.	TYP.	MAX.	
t_{TLH} t_{THL}	Output Transition Time		4	8	ns
t_{PLH} t_{PHL}	Propagation Delay Time CLOCK - $\overline{Yn}$		23	36	ns
t_{PLH} t_{PHL}	Propagation Delay Time G1, $\overline{G2}$ - $\overline{Yn}$		15	24	ns

AC ELECTRICAL CHARACTERISTICS ($C_L = 50pF$, Input $t_r = t_f = 6ns$)

Symbol	Parameter	V_{CC}	Test Condition	$T_A = 25°C$ 54HC and 74HC			-40 to $85°C$ 74HC		-55 to $125°C$ 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0		—	30	75	—	95	—	110	ns
		4.5		—	8	15	—	19	—	22	
		6.0		—	7	13	—	16	—	19	
t_{PLH} t_{PHL}	Propagation Delay Time (CLOCK - $\overline{Yn}$)	2.0		—	112	210	—	265	—	315	ns
		4.5		—	27	42	—	53	—	63	
		6.0		—	23	36	—	45	—	54	
t_{PLH} t_{PHL}	Propagation Delay Time (G1, $\overline{G2}$ $\overline{Yn}$)	2.0		—	72	140	—	175	—	210	ns
		4.5		—	18	28	—	35	—	42	
		6.0		—	16	24	—	30	—	36	
$t_{W(H)}$ $t_{W(L)}$	Minimum Pulse Width (CLOCK)	2.0		—	30	75	—	95	—	110	ns
		4.5		—	8	15	—	19	—	22	
		6.0		—	7	13	—	16	—	19	
t_s	Minimum Set-up Time (A, B, C)	2.0		—	12	50	—	65	—	75	ns
		4.5		—	3	10	—	13	—	15	
		6.0		—	2	9	—	11	—	13	
t_h	Minimum Hold Time (A, B, C)	2.0		—	—	5	—	5	—	5	ns
		4.5		—	—	5	—	5	—	5	
		6.0		—	—	5	—	5	—	5	
C_{IN}	Input Capacitance			—	5	10	—	10	—	10	pF
C_{PD} (*)	Power Dissipation Capacitance			—	89	—	—	—	—	—	

Note (*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load (refer to Test circuit).
Average operating current can be obtained by the following: $I_{CC(opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$

SWITCHING CHARACTERISTICS TEST CIRCUIT



SWITCHING CHARACTERISTICS TEST WAVEFORM