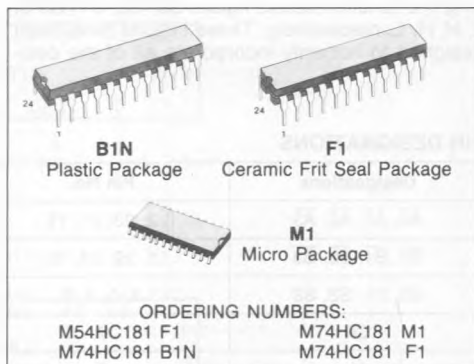


ARITHMETIC LOGIC UNIT/FUNCTION GENERATOR

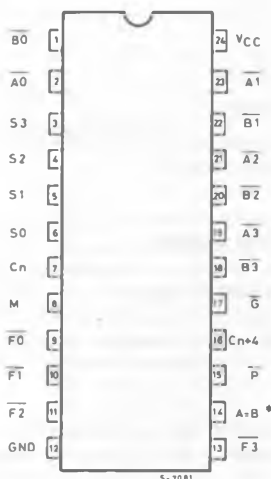
- LOW POWER DISSIPATION
 $I_{CC} = 4 \mu A$ (MAX.) at $T_A = 25^\circ C$
- HIGH NOISE IMMUNITY
 $V_{NIH} = V_{NIL} = 28\% V_{CC}$ (MIN.)
- OUTPUT DRIVE CAPABILITY
 10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
 $|I_{OH}| = I_{OL} = 6 mA$ (MIN.)
- BALANCED PROPAGATION DELAYS
 $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
 V_{CC} (OPR) = 2V to 6V
- PIN AND FUNCTION COMPATIBLE
 WITH 54/74LS181



DESCRIPTION

The M54/74HC181 is a high speed CMOS ARITHMETIC LOGIC UNIT/FUNCTION GENERATOR fabricated with silicon gate C²MOS technology. It has the same high speed performance of SLTTL combined with true CMOS low power consumption. These circuits perform 16 binary arithmetic operations on two 4-bit words as shown in Tables 1 and 2. These operations are selected by the four function-select lines (S₀, S₁, S₂, S₃) and include addition, subtraction, decrement, and straight transfer. When performing arithmetic manipulations, the internal carries must be enabled by applying a low-level voltage to the mode control input (M). A full carry look-ahead scheme is made available in these devices for fast, simultaneous carry generation by means of two cascade-outputs (pins 15 and 17) for the four bits in the package. When used in conjunction with the M54HC182 or M74HC182, full carry look-ahead circuits, high-speed arithmetic operations can be performed. These circuits will accommodate active-high or active-low data, if the pin designations are interpreted as shown below. Subtraction is accomplished by 1's complement addition where the 1's complement of the subtrahend is generated internally. The resultant output is 1—B—1, which requires an end-around or forced carry to produce A—B. The 181 can also be utilized as a comparator. The A = B output is internally decoded from the function outputs (F₀, F₁, F₂, F₃) so that when two words of equal magnitude are applied at the A and B inputs, it will assume a high level to indicated equality (A = B).

PIN CONNECTIONS (top view)



*: Open drain Output Structure

DESCRIPTION (Continued)

The ALU should be in the subtract mode with $C_n = H$ when performing this comparison. The $A = B$ output is open-drain so that it can be wire-AND connected to give a comparison for more than four bits. The carry output ($C_n + 4$) can also be used to supply relative magnitude information. Again, the ALU should be placed in the subtract mode by placing the function select inputs S_3, S_2, S_1, S_0 at L, H, H, L, respectively. These circuits have been designed to not only incorporate all of the desi-

gner's requirements for arithmetic operations, but also to provide 16 possible functions of two Boolean variables without the use of external circuitry. These logic functions are selected by use of the four function-select inputs (S_0, S_1, S_2, S_3) with the mode-control input (M) at a high level to disable the internal carry. All inputs are equipped with protection circuits against static discharge and transient excess voltage.

PIN DESIGNATIONS

Designations	Pin No.	Function
$A_0, \overline{A_1}, A_2, \overline{A_3}$	2, 23, 21, 19	Word A Inputs
$B_0, \overline{B_1}, B_2, \overline{B_3}$	1, 22, 20, 18	Word B Inputs
S_0, S_1, S_2, S_3	6, 5, 4, 3	Function Select Inputs
C_n	7	Inv. Carry Input
M	8	Mode Control Input
$F_0, \overline{F_1}, F_2, \overline{F_3}$	9, 10, 11, 13	Function Outputs
$A = B$	14	Comparator Outputs
$\overline{P}$	15	Carry Propagate Output
$C_n + 4$	16	Inv. Carry Output
$\overline{G}$	17	Carry Generate Output
V_{CC}	24	Supply Voltage
GND	12	Ground

PIN NUMBER	2	1	23	22	21	20	19	18	9	10	11	13	7	16	15	17
ACTIVE-LOW DATA (Table 1)	$\overline{A_0}$	$\overline{B_0}$	$\overline{A_1}$	$\overline{B_1}$	$\overline{A_2}$	$\overline{B_2}$	$\overline{A_3}$	$\overline{B_3}$	$\overline{F_0}$	$\overline{F_1}$	$\overline{F_2}$	$\overline{F_3}$	C_n	$C_n + 4$	$\overline{P}$	$\overline{G}$
ACTIVE-HIGH DATA (Table 2)	A0	B0	A1	B1	A2	B2	A3	B3	F0	F1	F2	F3	Cn	Cn + 4	X	Y

Input C_n	Output $C_n + 4$	Active-Low data (Figure 1)	Active-High data (Figure 2)
H	H	$A \geq B$	$A \leq B$
H	L	$A < B$	$A > B$
L	H	$A > B$	$A < B$
L	L	$A \leq B$	$A \geq B$

Figure 1

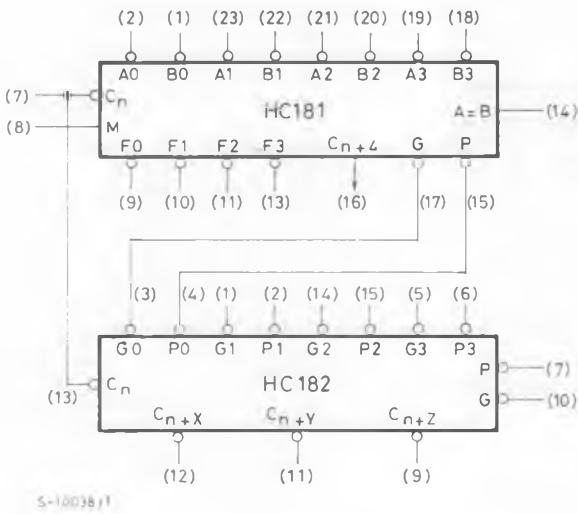
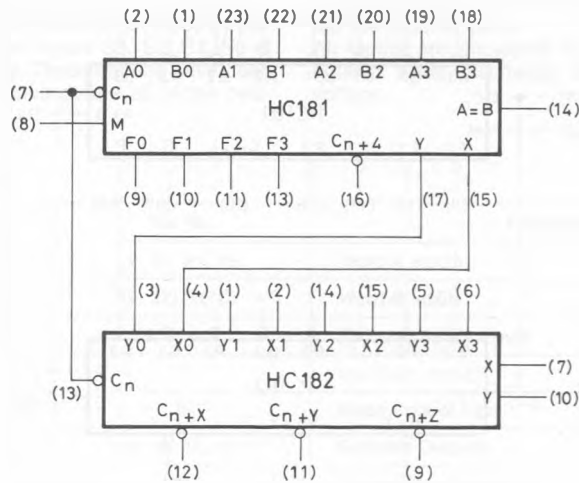


TABLE 1

Selection					Active Low Data	
					M = L: Arithmetic Operations	
					C _n = L (no carry)	C _n = H (with carry)
S3	S2	S1	S0	M = H Logic Functions		
L	L	L	L	$F = \bar{A}$	F = A Minus 1	F = A
L	L	L	H	$F = \bar{A}B$	F = AB Minus 1	F = AB
L	L	H	L	$F = \bar{A} + B$	F = AB Minus 1	F = (AB)
L	L	H	H	$F = 1$	F = Minus 1 (2's Compl)	F = Zero
L	H	L	L	$F = \bar{A} + B$	F = A Plus (A + B)	F = A Plus (A + B) Plus 1
L	H	L	H	$F = \bar{B}$	F = AB Plus (A + B)	F = AB Plus (A + B) Plus 1
L	H	H	L	$F = \bar{A} \oplus B$	F = A Minus B Minus 1	F = A Minus B
L	H	H	H	$F = A + B$	F = A + B	F = (A + B) Plus 1
H	L	L	L	$F = \bar{A}B$	F = A Plus (A + B)	F = A Plus (A + B) Plus 1
H	L	L	H	$F = A \oplus B$	F = A Plus B	F = A Plus B Plus 1
H	L	H	L	F = B	F = AB Plus (A + B)	F = AB Plus (A + B) Plus 1
H	L	H	H	F = A + B	F = A + B	F = (A + B) Plus 1
H	H	L	L	F = 0	F = A Plus A *	F = A Plus A Plus 1
H	H	L	H	$F = \bar{A}B$	F = AB Plus A	F = AB Plus A Plus 1
H	H	H	L	F = AB	F = AB Plus A	F = AB Plus A Plus 1
H	H	H	H	F = A	F = A	F = A Plus 1

* Each bit is shifted to the next more significant position.

Figure 2



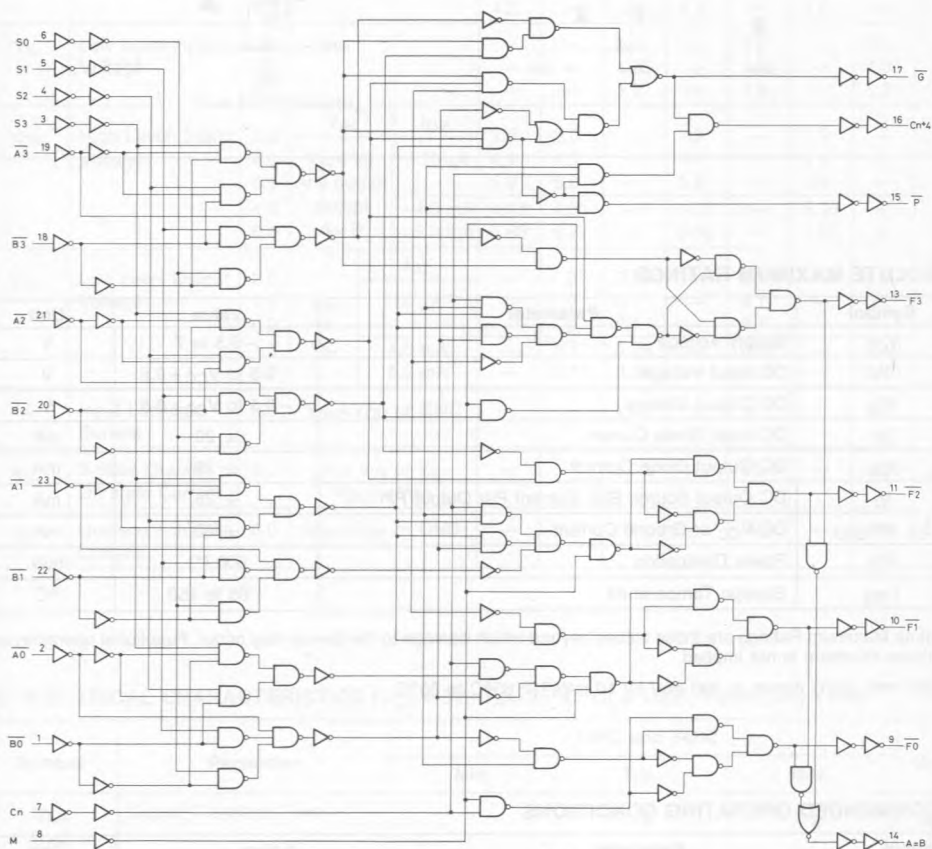
S-10037

TABLE 2

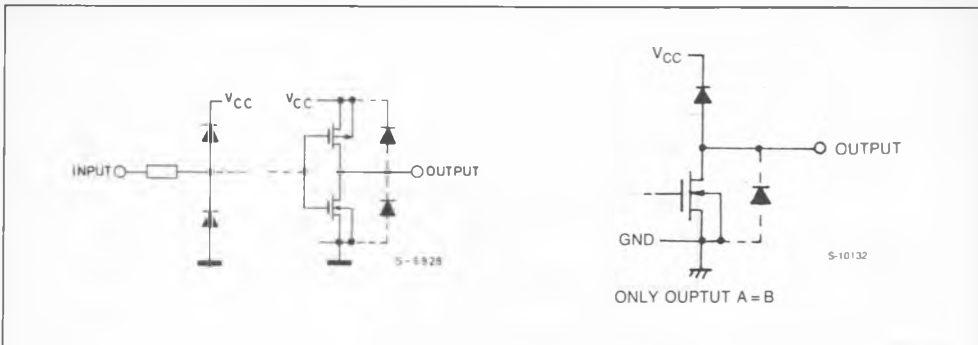
Selection					Active High Data		
					M = H Logic Functions	M = L: Arithmetic Operations	
						C _n = H (no carry)	C _n = L (with carry)
S3	S2	S1	S0				
L	L	L	L	$F = \bar{A}$	$F = A$	$F = A$	$F = A \text{ Plus } 1$
L	L	L	H	$F = \bar{A} + B$	$F = A + B$	$F = A + B$	$F = (A + B) \text{ Plus } 1$
L	L	H	L	$F = \bar{A} \bar{B}$	$F = A + \bar{B}$	$F = A + \bar{B}$	$F = (A + \bar{B}) \text{ Plus } 1$
L	L	H	H	$F = 0$	$F = \text{Minus } 1 \text{ (2's Comp1)}$	$F = \text{Minus } 1 \text{ (2's Comp1)}$	$F = \text{Zero}$
L	H	L	L	$F = \bar{A} \bar{B}$	$F = A \text{ Plus } \bar{A} \bar{B}$	$F = A \text{ Plus } \bar{A} \bar{B}$	$F = A \text{ Plus } \bar{A} \bar{B} \text{ Plus } 1$
L	H	L	H	$F = \bar{B}$	$F = (A + B) \text{ Plus } \bar{A} \bar{B}$	$F = (A + B) \text{ Plus } \bar{A} \bar{B}$	$F = (A + B) \text{ Plus } \bar{A} \bar{B} \text{ Plus } 1$
L	H	H	L	$F = A \oplus B$	$F = A \text{ Minus } B \text{ Minus } 1$	$F = A \text{ Minus } B \text{ Minus } 1$	$F = A \text{ Minus } B$
L	H	H	H	$F = \bar{A} \bar{B}$	$F = \bar{A} \bar{B} \text{ Minus } 1$	$F = \bar{A} \bar{B} \text{ Minus } 1$	$F = \bar{A} \bar{B}$
H	L	L	L	$F = \bar{A} + B$	$F = A \text{ Plus } \bar{A} \bar{B}$	$F = A \text{ Plus } \bar{A} \bar{B}$	$F = A \text{ Plus } \bar{A} \bar{B} \text{ Plus } 1$
H	L	L	H	$F = \bar{A} \oplus \bar{B}$	$F = A \text{ Plus } B$	$F = A \text{ Plus } B$	$F = A \text{ Plus } B \text{ Plus } 1$
H	L	H	L	$F = B$	$F = (A + \bar{B}) \text{ Plus } \bar{A} \bar{B}$	$F = (A + \bar{B}) \text{ Plus } \bar{A} \bar{B}$	$F = (A + \bar{B}) \text{ Plus } \bar{A} \bar{B} \text{ Plus } 1$
H	L	H	H	$F = \bar{A} \bar{B}$	$F = \bar{A} \bar{B} \text{ Minus } 1$	$F = \bar{A} \bar{B} \text{ Minus } 1$	$F = \bar{A} \bar{B}$
H	H	L	L	$F = 1$	$F = A \text{ Plus } A^*$	$F = A \text{ Plus } A^*$	$F = A \text{ Plus } A \text{ Plus } 1$
H	H	L	H	$F = A + \bar{B}$	$F = (A + B) \text{ Plus } A$	$F = (A + B) \text{ Plus } A$	$F = (A + B) \text{ Plus } A \text{ Plus } 1$
H	H	H	L	$F = A + B$	$F = (A + \bar{B}) \text{ Plus } A$	$F = (A + \bar{B}) \text{ Plus } A$	$F = (A + \bar{B}) \text{ Plus } A \text{ Plus } 1$
H	H	H	H	$F = A$	$F = A \text{ Minus } 1$	$F = A \text{ Minus } 1$	$F = A$

* Each bit is shifted to the next more significant position.

LOGIC DIAGRAM



INPUT AND OUTPUT EQUIVALENT CIRCUIT



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	- 0.5 to 7	V
V_I	DC Input Voltage	- 0.5 to $V_{CC} + 0.5$	V
V_O	DC Output Voltage	- 0.5 to $V_{CC} + 0.5$	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	- 65 to 150	$^{\circ}\text{C}$

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: 65 $^{\circ}\text{C}$ derate to 300 mW by 10 mW/ $^{\circ}\text{C}$: 65 $^{\circ}\text{C}$ to 85 $^{\circ}\text{C}$

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	2 to 6	V
V_I	Input Voltage	0 to V_{CC}	V
V_O	Output Voltage	0 to V_{CC}	V
T_A	Operating Temperature 74HC Series 54HC Series	- 40 to 85 - 55 to 125	$^{\circ}\text{C}$
t_r, t_f	Input Rise and Fall Time	$V_{CC} \begin{cases} 2 \text{ V} & 0 \text{ to } 1000 \\ 4.5 \text{ V} & 0 \text{ to } 500 \\ 6 \text{ V} & 0 \text{ to } 400 \end{cases}$	ns

DC SPECIFICATIONS

Symbol	Parameter	V _{CC}	Test Condition		T _A = 25°C 54HC and 74HC			– 40 to 85°C 74HC		– 55 to 125°C 54HC		Unit
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V _{IH}	High Level Input Voltage	2.0 4.5 6.0			1.5 3.15 4.2	— — —	— — —	1.5 3.15 4.2	— — —	1.5 3.15 4.2	— — —	V
V _{IL}	Low Level Input Voltage	2.0 4.5 6.0			— — —	— — —	0.5 1.35 1.8	— 1.35 1.8	0.5 1.35 1.8	— — —	0.5 1.35 1.8	V
V _{OH}	High Level Output Voltage	2.0	V _{IN}	I _{OH}	1.9	2.0	—	1.9	—	1.9	—	V
		4.5	V _{IH} = V _{IL}	– 20 µA	4.4	4.5	—	4.4	—	4.4	—	
		6.0	Any output		5.9	6.0	—	5.9	—	5.9	—	
		4.5	except	– 4.0 mA	4.18	4.31	—	4.13	—	4.10	—	
		6.0	A = B	– 5.2 mA	5.68	5.8	—	5.63	—	5.60	—	
V _{OL}	Low Level Output Voltage	2.0	V _{IN} or V _{IH}	I _{OL}	—	0	0.1	—	0.1	—	0.1	V
		4.5		20 µA	—	0	0.1	—	0.1	—	0.1	
		6.0			—	0	0.1	—	0.1	—	0.1	
		4.5		4.0 mA	—	0.17	0.26	—	0.33	—	0.40	
		6.0		5.2 mA	—	0.18	0.26	—	0.33	—	0.40	
I _{IN}	Input Leakage Current	6.0	V _{IN} = V _{CC} or GND		—	—	± 0.1	—	± 1	—	± 1	µA
I _{OZ}	3-State Output Off state Current	6.0	V _I = V _{IH} or V _{IL} V _{OUT} = V _{CC}		—	—	± 0.5	—	± 5.0	—	± 10	
I _{CC}	Quiescent Supply Current	6.0	V _{IN} = V _{CC} or GND		—	—	4	—	40	—	80	

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V, T_A = 25°C, C_L = 15pF, Input t_r = t_f = 6ns)

Symbol	Parameter	54HC and 74HC			Unit
		Min.	Typ.	Max.	
t _{TLH} t _{THL}	Output Transition Time		4	8	ns
t _{PLH} t _{PHL}	Propagation Delay Time (1)		14	23	ns
t _{PLH} t _{PHL}	Propagation Delay Time (2)		27	42	ns
t _{PLH} t _{PHL}	Propagation Delay Time (3)		26	41	ns
t _{PLH} t _{PHL}	Propagation Delay Time (4)		24	37	ns

AC ELECTRICAL CHARACTERISTICS (Continued)

Symbol	Parameter	54HC and 74HC			Unit
		Min.	Typ.	Max.	
t_{PLH} t_{PHL}	Propagation Delay Time (5)		25	39	ns
t_{PLH} t_{PHL}	Propagation Delay Time (6)		24	38	ns
t_{PLH} t_{PHL}	Propagation Delay Time (7)		23	37	ns
t_{PLH} t_{PHL}	Propagation Delay Time (8)		23	37	ns
t_{PLH} t_{PHL}	Propagation Delay Time (9)		30	46	ns
t_{PLH} t_{PHL}	Propagation Delay Time (10)		30	46	ns
t_{PLH} t_{PHL}	Propagation Delay Time (11)		24	37	ns
t_{PZL}	3-State Output•Enable Time (12)		27	42	ns
t_{PLZ}	3-State Output•Disable Time (12)		29	46	ns

AC ELECTRICAL CHARACTERISTICS ($C_L = 50\text{pF}$, Input $t_r = t_f = 6\text{ns}$)

Symbol	Parameter	V_{CC}	Test Condition	$T_A = 25^\circ\text{C}$ 54HC and 74HC			-40 to 85°C 74HC		-55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0 4.5 6.0		— — —	30 8 7	75 15 13	— — —	95 19 16	— — —	110 22 19	ns
t_{PLH} t_{PHL}	Propagation Delay Time (1)	2.0 4.5 6.0		— — —	68 17 14	135 27 23	— — —	170 34 29	— — —	205 41 35	ns
t_{PLH} t_{PHL}	Propagation Delay Time (2)	2.0 4.5 6.0		— — —	124 31 26	240 48 41	— — —	300 60 51	— — —	360 72 61	ns
t_{PLH} t_{PHL}	Propagation Delay Time (3)	2.0 4.5 6.0		— — —	120 30 26	235 47 40	— — —	295 59 50	— — —	355 71 60	ns
t_{PLH} t_{PHL}	Propagation Delay Time (4)	2.0 4.5 6.0		— — —	112 28 24	215 43 37	— — —	270 54 46	— — —	325 65 55	ns

AC ELECTRICAL CHARACTERISTICS (Continued)

Symbol	Parameter	V _{CC}	Test Condition	T _A = 25°C 54HC and 74HC			- 40 to 85°C 74HC		- 55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t _{PLH} t _{PHL}	Propagation Delay Time (5)	2.0 4.5 6.0		— — —	116 29 25	225 45 38	— — —	280 56 48	— — —	340 68 58	ns
t _{PLH} t _{PHL}	Propagation Delay Time (6)	2.0 4.5 6.0		— — —	116 29 25	220 44 37	— — —	275 55 47	— — —	330 66 56	ns
t _{PLH} t _{PHL}	Propagation Delay Time (7)	2.0 4.5 6.0		— — —	108 27 23	210 42 36	— — —	265 53 45	— — —	315 63 54	ns
t _{PLH} t _{PHL}	Propagation Delay Time (8)	2.0 4.5 6.0		— — —	108 27 23	210 42 36	— — —	265 53 45	— — —	315 63 54	ns
t _{PLH} t _{PHL}	Propagation Delay Time (9)	2.0 4.5 6.0		— — —	136 34 29	265 53 45	— — —	335 66 56	— — —	400 80 68	ns
t _{PLH} t _{PHL}	Propagation Delay Time (10)	2.0 4.5 6.0		— — —	136 34 29	265 53 45	— — —	335 66 56	— — —	400 80 68	ns
t _{PLH} t _{PHL}	Propagation Delay Time (11)	2.0 4.5 6.0		— — —	112 28 24	215 43 37	— — —	270 54 46	— — —	325 65 55	ns
t _{PZL}	3-State Output Enable Time (12)	2.0 4.5 6.0	R _L = 1kΩ	— — —	124 31 26	240 48 41	— — —	300 60 51	— — —	360 72 61	ns
t _{PLZ}	3-State Output Disable Time (12)	2.0 4.5 6.0	R _L = 1kΩ	— — —	140 35 30	260 52 44	— — —	325 65 55	— — —	390 78 66	ns
C _{IN}	Input Capacitance			—	5	10	—	10	—	10	pF
C _{PD} (*)	Power Dissipation Capacitance			—	216	—	—	—	—	—	pF

Note (*) C_{PD} is defined as the value of IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit)

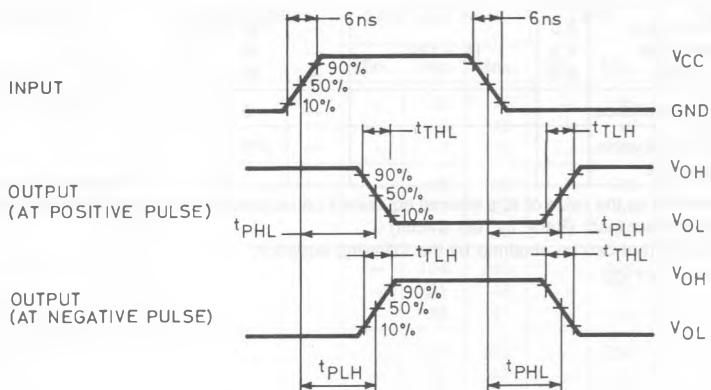
Average operating current can be obtained by the following equation:

$$I_{CC(opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

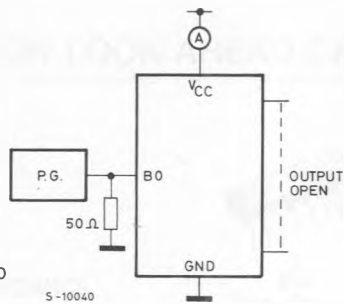
PROPAGATION DELAY TIME TEST CONDITIONS

Test No.	From (Input)	To (Output)	Test Conditions
(1)	C _n	C _n + 4	
(2)	Any $\bar{A}$ or $\bar{B}$	C _n + 4	M = GND, S0 = S3 = V _{CC} , S1 = S2 = GND (<u>SUM</u> mode)
(3)	Any $\bar{A}$ or $\bar{B}$	C _n + 4	M = GND, S0 = S3 = GND, S1 = S2 = V _{CC} (<u>DIFF</u> mode)
(4)	$\bar{C}_n$	Any $\bar{F}$	M = GND (<u>SUM</u> or <u>DIFF</u> mode)
(5)	Any $\bar{A}$ or $\bar{B}$	$\bar{G}$	M = GND, S0 = S3 = V _{CC} , S1 = S2 = GND (<u>SUM</u> mode)
(6)	Any $\bar{A}$ or $\bar{B}$	$\bar{G}$	M = GND, S0 = S3 = GND, S1 = S2 = V _{CC} (<u>DIFF</u> mode)
(7)	Any $\bar{A}$ or $\bar{B}$	$\bar{F}$	M = GND, S0 = S3 = V _{CC} , S1 = S2 = GND (<u>SUM</u> mode)
(8)	Any $\bar{A}$ or $\bar{B}$	$\bar{F}$	M = GND, S0 = S3 = GND, S1 = S2 = V _{CC} (<u>DIFF</u> mode)
(9)	$\bar{A}_1$ or $\bar{B}_1$	$\bar{F}_i$	M = GND, S0 = S3 = V _{CC} , S1 = S2 = GND (<u>SUM</u> mode)
(10)	$\bar{A}_1$ or $\bar{B}_1$	$\bar{F}_i$	M = GND, S0 = S3 = GND, S1 = S2 = V _{CC} (<u>DIFF</u> mode)
(11)	$\bar{A}_1$ or $\bar{B}_1$	$\bar{F}_i$	M = V _{CC} (Logic Mode)
(12)	Any $\bar{A}$ or $\bar{B}$	A = B	M = GND, S0 = S3 = GND, S1 = S2 = V _{CC} (<u>DIFF</u> mode)

SWITCHING CHARACTERISTICS TEST WAVEFORM



S-10041

TEST CIRCUIT I_{CC} (Opr.)

Input Condition:

$A_0, A_1, A_2, A_3, S_0, S_3, C_n = V_{DD}$

$B_1, B_2, B_3, S_1, S_2, M = GND$

INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST