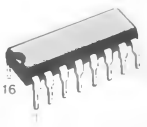
SGS-THOMSON MICROELECTRONICS

M54HC251
M74HC251

8-CHANNEL MULTIPLEXER (3-STATE)

- HIGH SPEED
  t_{PD} = 18 ns (TYP.) at V_{CC} = 5V
- LOW POWER DISSIPATION
  I_{CC} = 4 μA (MAX.) at T_A = 25°C 6V
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28% V_{CC} (MIN).
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2V to 6V
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS251



B1N
Plastic Package

F1
Ceramic Frit Seal Package

M1
Micro Package

C1
Plastic Chip Carrier

ORDERING NUMBERS:
M54HC251 F1
M74HC251 B1N
M74HC251 F1
M74HC251 C1
M74HC251 M1

DESCRIPTION

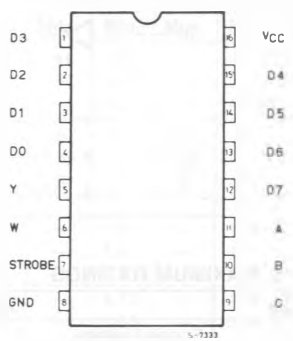
The M54/74HC251 is a high speed CMOS 8-CHANNEL MULTIPLEXER (3-STATE) fabricated in silicon gate C²MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low power consumption. This multiplexer features both true (Y) and complement (W) outputs as well as a STROBE input. The STROBE must be at a low logic level to enable this device. When the STROBE input is high, both outputs are in the high impedance state. When enabled, address information on the data select inputs determines which data input is routed to Y and W. All inputs are equipped with protection circuits against static discharge and transient excess voltage.

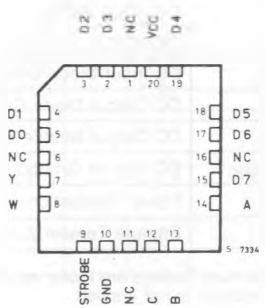
TRUTH TABLE

INPUTS				OUTPUTS	
SELECT			STROBE		
C	B	A	S	Y	W
X	X	X	H	Z	Z
L	L	L	L	D0	$\overline{D0}$
L	L	H	L	D1	$\overline{D1}$
L	H	L	L	D2	$\overline{D2}$
L	H	H	L	D3	$\overline{D3}$
H	L	L	L	D4	$\overline{D4}$
H	L	H	L	D5	$\overline{D5}$
H	H	L	L	D6	$\overline{D6}$
H	H	H	L	D7	$\overline{D7}$

Z: HIGH IMPEDANCE X: DON'T CARE

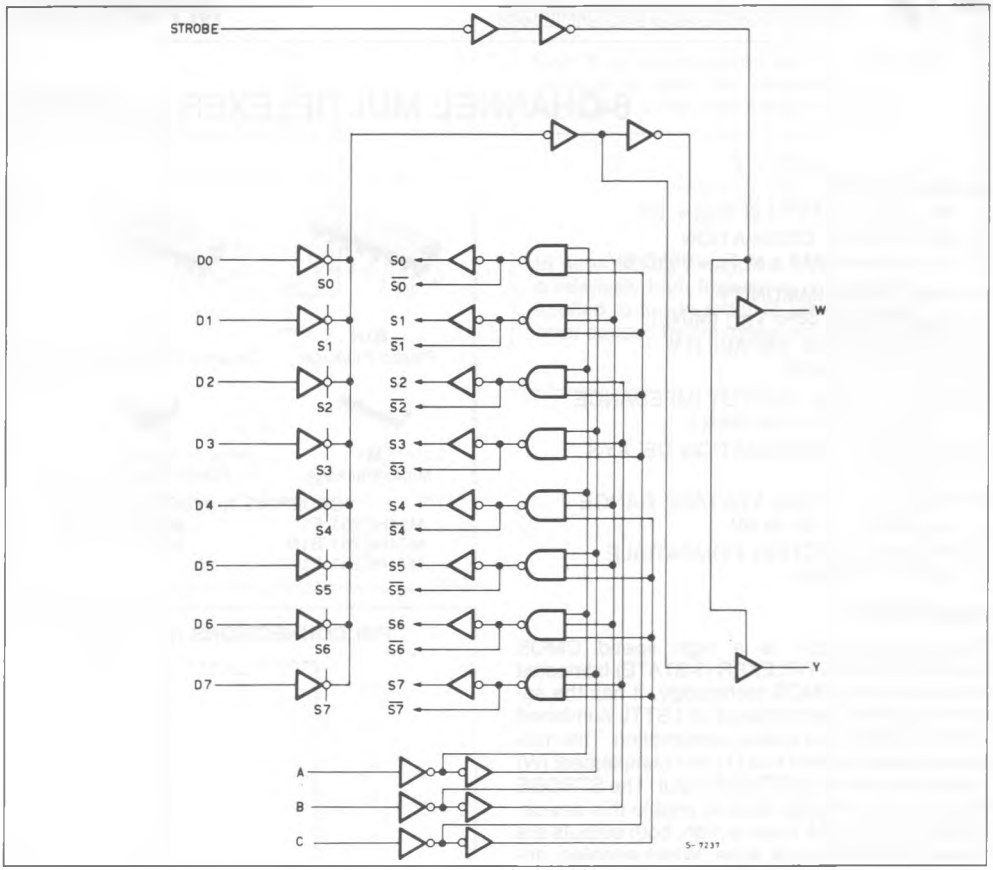
PIN CONNECTIONS (top view)





NC = No Internal Connection

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	− 0.5 to 7	V
V_I	DC Input Voltage	− 0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	− 0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	− 65 to 150	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: ≡ 65°C derate to 300 mW by 10 mW/°C: 65°C to 85°C.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value		Unit
V_{CC}	Supply Voltage		2 to 6		V
V_I	Input Voltage		0 to V_{CC}		V
V_O	Output Voltage		0 to V_{CC}		V
T_A	Operating Temperature	74HC Series 54HC Series	−40 to 85 −55 to 125		°C
t_r, t_f	Input Rise and Fall Time		V_{CC} = 2 V	0 to 1000	ns
			V_{CC} = 4.5V	0 to 500	
			V_{CC} = 6 V	0 to 400	

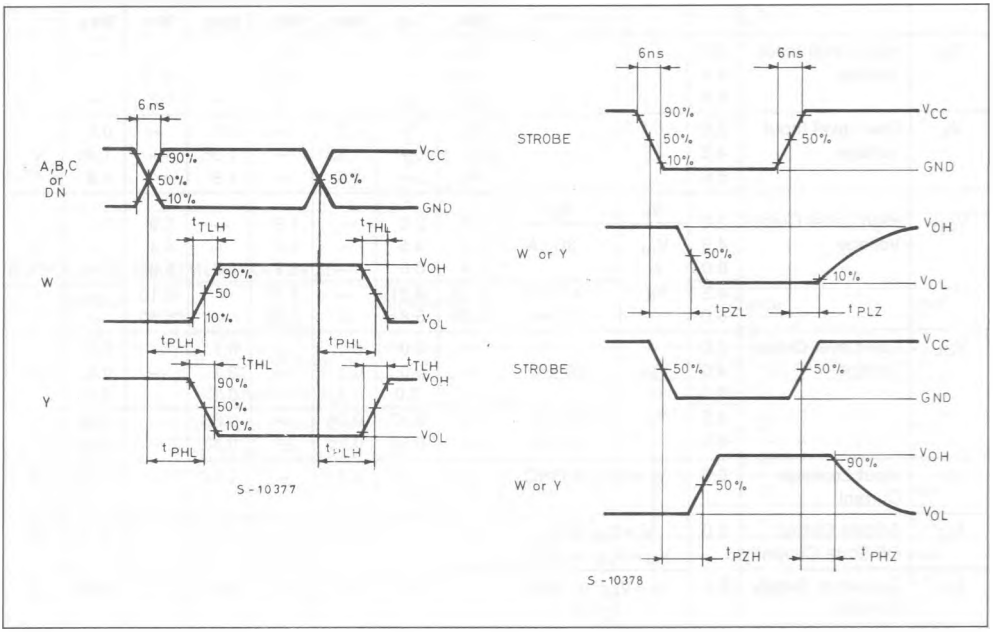
DC SPECIFICATIONS

Symbol	Parameter	V_{CC}	Test Condition		T_A = 25°C 54HC and 74HC			− 40 to 85°C 74HC		− 55 to 125°C 54HC		Unit
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5	—	—	1.5	—	1.5	—	V
		4.5			3.15	—	—	3.15	—	3.15	—	
		6.0			4.2	—	—	4.2	—	4.2	—	
V_{IL}	Low Level Input Voltage	2.0			—	—	0.5	—	0.5	—	0.5	V
		4.5			—	—	1.35	—	1.35	—	1.35	
		6.0			—	—	1.8	—	1.8	—	1.8	
V_{OH}	High Level Output Voltage	2.0	V_I	I_O	1.9	2.0	—	1.9	—	1.9	—	V
		4.5	V_{IH} or V_{IL}	− 20 μA	4.4	4.5	—	4.4	—	4.4	—	
		6.0			5.9	6.0	—	5.9	—	5.9	—	
		4.5		− 4.0 mA	4.18	4.31	—	4.13	—	4.10	—	
		6.0		− 5.2 mA	5.68	5.8	—	5.63	—	5.60	—	
V_{OL}	Low Level Output Voltage	2.0	V_{IH} or V_{IL}	20 μA	—	0.0	0.1	—	0.1	—	0.1	V
		4.5			—	0.0	0.1	—	0.1	—	0.1	
		6.0			—	0.0	0.1	—	0.1	—	0.1	
		4.5		4.0 mA	—	0.17	0.26	—	0.33	—	0.40	
		6.0		5.2 mA	—	0.18	0.26	—	0.33	—	0.40	
I_I	Input Leakage Current	6.0	V_I = V_{CC} or GND		—	—	±0.1	—	±1.0	—	±1.0	μA
I_{OZ}	3-State Output Off-State Current	6.0	V_I = V_{IH} or V_{IL} V_O = V_{CC} or GND		—	—	±0.5	—	±5.0	—	±10	μA
I_{CC}	Quiescent Supply Current	6.0	V_I = V_{CC} or GND I_O = 0		—	—	4	—	40	—	80	μA

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V, T_A = 25°C, C_L = 15pF, Input $t_r = t_f$ = 6ns)

Symbol	Parameter	C_L (pF)	54HC and 74HC			Unit
			Min.	Typ.	Max.	
t_{TLH} t_{THL}	Output Transition Time	15		4	8	ns
t_{PLH} t_{PHL}	Propagation Delay Time (D - W)	15		18	29	ns
t_{PLH} t_{PHL}	Propagation Delay Time (D - Y)	15		17	27	ns
t_{PLH} t_{PHL}	Propagation Delay Time (A, B, C - W)	15		22	35	ns
t_{PLH} t_{PHL}	Propagation Delay Time (A, B, C - Y)	15		21	33	ns
t_{PZH} t_{PZL}	3-State Output Enable Time	15		11	18	ns
t_{PHZ} t_{PLZ}	3-State Output Disable Time	5		9	15	ns

SWITCHING CHARACTERISTICS TEST WAVEFORM

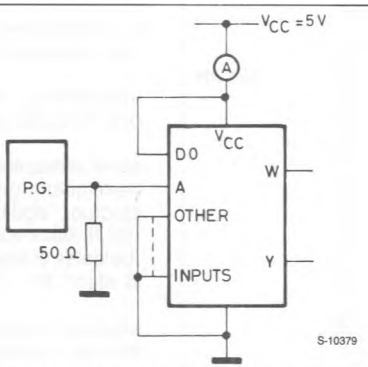


AC ELECTRICAL CHARACTERISTICS (C_L = 50pF, Input $t_r = t_f$ = 6ns)

Symbol	Parameter	V_{CC}	Test Condition	T_A = 25°C 54HC and 74HC			– 40 to 85°C 74HC		– 55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0		—	30	75	—	95		110	ns
		4.5		—	8	15	—	19		22	
		6.0		—	7	13	—	16		19	
t_{PLH} t_{PHL}	Propagation Delay Time (D - W)	2.0		—	76	165	—	205		250	ns
		4.5		—	19	33	—	41		50	
		6.0		—	16	28	—	35		43	
t_{PLH} t_{PHL}	Propagation Delay Time (D - Y)	2.0		—	76	160	—	200		240	ns
		4.5		—	19	32	—	40		48	
		6.0		—	16	27	—	34		41	
t_{PLH} t_{PHL}	Propagation Delay Time (A, B, C - W)	2.0		—	96	205	—	255		310	ns
		4.5		—	24	41	—	51		62	
		6.0		—	20	35	—	43		53	
t_{PLH} t_{PHL}	Propagation Delay Time (A, B, C, - Y)	2.0		—	96	195	—	245		295	ns
		4.5		—	24	39	—	49		59	
		6.0		—	20	34	—	42		50	
t_{PZL} t_{PZH}	3 State Output Enable Time	2.0		—	52	105	—	130		160	ns
		4.5		—	13	21	—	26		32	
		6.0		—	11	18	—	22		27	
t_{PLZ} t_{PHZ}	3 State Output Disable Time	2.0		—	60	105	—	130		160	ns
		4.5		—	15	21	—	26		32	
		6.0		—	13	18	—	22		27	
C_{IN}	Input Capacitance			—	5	10	—	10		10	pF
C_{OUT}	Output Capacitance			—	10	—	—	—	—	—	pF
C_{PD} (*)	Power Dissipation Capacitance			—	100	—	—	—			pF

Note (*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to test Circuit)
Average operating current can be obtained by the following equation. $I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$

TEST WAVEFORM I_{CC} (Opr.)



INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST