SGS-THOMSON MICROELECTRONICS

# M54HC367/368
# M74HC367/368

## HEX BUS BUFFER (3-STATE)
## HC367 NON-INVERTING, HC368 INVERTING

- HIGH SPEED
  $t_{PD}$ = 13 ns (TYP.) at $V_{CC}$ = 5V
- LOW POWER DISSIPATION
  $I_{CC}$ = 4 $\mu$A (MAX.) at $T_A$ = 25°C 6V
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28% $V_{CC}$ (MIN).
- OUTPUT DRIVE CAPABILITY
  15 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 6 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  $V_{CC}$ (OPR) = 2V to 6V
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS367/368

**B1N**
Plastic Package

**F1**
Ceramic Frit Seal Package

**M1**
Micro Package

**C1**
Plastic Chip Carrier

ORDERING NUMBERS:

M54HCXXX F1
M74HCXXX B1N
M74HCXXX F1
M74HCXXX C1
M74HCXXX M1

### DESCRIPTION

The M54/74HC367 and the M54/74HC368 are high speed CMOS HEX BUS BUFFER (3-STATE) fabricated in silicon gate C²MOS technology. They have the same high speed performance of LSTTL combined with true CMOS low power consumption. These devices contain six buffers, four buffers are controlled by an enable input ($\overline{G1}$) and the other two buffers are controlled by the other enable input ($\overline{G2}$); the outputs of each buffer group are enabled when $\overline{G1}$ and/or $\overline{G2}$ inputs are held low, and when held high these outputs are disabled to be high-impedance.
These outputs are capable of driving up to 15 LSTTL loads. The designer has a choice of non-inverting outputs (HC367) and inverting outputs (HC368).
All inputs are equipped with protection circuits against static discharge and transient excess voltage.

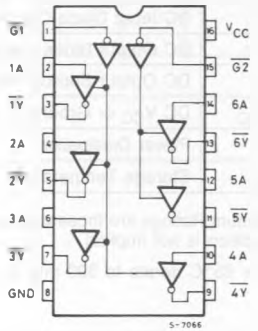
### TRUTH TABLE

| INPUTS | | OUTPUTS | |
|---|---|---|---|
| $\overline{G}$ | An | Yn (367) | $\overline{Yn}$ (368) |
| L | L | L | H |
| L | H | H | L |
| H | X | Z | Z |

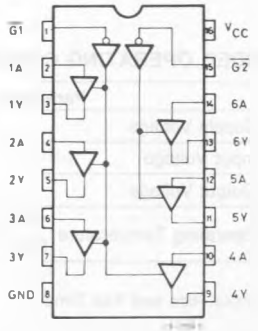
X: DON'T CARE Z: HIGH IMPEDANCE

**PIN CONNECTIONS** (top view)

HC367




HC368



## CHIP CARRIER


NC = No internal Connection

## ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{CC}$ | Supply Voltage | − 0.5 to 7 | V |
| $V_I$ | DC Input Voltage | − 0.5 to $V_{CC}$ + 0.5 | V |
| $V_O$ | DC Output Voltage | − 0.5 to $V_{CC}$ + 0.5 | V |
| $I_{IK}$ | DC Input Diode Current | ± 20 | mA |
| $I_{OK}$ | DC Output Diode Current | ± 20 | mA |
| $I_O$ | DC Output Source Sink Current Per Output Pin | ± 35 | mA |
| $I_{CC}$ or $I_{GND}$ | DC $V_{CC}$ or Ground Current | ± 70 | mA |
| $P_D$ | Power Dissipation | 500 (*) | mW |
| $T_{stg}$ | Storage Temperature | − 65 to 150 | °C |

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: ≡ 65°C derate to 300 mW by 10 mW/°C: 65°C to 85°C

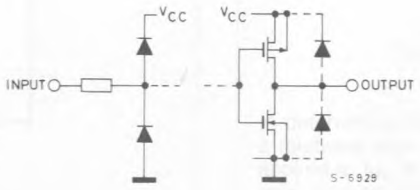
## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Value | | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | 2 to 6 | | V |
| $V_I$ | Input Voltage | 0 to $V_{CC}$ | | V |
| $V_O$ | Output Voltage | 0 to $V_{CC}$ | | V |
| $T_A$ | Operating Temperature 74HC Series<br>54HC Series | − 40 to 85<br>− 55 to 125 | | °C |
| $t_r$, $t_f$ | Input Rise and Fall Time | $V_{CC}$ = 2 V | 0 to 1000 | ns |
| | | $V_{CC}$ = 4.5V | 0 to 500 | |
| | | $V_{CC}$ = 6 V | 0 to 400 | |

## DC SPECIFICATIONS

| Symbol | Parameter | $V_{CC}$ | Test Condition | | $T_A = 25°C$ 54HC and 74HC | | | −40 to 85°C 74HC | | −55 to 125°C 54HC | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | Min. | Typ. | Max. | Min. | Max. | Min. | Max. | |
| $V_{IH}$ | High Level Input Voltage | 2.0 | | | 1.5 | — | — | 1.5 | — | 1.5 | — | V |
| | | 4.5 | | | 3.15 | — | — | 3.15 | — | 3.15 | — | |
| | | 6.0 | | | 4.2 | — | — | 4.2 | — | 4.2 | — | |
| $V_{IL}$ | Low Level Input Voltage | 2.0 | | | — | — | 0.5 | — | 0.5 | — | 0.5 | V |
| | | 4.5 | | | — | — | 1.35 | — | 1.35 | — | 1.35 | |
| | | 6.0 | | | — | — | 1.8 | — | 1.8 | — | 1.8 | |
| $V_{OH}$ | High Level Output Voltage | 2.0 | $V_I$ | $I_O$ | 1.9 | 2.0 | — | 1.9 | — | 1.9 | — | V |
| | | 4.5 | $V_{IH}$ or $V_{IL}$ | −20 μA | 4.4 | 4.5 | — | 4.4 | — | 4.4 | — | |
| | | 6.0 | | | 5.9 | 6.0 | — | 5.9 | — | 5.9 | — | |
| | | 4.5 | | −6.0 mA | 4.18 | 4.31 | — | 4.13 | — | 4.10 | — | |
| | | 6.0 | | −7.8 mA | 5.68 | 5.8 | — | 5.63 | — | 5.60 | — | |
| $V_{OL}$ | Low Level Output Voltage | 2.0 | $V_{IH}$ or $V_{IL}$ | 20 μA | — | 0.0 | 0.1 | — | 0.1 | — | 0.1 | V |
| | | 4.5 | | | — | 0.0 | 0.1 | — | 0.1 | — | 0.1 | |
| | | 6.0 | | | — | 0.0 | 0.1 | — | 0.1 | — | 0.1 | |
| | | 4.5 | | 6.0 mA | — | 0.17 | 0.26 | — | 0.33 | — | 0.40 | |
| | | 6.0 | | 7.8 mA | — | 0.18 | 0.26 | — | 0.33 | — | 0.40 | |
| $I_I$ | Input Leakage Current | 6.0 | $V_I = V_{CC}$ or GND | | — | — | ±0.1 | — | ±1.0 | — | ±1.0 | μA |
| $I_{OZ}$ | 3-State Output Off-State Current | 6.0 | $V_I = V_{IH}$ or $V_{IL}$<br>$V_O = V_{CC}$ or GND | | — | — | ±0.5 | — | ±5.0 | — | ±10 | μA |
| $I_{CC}$ | Quiescent Supply Current | 6.0 | $V_I = V_{CC}$ or GND<br>$I_O = 0$ | | — | — | 4 | — | 40 | — | 80 | μA |

## INPUT AND OUTPUT EQUIVALENT CIRCUIT



**AC ELECTRICAL CHARACTERISTICS** ($C_L$ = 50pF, Input $t_r = t_f$ = 6ns)

| Symbol | Parameter | $V_{CC}$ | Test Condition | $T_A$ = 25°C 54HC and 74HC | | | – 40 to 85°C 74HC | | – 55 to 125°C 54HC | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Min. | Typ. | Max. | Min. | Max. | Min. | Max. | |
| $t_{TLH}$ $t_{THL}$ | Output Transition Time | 2.0 | | — | 22 | 60 | — | 75 | — | 90 | ns |
| | | 4.5 | | — | 8 | 12 | — | 15 | — | 18 | |
| | | 6.0 | | — | 7 | 10 | — | 13 | — | 15 | |
| $t_{PLH}$ $t_{PHL}$ | Propagation Delay Time * | 2.0 | | — | 60 | 120 | — | 150 | — | 180 | ns |
| | | 4.5 | | — | 15 | 24 | — | 30 | — | 36 | |
| | | 6.0 | | — | 13 | 20 | — | 26 | — | 31 | |
| $t_{PLH}$ $t_{PHL}$ | Propagation Delay Time ** | 2.0 | | — | 56 | 115 | — | 145 | — | 175 | ns |
| | | 4.5 | | — | 14 | 23 | — | 29 | — | 35 | |
| | | 6.0 | | — | 12 | 20 | — | 25 | — | 30 | |
| $t_{PZL}$ $t_{PZH}$ | Output Enable Time | 2.0 | $R_L$ = 1KΩ | — | 60 | 120 | — | 150 | — | 180 | ns |
| | | 4.5 | | — | 15 | 24 | — | 30 | — | 36 | |
| | | 6.0 | | — | 13 | 20 | — | 26 | — | 31 | |
| $t_{PLZ}$ $t_{PHZ}$ | Output Disable Time | 2.0 | $R_L$ = 1KΩ | — | 63 | 150 | — | 190 | — | 225 | ns |
| | | 4.5 | | — | 20 | 30 | — | 38 | — | 45 | |
| | | 6.0 | | — | 18 | 26 | — | 33 | — | 38 | |
| $C_{IN}$ | Input Capacitance | — | | — | 5 | 10 | — | 10 | — | 10 | pF |
| $C_{OUT}$ | Output Capacitance | — | | — | 10 | — | — | — | — | — | |
| $C_{PD}$ (1) | Power Dissipation Capacitance | — | HC 367 | — | 34 | — | — | — | — | — | pF |
| | | — | HC 368 | — | 32 | — | — | — | — | — | |

Note (1) $C_{PD}$ is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit)

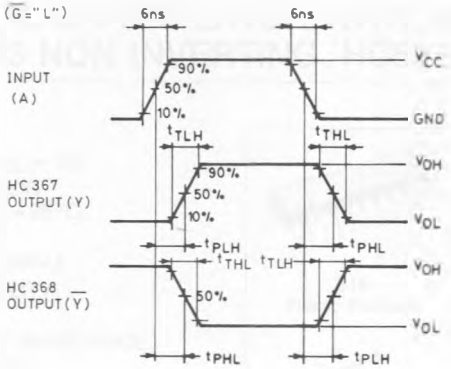
Average operating current can be obtained by the following equation.

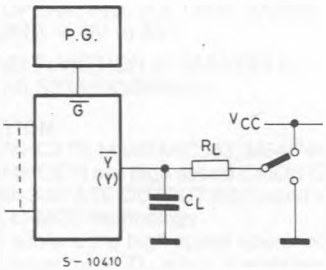
$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/6$ (per circuit).

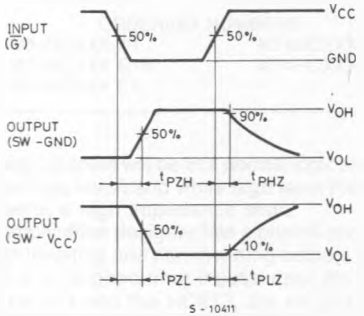
* For M54/74HC367 only

** For M54/74HC368 only

## SWITCHING CHARACTERISTICS TEST WAVEFORM

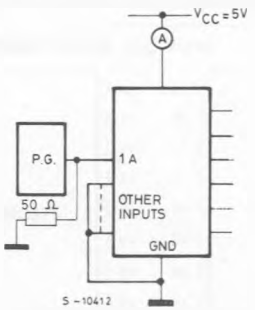



NOTE: SUCH A LOGIC LEVEL SHALL BE APPLIED TO EACH INPUT THAT THE OUTPUT VOLTAGE STAYS IN THE APPOSITE SIDE TO THE SWITCH CONNECTION LEVEL, WHEN THE OUTPUT IS ENABLE

## TEST CIRCUIT $I_{CC}$ (Opr.)




INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST

## $C_{PD}$ CALCULATION

$C_{PD}$ is to be calculated with the following formula by using the measured value of $I_{CC}$ (Opr.) in the test circuit opposite

$$C_{PD} = \frac{I_{CC}\ (Opr.)}{f_{IN} \cdot V_{CC}}$$

In determining the typical value of $C_{PD}$, a relatively high frequency of 1 MHz was applied to $f_{IN}$, in order to eliminate any error caused by the quiescent supply current.