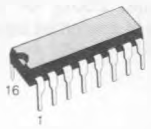
SGS-THOMSON MICROELECTRONICS

M54/74HC40102
M54/74HC40103

8 STAGE PRESETTABLE SYNCHRONOUS DOWN COUNTERS

- HIGH SPEED
  f_{MAX} = 34 MHz (Typ) at V_{CC} = 5V
- LOW POWER DISSIPATION
  I_{CC} = 4 μA (MAX.) at T_A = 25°C
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28% V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2V to 6V
- PIN AND FUNCTION COMPATIBLE
  WITH 40102B/40103B



B1N
Plastic Package

F1
Ceramic Frit Seal Package

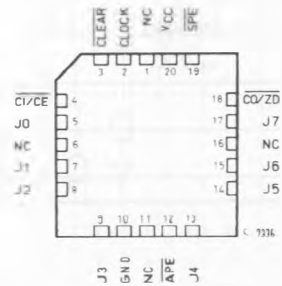
M1
Micro Package

C1
Plastic Chip Carrier

ORDERING NUMBERS:

M54HCXXXX F1
M74HCXXXX B1N
M74HCXXXX F1
M74HCXXXX C1
M74HCXXXX M1

PIN CONNECTION (top view)



NC = No Internal Connection

DESCRIPTION

The M54/74HC40102/40103 are high speed CMOS 8-STAGE PRESETTABLE SYNCHRONOUS DOWN COUNTERS fabricated with silicon gate C²MOS technology. They achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

The HC40102, and HC40103 consist of an 8-stage synchronous down counter with a single output which is active when the internal count is zero. The HC40102 is configured as two cascaded 4-bit BCD counters, and the HC40103 contains a single 8-bit binary counter. Each type has control inputs for enabling or disabling the clock, for clearing the counter to its maximum count, and for presetting the counter either synchronously or asynchronously. All control inputs and the CARRY-OUT/ZERO-DETECT output are active-low logic. In normal operation, the counter is decremented by one count on each positive transition of the CLOCK. Counting is inhibited when the CARRY-IN/COUNTER ENABLE ($\overline{CI/CE}$) input is high. The CARRY-OUT/ZERO-DETECT ($\overline{CO/ZD}$) output goes low when the count reaches zero if the $\overline{CI/CE}$ input is low, and remains low for one full clock period. When the SYNCHRONOUS PRESET-ENABLE ($\overline{SPE}$) input is low, data at the J input is clocked into the counter on the next positive clock transition regardless of the state of the $\overline{CI/CE}$ input.

DESCRIPTION (Continued)

When the ASYNCHRONOUS PRESET-ENABLE ($\overline{APE}$) input is low, data at the J inputs is asynchronously forced into the counter regardless of the state of the $\overline{SPE}$, $\overline{CI/CE}$, or CLOCK inputs. J Inputs J0-J7 represent two 4-bit BCD words for the HC40102 and a single 8-bit binary word for the HC40103. When the CLEAR ($\overline{CLR}$ input is low, the counter is asynchronously cleared to its maximum count ($99_{10}$for the HC40102 and 255_{10} for the HC40103 regardless of the state of any other input.

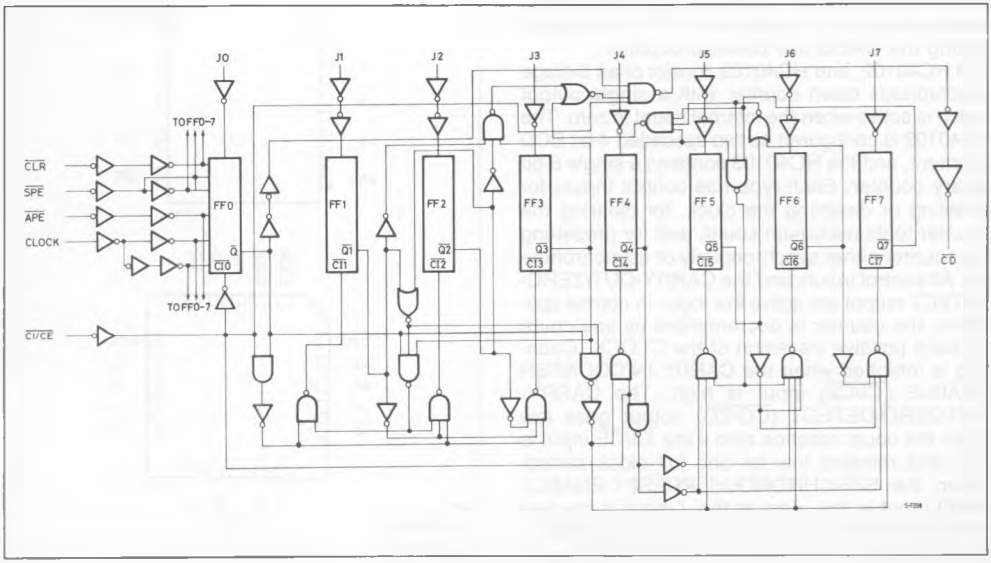
The precedence relationship between control input is indicated in the truth table. If all control inputs are high at the time of zero count, the counters will jump to the maximum count, giving a counting sequence of 100 or 256 clock pulses long. The HC40102 and HC40103 may be cascaded using the $\overline{CI/CE}$ input and the $\overline{CO/ZD}$ output, in either a synchronous or ripple mode. All inputs are equipped with protection circuits against static discharge and transient excess voltage.

TRUTH TABLE

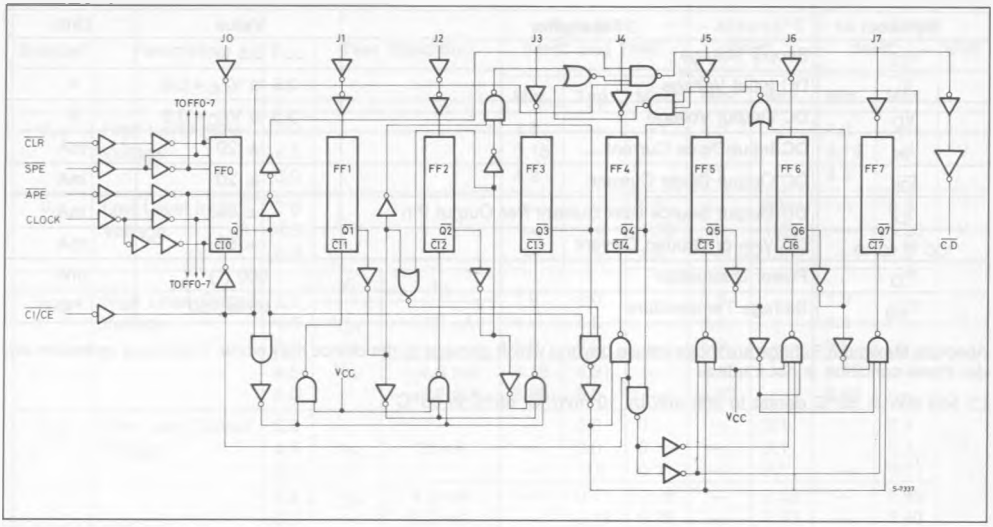
CONTROL INPUTS				MODE	FUNCTIONAL DESCRIPTION
$\overline{CLEAR}$	$\overline{APE}$	$\overline{SPE}$	$\overline{CI/CE}$		
H	H	H	H	COUNT INHIBIT	EVEN IF CLOCK IS GIVEN, NO COUNT IS MADE.
H	H	H	L	REGULAR COUNT	DOWN COUNT AT RISING EDGE OF CLOCK.
H	H	L	X	SYNCHRONOUS PRESET	DATA OF PI TERMINAL IS PRESET AT RISING EDGE OF CLOCK
H	L	X	X	ASYNCHRONOUS PRESET	DATA OF PI TERMINAL IS ASYNCHRONOUSLY PRESET TO CLOCK
L	X	X	X	CLEAR	COUNTER IS SET TO MAXIMUM COUNT.

X. DON'T CARE — MAXIMUM COUNT: "99" FOR HC40102 AND "255" FOR HC40103

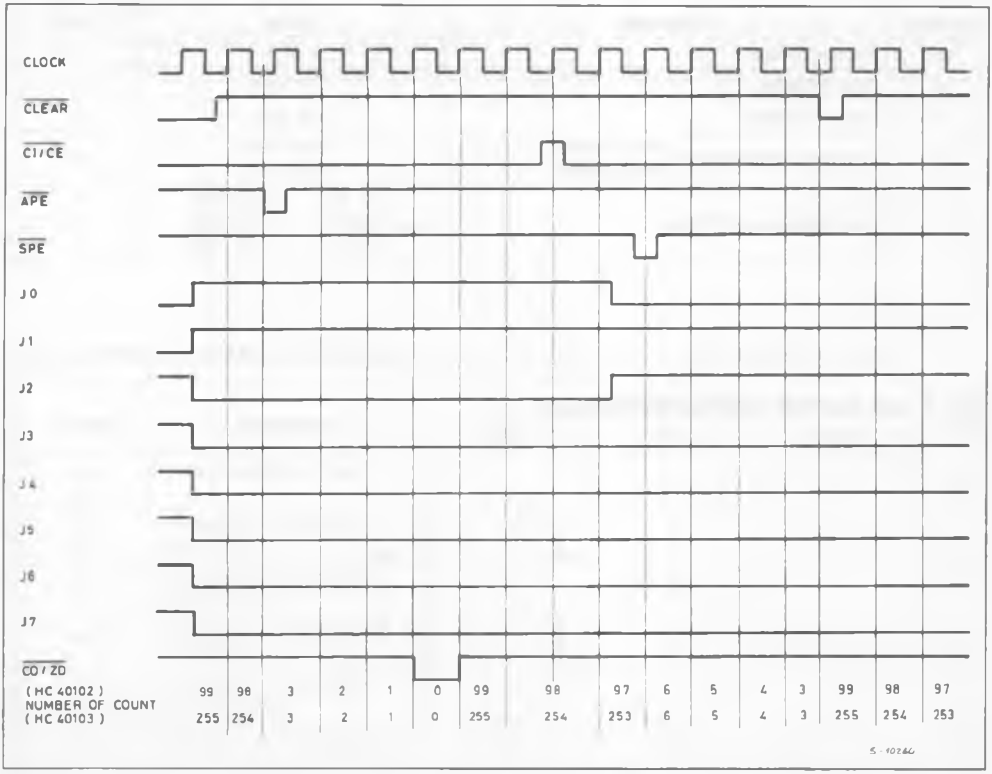
LOGIC DIAGRAM (HC40102)



LOGIC DIAGRAM (HC40103)



TIMING CHART



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to 7	V
V_I	DC Input Voltage	−0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	−0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	−65 to 150	°C

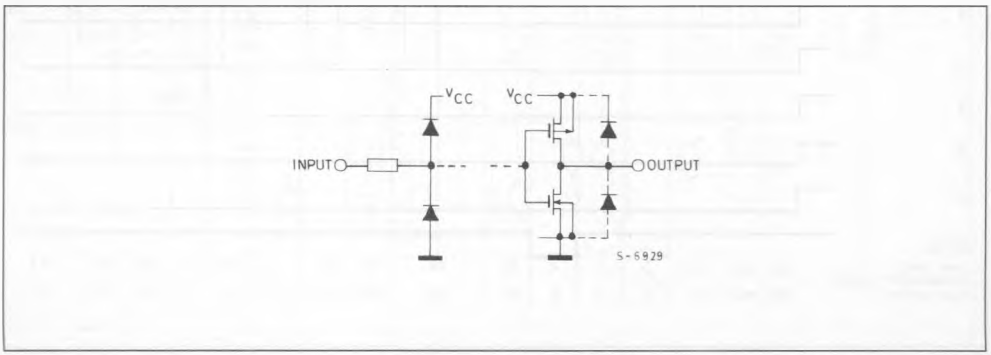
Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: ≅ 65°C derate to 300 mW by 10 mW/°C: 65°C to 85°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value		Unit
V_{CC}	Supply Voltage	2 to 6		V
V_I	Input Voltage	0 to V_{CC}		V
V_O	Output Voltage	0 to V_{CC}		V
T_A	Operating Temperature 74HC Series 54HC Series	−40 to 85 −55 to 125		°C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V	0 to 1000	ns
		V_{CC} = 4.5V	0 to 500	
		V_{CC} = 6 V	0 to 400	

INPUT AND OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	V_{CC}	Test Condition		$T_A = 25°C$ 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5	—	—	1.5	—	1.5	—	V
		4.5			3.15	—	—	3.15	—	3.15	—	
		6.0			4.2	—	—	4.2	—	4.2	—	
V_{IL}	Low Level Input Voltage	2.0			—	—	0.5	—	0.5	—	0.5	V
		4.5			—	—	1.35	—	1.35	—	1.35	
		6.0			—	—	1.8	—	1.8	—	1.8	
V_{OH}	High Level Output Voltage	2.0	V_I	I_O	1.9	2.0	—	1.9	—	1.9	—	V
		4.5	V_{IH} or V_{IL}	−20 μA	4.4	4.5	—	4.4	—	4.4	—	
		6.0			5.9	6.0	—	5.9	—	5.9	—	
		4.5		−4.0 mA	4.18	4.31	—	4.13	—	4.10	—	
		6.0		−5.2 mA	5.68	5.8	—	5.63	—	5.60	—	
V_{OL}	Low Level Output Voltage	2.0	V_{IH} or V_{IL}	20 μA	—	0.0	0.1	—	0.1	—	0.1	V
		4.5			—	0.0	0.1	—	0.1	—	0.1	
		6.0			—	0.0	0.1	—	0.1	—	0.1	
		4.5		4.0 mA	—	0.17	0.26	—	0.33	—	0.40	
		6.0		5.2 mA	—	0.18	0.26	—	0.33	—	0.40	
I_I	Input Leakage Current	6.0	$V_I = V_{CC}$ or GND		—	—	±0.1	—	±1.0	—	±1.0	μA
I_{CC}	Quiescent Supply Current	6.0	$V_I = V_{CC}$ or GND		—	—	4	—	40	—	80	μA

AC ELECTRICAL CHARACTERISTICS ($V_{CC} = 5V$, $T_A = 25°C$, $C_L = 15pF$, Input $t_r = t_f = 6ns$)

Symbol	Parameter	54HC and 74HC			Unit
		Min.	Typ.	Max.	
t_{TLH} t_{THL}	Output Transition Time		4	8	ns
t_{PLH} t_{PHL}	Propagation Delay Time CK-$\overline{CO}$/ZO		27	42	ns
t_{PHL}	Propagation Delay Time ($\overline{APE}$-$\overline{CO}$/ZD)		34	53	ns
t_{PHL}	Propagation Delay Time ($\overline{CL}$-$\overline{CO}$/ZD)		27	42	ns
t_{PHL}	Propagation Delay Time ($\overline{CI}$/$\overline{CE}$-$\overline{CO}$/$\overline{ZO}$)		11	18	ns
f_{MAX}	Maximum Clock Frequency	22	34		MHz

AC ELECTRICAL CHARACTERISTICS ($C_L = 50pF$, Input $t_r = t_f = 6ns$)

Symbol	Parameter	V_{CC}	Test Condition	T_A = 25°C 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0		—	30	75	—	95		110	ns
		4.5		—	8	15	—	19		22	
		6.0		—	7	13	—	16		19	
t_{PLH} t_{PHL}	Propagation Delay Time (CLOCK - CO/ZD)	2.0		—	128	245	—	305		370	ns
		4.5		—	32	49	—	61		74	
		6.0		—	27	42	—	52		63	
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{APE}$ - $\overline{CO/ZD}$)	2.0		—	156	300	—	380		450	ns
		4.5		—	39	60	—	76		90	
		6.0		—	33	52	—	66		76	
t_{PLH}	Propagation Delay Time ($\overline{CL}$ - $\overline{CO/ZD}$)	2.0		—	124	240	—	300		360	ns
		4.5		—	31	48	—	60		72	
		6.0		—	27	41	—	51		61	
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{CI/CE}$ - $\overline{CO/ZO}$)	2.0		—	56	115	—	145		175	ns
		4.5		—	14	23	—	29		35	
		6.0		—	12	20	—	25		30	
f_{MAX}	Maximum Clock Frequency	2.0		4	8	—	3.2	—	2.6	—	MHz
		4.5		20	31	—	16	—	13	—	
		6.0		24	36	—	18	—	15	—	
$t_{W(H)}$ $t_{W(L)}$	Minimum Pulse Width (CLOCK)	2.0		—	30	75	—	95		110	ns
		4.5		—	8	15	—	19		22	
		6.0		—	7	13	—	16		19	
$t_{W(L)}$	Minimum Pulse Width ($\overline{CL}$, $\overline{APE}$)	2.0		—	30	75	—	95		110	ns
		4.5		—	8	15	—	19		22	
		6.0		—	7	13	—	16		19	
t_s	Minimum Set-up Time ($\overline{SPE}$ - CK)	2.0		—	30	75	—	95		110	ns
		4.5		—	7	15	—	19		22	
		6.0		—	6	13	—	16		19	
t_s	Minimum Set-up Time ($\overline{CI/CE}$ - CK)	2.0		—	56	125	—	155	—	190	ns
		4.5		—	14	25	—	31	—	38	
		6.0		—	12	21	—	26	—	32	
t_s	Minimum Set up Time (Jn-CK)	2.0		—	30	75	—	95	—	110	ns
		4.5		—	8	15	—	19	—	22	
		6.0		—	7	13	—	16	—	19	
t_h	Minimum Hold Time (All inputs)	2.0		—	—	5	—	5		5	ns
		4.5		—	—	5	—	5		5	
		6.0		—	—	5	—	5		5	
t_{REM}	Minimum Removal Time ($\overline{CL}$ - $\overline{APE}$)	2.0		—	20	75	—	95		110	ns
		4.5		—	5	15	—	19		22	
		6.0		—	4	13	—	16		19	
t_s	Minimum Set-up Time (Jn $\overline{APE}$)	2.0		—	30	75	—	95		110	ns
		4.5		—	8	15	—	19		22	
		6.0		—	7	13	—	16		19	
C_{IN}	Input Capacitance			—	5	10	—	10		10	pF
C_{PD} (*)	Power Dissipation Capacitance		M54/74HC40102	—	110	—	—	—			pF
			M54/74HC40103	—	128	—	—	—			

Note (*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the following equation.
I_{CC} (Opr.)•C_{PD}•V_{CC}•f_{IN} + I_{CC}

FUNCTIONAL DESCRIPTION

The HC40102 and HC40103 are 8-stage presettable synchronous down counters. Carry Out/Zero Detect ($\overline{CO/ZD}$) is output at the "L" level for the period of 1 bit when the readout becomes "0". The HC40102 adopts binary coded decimal notation, making setting up to 99 counts possible. While the HC40103 adopts 8-bit binary counter and can set up to 255 counts.

Count operation

At the "H" level of control input of $\overline{CLEAR}$, $\overline{SPE}$ and $\overline{APE}$, the counter carriers out down count operation one by one at the rise of pulse given to CLOCK input. Count operation can be inhibited by setting Carry Input/Clock Enable $\overline{CI/CE}$ to the "H" level.

$\overline{CO/ZD}$ is output at the "L" level when the readout becomes "0", but is not output even if the readout becomes "0" when $\overline{CI/CE}$ is at the "H" level, thus maintaining the "H" level.

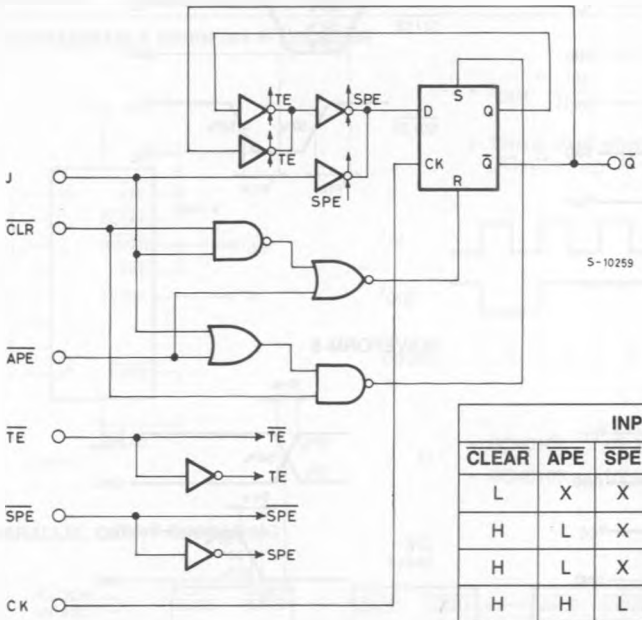
Synchronous cascade operation can be carried out by using $\overline{CI/CE}$ input and $\overline{CO/ZD}$ output.

The contents of count jump to maximum count (99 for the HC40102 and 225 for the HC40103) if clock is given when the readout is "0". Therefore, operation of 100-frequency division and that of 256-frequency division are carried out for the HC40102 and HC40103, respectively, when clock input alone is given without various kinds of preset operation.

Preset operation and reset operation

When Clear ($\overline{CLEAR}$) input is set to the "L" level, the readout is set to the maximum count independetly of other inputs. When Asynchronous Preset Enable ($\overline{APE}$) input is set to the "L" level, readouts given on J0 to J7 can be preset asynchronously to counter independently of inputs other than $\overline{CLEAR}$ input. When Synchronous Preset Enable ($\overline{SPE}$) is set to the "L" level, the readouts given on J0 to J7 can be preset to counter synchronously with the rise of clock.

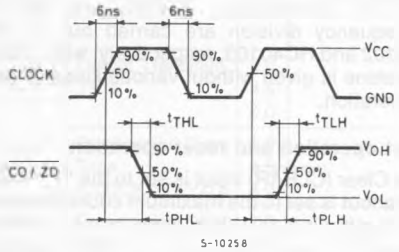
As to these operation modes, refer to the truth table.



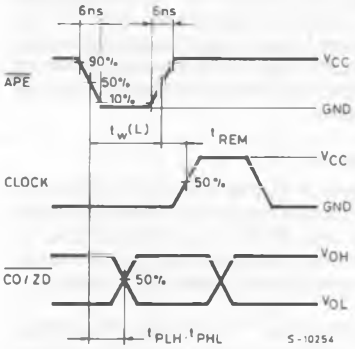
INPUT						OUTPUT
$\overline{CLEAR}$	$\overline{APE}$	$\overline{SPE}$	J	$\overline{TE}$	CLOCK	$\overline{Q}_n+1$
L	X	X	X	X	X	L
H	L	X	L	X	X	L
H	L	X	H	X	X	H
H	H	L	L	X	↓	L
H	H	L	H	X	↓	H
H	H	L	X	X	↑	$\overline{Q_n}$
H	H	H	X	L	↓	Q_n
H	H	H	X	H	X	$\overline{Q_n}$

SWITCHING CHARACTERISTICS TEST WAVEFORM

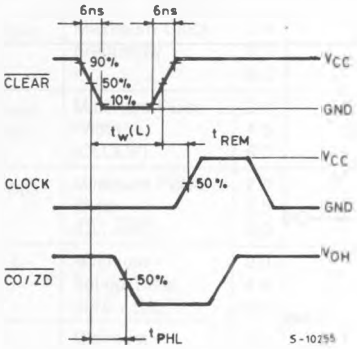
WAVEFORM 1



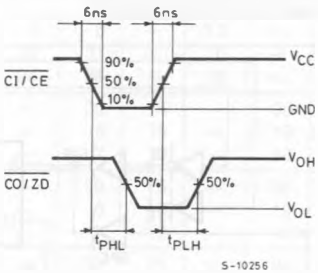
WAVEFORM 2



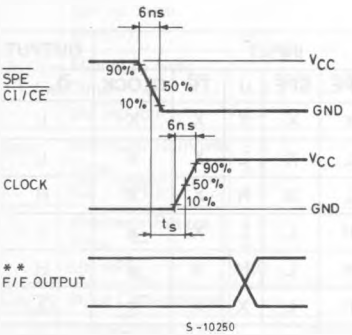
WAVEFORM 3



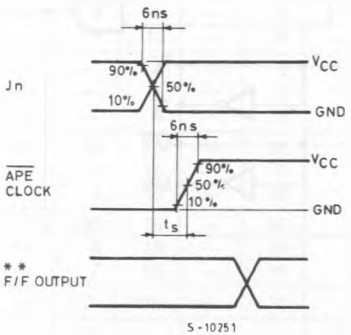
WAVEFORM 4



WAVEFORM 5

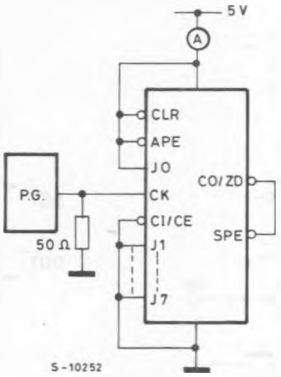


WAVEFORM 6



(** F/F output is internal signal of IC)

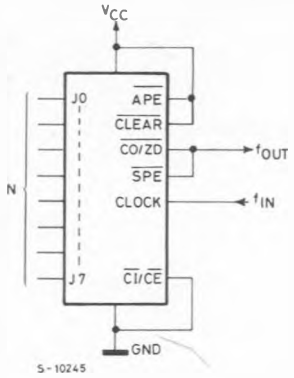
TEST CIRCUIT I_{CC} (Opr.)



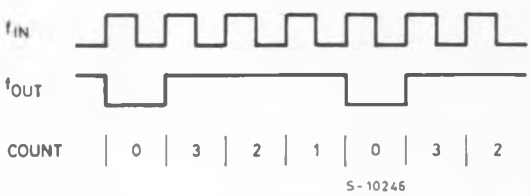
INPUT TRANSITION TIME IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST

EXAMPLE OF TYPICAL APPLICATION

PROGRAMMABLE DIVIDE-BY-N COUNTER

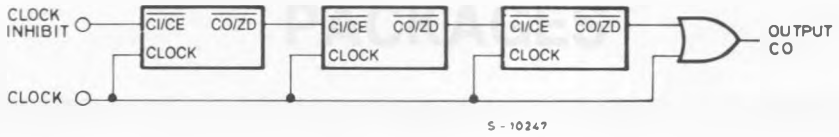


- $f_{OUT} = \frac{f_{IN}}{N+1}$
- Timing chart when N = "3" (JO, J1 = V_{CC}, J2 ~ J7 = GND)



- HC40102 .... 1/2 to 1/100 are dividable
- HC40103 .... 1/2 to 1/256 are dividable

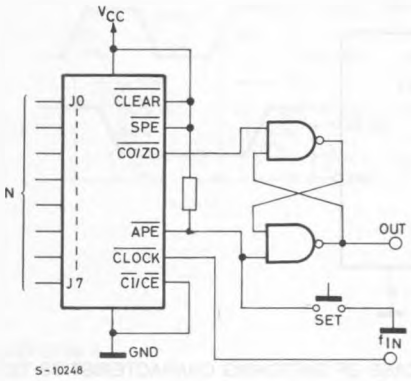
PARALLEL CARRY CASCADING

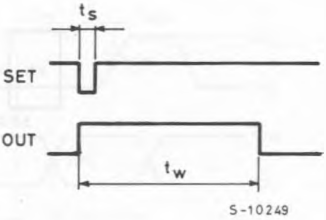


* At synchronous cascade connection, huzzerd occurs at C0 output after its second stage when digit place changes, due to delay arrival. Therefore, take gate from HC32 or the like, not from C0 output at the rear stage directly.

EXAMPLE OF TYPICAL APPLICATION (Continued)

PROGRAMMABLE TIMER





$$t_W = \left(\frac{N}{f_{IN}} + t_S\right)$$

Note: The above formula does not take into account the phase of clock input. Therefore, the real pulse width is the distance between the above formula-$1/f_{IN}$ ~ the above formula.