



7-STAGE BINARY COUNTER

- HIGH SPEED
 $t_{PD} = 15 \text{ ns (TYP.) at } V_{CC} = 5V$
- LOW POWER DISSIPATION
 $I_{CC} = 4 \mu\text{A (MAX.) at } T_A = 25^\circ\text{C}$
- HIGH NOISE IMMUNITY
 $V_{NIH} = V_{NIL} = 28\% V_{CC} \text{ (MIN.)}$
- OUTPUT DRIVE CAPABILITY
 10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
 $|I_{OH}| = I_{OL} = 4 \text{ mA (MIN.)}$
- BALANCED PROPAGATION DELAYS
 $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
 $V_{CC} \text{ (OPR)} = 2V \text{ to } 6V$
- PIN AND FUNCTION COMPATIBLE
 WITH 4024B

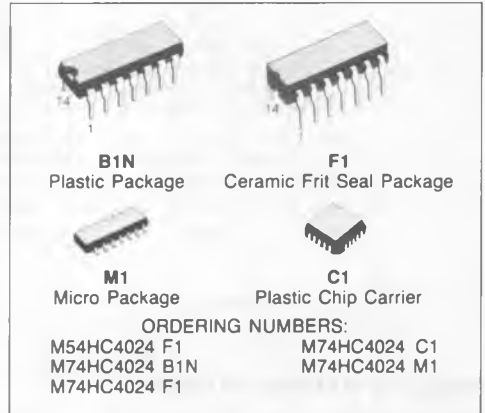
DESCRIPTION

The M54/74HC4024 is a high speed CMOS 7-STAGE BINARY COUNTER fabricated in silicon gate C²MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low power consumption. The HC4024 is a 7 stage Counter. This device is incremented on the falling edge (negative transition) of the input clock, and all its outputs are reset to a low level by applying a logical high on their reset input. All inputs are equipped with protection circuits against static discharge and transient excess voltage.

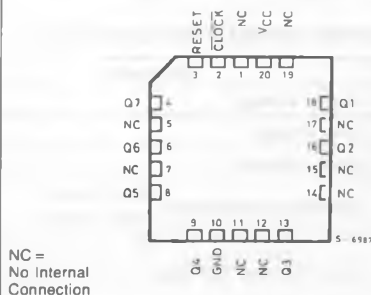
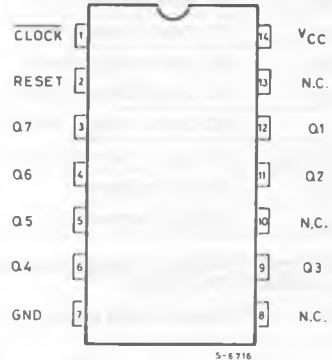
TRUTH TABLE

CLOCK	CLEAR	OUTPUT STATE
X	H	ALL OUTPUTS = "L"
	L	NO CHANGE
	L	ADVANCE TO NEXT STATE

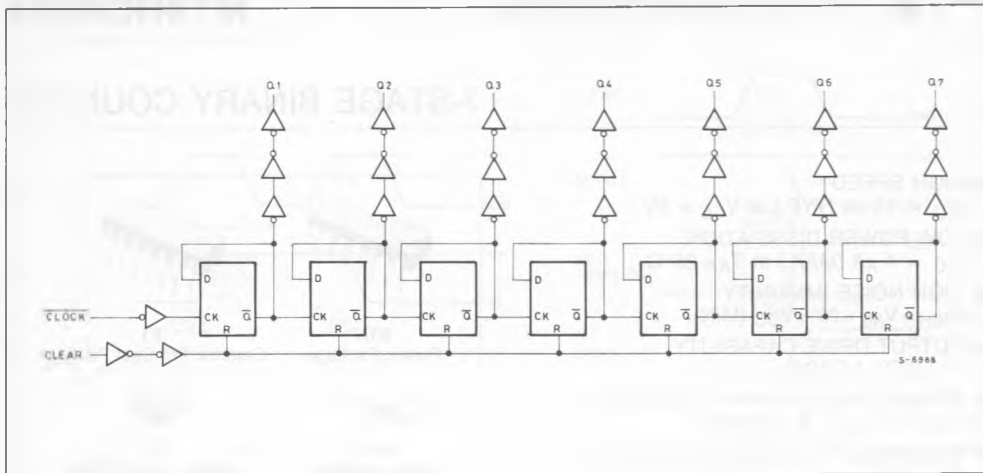
X: DON'T CARE



PIN CONNECTIONS (top view)



LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{CC}	Supply Voltage	- 0.5 to 7	V
V _I	DC Input Voltage	- 0.5 to V _{CC} + 0.5	V
V _O	DC Output Voltage	- 0.5 to V _{CC} + 0.5	V
I _{IK}	DC Input Diode Current	± 20	mA
I _{OK}	DC Output Diode Current	± 20	mA
I _O	DC Output Source Sink Current Per Output Pin	± 25	mA
I _{CC} or I _{GND}	DC V _{CC} or Ground Current	± 50	mA
P _D	Power Dissipation	500 (*)	mW
T _{stg}	Storage Temperature	- 65 to 150	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: ≅ 65°C derate to 300 mW by 10 mW/°C: 65°C to 85°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V _{CC}	Supply Voltage	2 to 6	V
V _I	Input Voltage	0 to V _{CC}	V
V _O	Output Voltage	0 to V _{CC}	V
T _A	Operating Temperature 74HC Series 54HC Series	- 40 to 85 - 55 to 125	°C
t _r , t _f	Input Rise and Fall Time	V _{CC} { 2 V 0 to 1000 4.5V 0 to 500 6 V 0 to 400	ns

DC SPECIFICATIONS

Symbol	Parameter	V _{CC}	Test Condition	T _A = 25°C 54HC and 74HC			- 40 to 85°C 74HC		- 55 to 125°C 54HC		Unit	
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.		
V _{IH}	High Level Input Voltage	2.0		1.5	—	—	1.5	—	1.5	—	V	
		4.5		3.15	—	—	3.15	—	3.15	—		
		6.0		4.2	—	—	4.2	—	4.2	—		
V _{IL}	Low Level Input Voltage	2.0		—	—	0.5	—	0.5	—	0.5	V	
		4.5		—	—	1.35	—	1.35	—	1.35		
		6.0		—	—	1.8	—	1.8	—	1.8		
V _{OH}	High Level Output Voltage	2.0	V _I	I _O	1.9	2.0	—	1.9	—	1.9	—	V
		4.5	V _{IH} or V _{IL}	- 20 μA	4.4	4.5	—	4.4	—	4.4	—	
		6.0			5.9	6.0	—	5.9	—	5.9	—	
		4.5	- 4.0 mA - 5.2 mA	4.18	4.31	—	4.13	—	4.10	—	4.10	
6.0	5.68	5.8		—	5.63	—	5.60	—	5.60	—		
V _{OL}	Low Level Output Voltage	2.0	V _{IH} or V _{IL}	20 μA	—	0.0	0.1	—	0.1	—	0.1	V
		4.5			—	0.0	0.1	—	0.1	—	0.1	
		6.0			—	0.0	0.1	—	0.1	—	0.1	
		4.5			4.0 mA 5.2 mA	—	0.17	0.26	—	0.33	—	
6.0	—	0.18	0.26	—		0.33	—	0.40				
I _I	Input Leakage Current	6.0	V _I = V _{CC} or GND		—	—	± 0.1	—	± 1.0	—	± 1.0	μA
I _{CC}	Quiescent Supply Current	6.0	V _I = V _{CC} or GND		—	—	4	—	40	—	80	μA

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V, T_A = 25°C, C_L = 15pF, Input t_r = t_f = 6ns)

Symbol	Parameter	54HC and 74HC			Unit
		Min.	Typ.	Max.	
t _{TLH} t _{THL}	Output Transition Time		4	8	ns
t _{PLH} t _{PHL}	Propagation Delay Time (Q _N - Q _N + 1)		5	9	ns
t _{PLH} t _{PHL}	Propagation Delay Time (CK - Q ₁)		15	24	ns
t _{PHL}	Propagation Delay Time (CL-Q)		20	31	ns
f _{MAX}	Maximum Clock Frequency	33	60		MHz

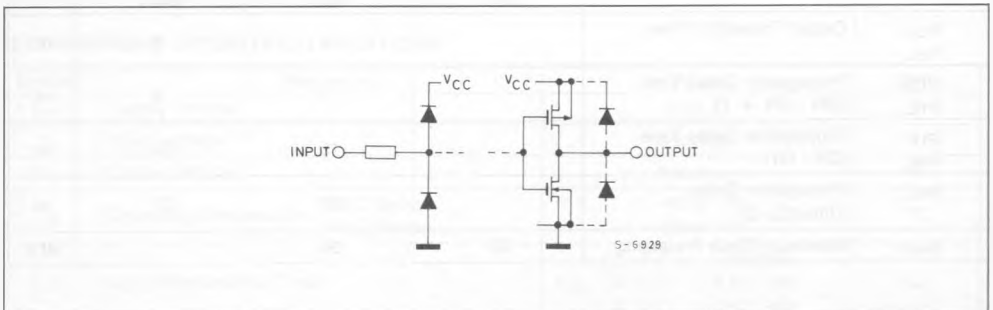
AC ELECTRICAL CHARACTERISTICS ($C_L = 50\text{pF}$, Input $t_r = t_f = 6\text{ns}$)

Symbol	Parameter	V_{CC}	Test Condition	$T_A = 25^\circ\text{C}$ 54HC and 74HC			-40 to 85°C 74HC		-55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0		—	30	75	—	95	—	110	ns
		4.5		—	8	15	—	19	—	22	
		6.0		—	7	13	—	16	—	19	
t_{PLH} t_{PHL}	Propagation Delay Time ($Q_n - Q_{n+1}$)	2.0		—	28	60	—	75	—	90	ns
		4.5		—	7	12	—	15	—	18	
		6.0		—	6	10	—	13	—	15	
t_{PLH} t_{PHL}	Propagation Delay Time (CLOCK-Q1)	2.0		—	72	145	—	180	—	220	ns
		4.5		—	18	29	—	36	—	44	
		6.0		—	15	25	—	31	—	38	
t_{PLH} t_{PHL}	Propagation Delay Time (CLEAR - Q_n)	2.0		—	96	185	—	230	—	280	ns
		4.5		—	24	37	—	46	—	56	
		6.0		—	20	31	—	39	—	48	
f_{MAX}	Maximum Clock Frequency	2.0		6	14	—	4.8	—	4.0	—	MHz
		4.5		30	55	—	24	—	20	—	
		6.0		35	65	—	28	—	24	—	
$t_{W(H)}$ $t_{W(L)}$	Minimum Pulse Width (CLOCK)	2.0		—	30	75	—	95	—	110	ns
		4.5		—	8	15	—	19	—	22	
		6.0		—	7	13	—	16	—	19	
$t_{W(H)}$	Minimum Pulse Width (CLEAR)	2.0		—	30	75	—	95	—	110	ns
		4.5		—	8	15	—	19	—	22	
		6.0		—	7	13	—	16	—	19	
t_{REM}	Minimum Removal Time (CL)	2.0		—	15	50	—	65	—	75	ns
		4.5		—	3	10	—	13	—	15	
		6.0		—	3	9	—	11	—	13	
C_{IN}	Input Capacitance			—	5	10	—	10	—	10	pF
$C_{PD} (*)$	Power Dissipation Capacitance			—	42	—	—	—	—	—	pF

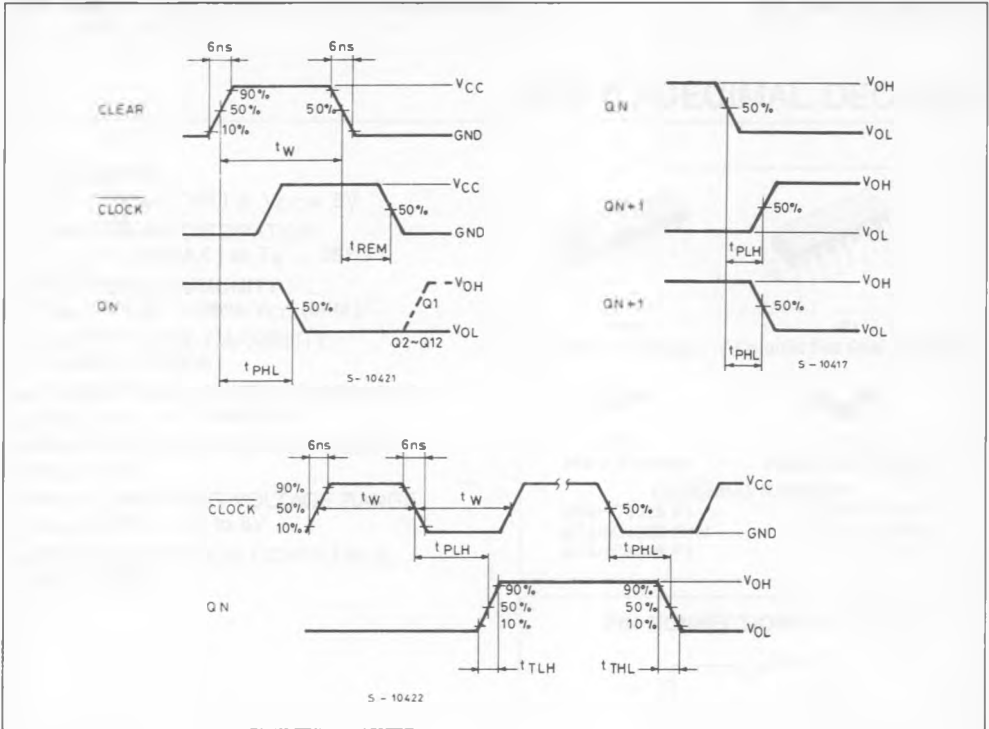
Note (*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit)

Average operating current can be obtained by the following equation: $I_{CC(oper)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$

INPUT AND OUTPUT EQUIVALENT CIRCUIT



SWITCHING CHARACTERISTICS TEST WAVEFORM

TEST CIRCUIT I_{CC} (Opr.)